Field Effect Transistors and Op Amps I

The Field Effect Transistor

This lab begins with some experiments on a junction field effect transistor (JFET), type 2N5458, and then continues with an op amp chip from the TL081/082/084 family. Details of these devices, including pin-out, can be found on the data sheets in the supplementary reading section on your web page. Items marked with an asterisk (*) should be done before coming to lab.

1. Pinch-off bias

Set up the circuit below. Use the LabView program c:\Phy440\NewJFET.vi to measure the drain current I_D as a function of the Gate-Source voltage V_{GS}. Instructions on wire connections between the protoboard and the LabView circuitry can be found by following the selections within the program: File → VI Properties. Open the window "Documentation." Remember that the variable gate voltage is negative and you should keep it within the range of –5V to 0V.

You should find that the drain current decreases with increasingly negative gate voltage until a point where it is essentially zero. This is the so-called pinch-off voltage. (a) Compare your answer for the pinch-off voltage with the rather liberal limits given on the data page for "Gate-Source Cutoff Voltage". [3 p]

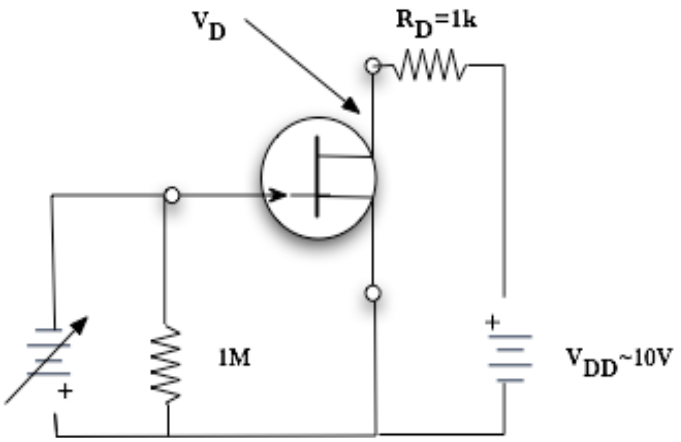

Figure 1: FET Circuit.

2. Common-source transfer characteristics

The program measures the current by measuring the voltage drop across the 1kΩ drain resistor.

(a) Make a copy of the computer plot of drain current vs. gate-source voltage and paste it into your notebook. [3 p]

(b) Compare your plot to the one in the data sheet. Are the plots similar? Does your plot have the right curvature? [3 p]

(c) The plot should have the form:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where I_D is the drain current, V_{GS} is the gate-source voltage, and I_{DSS} is the drain current at V_{GS}=0 V. From your plot determine the parameters I_{DSS} and V_P. [3 p]

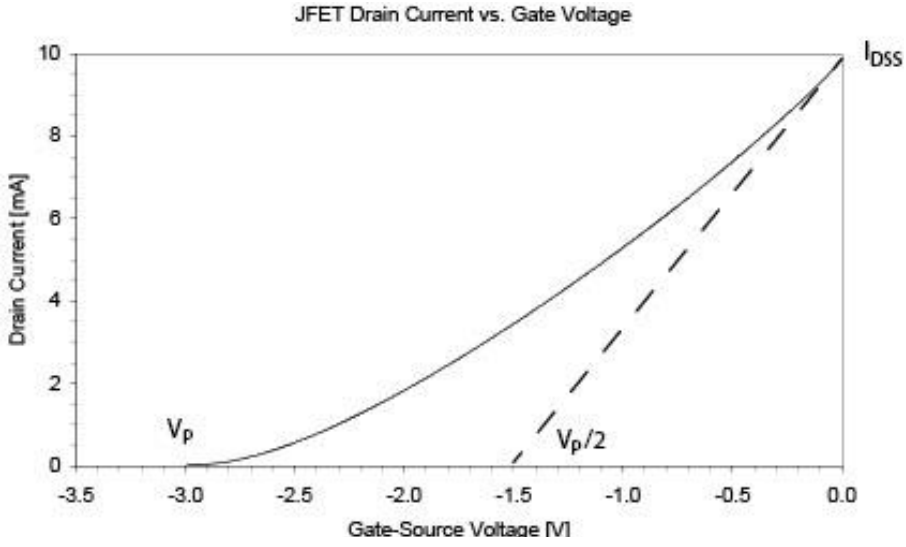

Figure 2: Drain Current vs. Gate Source Voltage.

3. Common-source JFET amplifier

Using the same transistor, build the circuit in Fig. 3 with a power supply for V_{DD} and a signal generator for the variable input voltages, as shown in Figure 3. For a good operating point, the drain voltage should be between 3 V and 7 V. Measure the quiescent drain voltage for your circuit. (The AC signal on the input is not relevant for quiescent conditions and may be disconnected for this part.) If your V_D is outside the above range, swap the resistor R_S from 1k to a different value, in order to get V_D within the desired range.

(a) What is your final V_D? What is your quiescent drain current now? [3 p]

Recommend signal voltage of 250 mV peak to peak

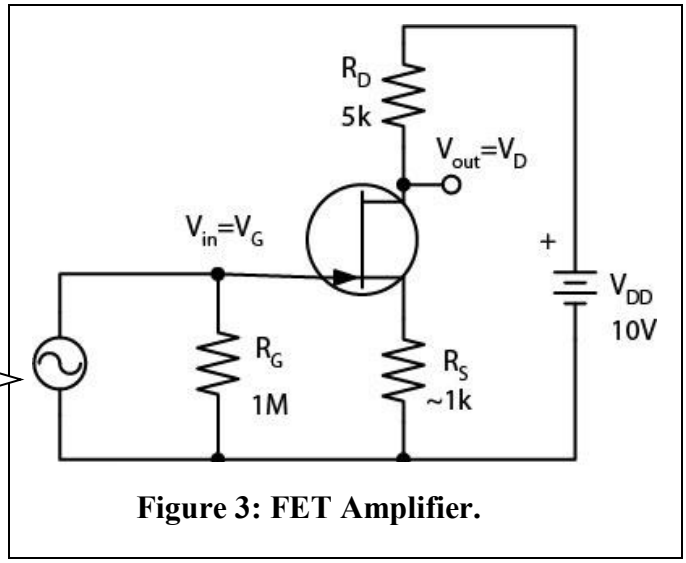

Figure 3: FET Amplifier.

The circuit above is an AC amplifier. The output signal at the drain will be larger than the input signal on the gate.

(b)*Explain why this is an inverting amplifier. [3 p]

(c) The gain of the amplifier depends upon the transconductance g_m. From your earlier measurements determine the value of $g_m = \Delta I_D/\Delta V_{GS}$ at your operating point. The units of this parameter are mhos (reciprocal ohms) or siemens (S). [3 p]

(d) *The gain is defined as $A_V = \Delta V_{out}/\Delta V_{in}$

Show that: $$A_V = -\frac{g_m R_D}{1 + g_m R_S}$$

and therefore that you expect a gain of about 2.5, if $g_m = 1\text{x}10^{-3}$ mhos, R_D=5kΩ and R_S=1kΩ. [3 p]

(e) Measure the gain of your amplifier circuit and compare with the expectation. Can you confirm that the amplifier is inverting? [3 p]

Op Amps I

Build the circuits below using a TL082 dual op-amp chip. Each chip contains two amplifiers. Pin number 1 is probably indicated with a dimple on the chip case. You will need to use only one of those amplifiers within a chip in this lab. Remember to connect ±15 volt supplies to the chip. Make sure that the grounds indicated for the circuits combine your power supply ground (0V) with the generator and DPO grounds.

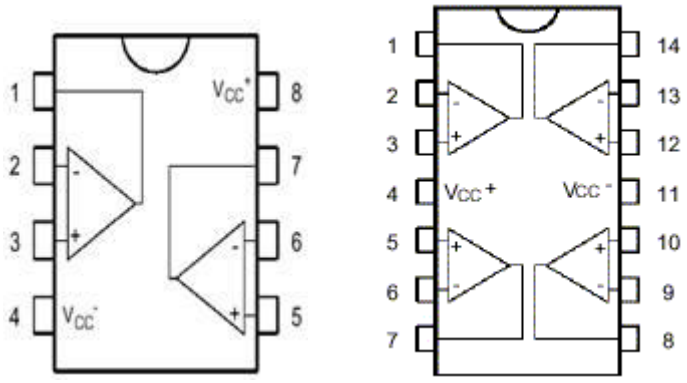

Figure 4: Pin-Out for TL082 and TL084 Chips.

4. The voltage follower

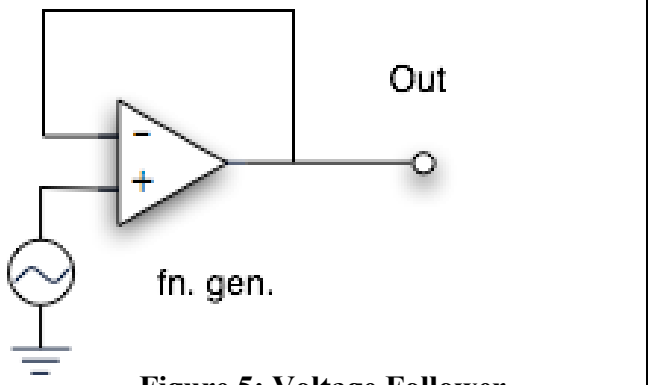

Figure 5: Voltage Follower.

(a) Use an oscilloscope to compare the input and output. Are they the same? Include a copy of the DPO output showing input and output wave forms. [4 p]
(b) Make the input at zero volts by grounding it. Use a DMM to discover whether the output is precisely zero volts. Possibly the output will be at a few millivolts. That represents an offset within the op amp. [3 p]

5. The non-inverting amp

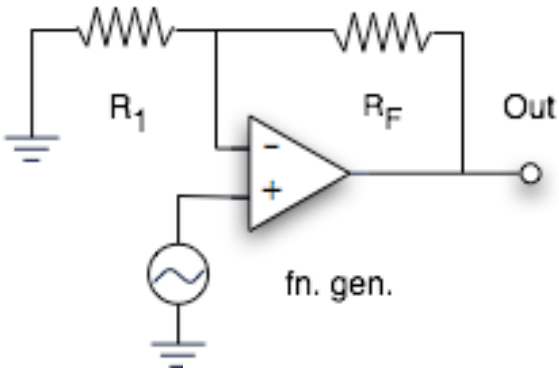

Figure 6: The non-inverting amp.

(a) *Show mathematically that you expect the gain to be given by $1+ R_F/R_1$. Measure the gain to verify this using resistor values in the range 3K to 200K. Paste a copy of an example DPO screen in your notebook. [4 p]

6. The inverting amp

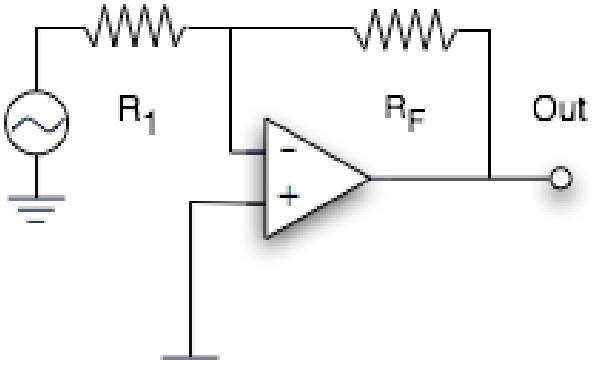

Figure 7: The inverting amp.

(a) *Show mathematically that you expect the gain to be given by $-R_F/R_1$. Measure the gain to verify this using resistor values in the range 3K to 200K. Place a copy of a screen output in your notebook. [4 p]

(b) Replace one of the fixed resistors by a trimmer potentiometer. Can you vary the gain of the amplifier using this control? [3 p]