Troubleshooting tips for the Xilinx FPGA labs

- Sometimes simply restarting the program or project will fix any error that occurred.
- The most common error is for the schematic symbol to not appear in the list even after the program says “schematic symbol successfully created”. Sometimes this clears up after restarting the project. Another strategy for fixing this is to open the “SYM” file directly. Sometimes Xilinx will then recognize it as a valid symbol. If a new project is not recognizing an older projects symbol (for example if the final project does not recognize the count to 5 symbol) then you may need to add the counter schematic to the current project. Just be sure Xilinx does not recognize the count 5 schematic as the primary schematic for the project.
- At the beginning of the second lab session, it is important to remember to check the settings for any newly created project. If the project settings are wrong, the program will not recognize the waveforms, e.g. clock and input signals, during the simulation. They will show up as “U” (undefined signals) in the data stream.