J. H. Greiner
C. J. Kircher
S. P. Klepner
S. K. Lahiri
A. J. Warnecke
S. Basavaiah
E. T. Yen
John M. Baker
P. R. Brosious
H.-C. W. Huang
M. Murakami
I. Ames

Fabrication Process for Josephson Integrated Circuits

A process for fabricating experimental Josephson integrated circuits is described that is based primarily on the use of vacuum-deposited Pb-alloy and SiO films patterned by photoresist stencil lift-off. The process has evolved from one previously reported, with changes having occurred in junction electrodes, tunnel barrier formation, layer patterning, device geometry, and minimum linewidths. Films of Pb-In(12 wt%)-Au(4 wt%) alloy (200–800 nm thick) are used for forming junction base electrodes, interferometer controls, and interconnection lines. Tunnel barriers are formed on the base electrode films by thermal oxidation and subsequent sputter-etching in an rf-oxygen plasma. Junction counter electrodes are formed from 400-nm-thick Pb-Bi(29 wt%) alloy films. Ground planes are formed from 300-nm-thick Nb films patterned by subtractive etching and insulated in part by a Nb_2O_5 layer formed by liquid anodization. Films of the intermetallic compound $AuIn_2$ (30–43 nm thick) are used for forming terminating, load, and damping resistors. The SiO films are used for interlayer insulation, for defining junction areas in interferometers, and as protective coatings. Layer patterning is achieved mainly by means of photoresist lift-off stencils. By utilizing this process, experimental logic and memory circuits containing ≈100 interferometers with lines as small as 2.5 μm in width have been successfully fabricated.

Introduction

Josephson tunneling devices exhibit fast switching and low power dissipation [1], characteristics that make them attractive for future computer applications [2]. Work is in progress to explore the potential of circuits containing such devices. A process was developed that allowed several initial types of logic and memory circuits to be successfully fabricated [3]. Since that time, improvements have been made in the process, and other investigators have successfully made devices and circuits using adaptations of the process [4].

This paper describes the fabrication process used to prepare recent Josephson devices and circuits. The multilayer, integrated circuits were formed on oxidized Si substrates primarily through use of vacuum-deposited thin films. Superconducting layers were generally Pb alloys and insulation layers, SiO. These layers were patterned using photoresist stencil lift-off methods and optical lithography with minimum linewidths of 2.5 μm. An overview of the fabrication process is presented, and preparation and properties of the various layers are de-

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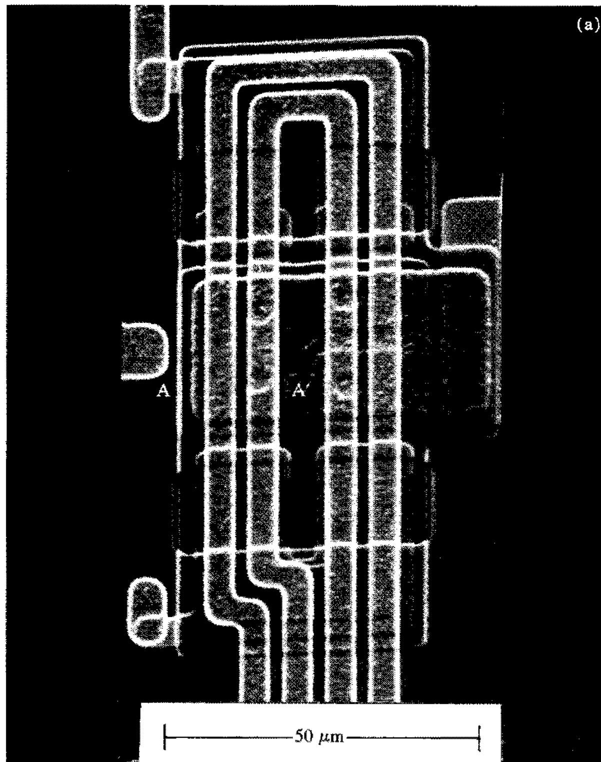

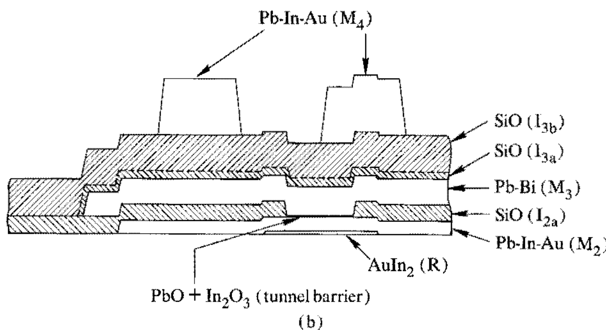

Figure 1 (a) Scanning electron micrograph (SEM) of a Josephson logic interferometer containing 2.5-μm-diameter junctions. (b) Associated schematic cross section through A—A′. The cross section illustrates most of the layers present.

scribed. In addition, some relevant characteristics of circuit elements are discussed and examples are given of experimental circuits that have been fabricated. Overviews of associated materials and process studies [5] and circuit studies [1] are contained in accompanying papers in this issue.

Circuit layers

A scanning electron micrograph (SEM) of a typical device, a logic interferometer, and its schematic cross section are shown in Fig. 1. Layers of Pb-In-Au (M_2) and Pb-Bi (M_3) are used to form the Josephson junction electrodes. The tunnel barrier is an oxide grown on M_2. The junction areas are defined by openings in an SiO (I_{2a}) layer. Damping resistors are formed from an $AuIn_2$ (R) layer that lies beneath the junctions. The control lines are formed from a Pb-In-Au (M_4) layer and are insulated from the underlying junction electrodes by SiO (I_{3a} + I_{3b}). The layers typically serve several functions in the circuits. For example, device interconnections are accomplished with the M_2 and M_4 layers, using the I_{3b} layer where insulated crossovers are required; load and terminating resistors are formed from the R layer; etc. For clarity, several layers have been omitted from the cross section: the interferometer lies above a superconducting Nb ground plane (M_1) that is covered by Nb_2O_5 (I_{1a}) and SiO (I_{1b}) insulation layers; an SiO (I_4) layer serves as an overlying protective layer. External connections are made to solder terminals [6] or contact pads through openings in the I_4 layer. Where ground-plane contacts are needed, they are established with a Pb-In-Au (C) layer. A typical integrated circuit thus utilizes ≈14 patterned thin-film layers. The various thin-film layers that have been used recently to fabricate logic and memory circuits are listed in Table 1, together with their thicknesses and functions. Several weeks are usually required to fabricate a typical circuit. Details of the fabrication steps are now presented.

- *Metal layers*

Lead-base materials were selected for forming junction electrodes because the transition temperatures and energy gaps of such materials are relatively insensitive to impurity levels and structure variations, and because, through their use, devices can be prepared with low junction capacitances [7] (the latter are important for high-speed circuits). Alloy additions to Pb were selected to improve its chemical and mechanical stability [8, 9]. Relevant electrical properties of the various metal layers are summarized in Table 2 for representative thicknesses. Included are ρ, the electrical resistivity at ≈300 K; ρ_0, the resistivity at 4.2 K (just above the superconducting transition temperature T_c); λ, the magnetic penetration depth at 4.2 K [10]; and Δ, the superconducting energy gap at 4.2 K. The compositions are as listed in Table 1. Niobium was selected for the ground plane because such films are stable, can be formed with a high T_c, and can be readily insulated by liquid anodization [11].

The depositions of the M_2, M_4, and R layers are preceded by an oxygen rf sputter-etch cleaning process in order to remove photoresist residues, improve adhesion, and form electrical contacts. These layers are deposited at pressures of ≈5 × 10^{-5} Pa onto substrates held at temperatures near 300 K through the use of water-cooled substrate holders and Ga backing.

Table 1 Layers for logic and memory circuits.

Layer	*Material*	*Thickness* (nm)	*Function*
M_1	Nb	300	Ground plane
I_{1a}	Nb_2O_5	25-35	Ground-plane insulation
I_{1b}	SiO	145-275	Ground-plane insulation
R	$AuIn_2$	30-43	Terminating, loading, and damping resistors
I_{1c}	SiO	200	Logic interferometer isolation and resistor insulation
C	Pb-In-Au*	300	Ground-plane contacts and logic interferometer inductance
M_2	Pb-In-Au*	200	Base electrodes, interconnections, and resistor contacts
I_{2a}	SiO	275	Junction definition and insulation
I_{2b}	SiO	275	Memory interferometer inductance and insulation
I_{2c}	PbO/In_2O_3	6.5	Tunneling barriers
M_3	Pb-Bi†	400	Counter electrodes
I_{3a}	SiO	100	Counter-electrode protection layer
I_{3b}	SiO	500	Controls and interconnection insulation
M_4	Pb-In-Au*	800	Controls, interconnection, and contacts to R, C, and M_2 layers
I_4	SiO	2000	Protective layer

*12 wt% In and 4 wt% Au.
†29 wt% Bi.

Table 2 Metal and insulation layer properties.

Metal layers	*Thickness* (nm)	ρ ($\mu\Omega$-cm)	ρ_0 ($\mu\Omega$-cm)	T_c (K)	λ (nm)	Δ (meV)
M_1	235	21	6.3	8.8	85	
Pb	500	21	0.014	7.2	49	
M_2	180	26	7.3	6.8	137	1.15
M_3	400	53	27	8.3	202	1.7
M_4	900	24	6.5	7.0	156	
R	43	12	4.0	0.2	—	
Insulation layers	ϵ_r	E_B (V/cm)	ρ (Ω-cm)			
Nb_2O_5	29	$\gtrsim 10^6$	4×10^6			
SiO	5.7	$\gtrsim 10^6$	10^{11}			

The Nb ground-plane layer (M_1) is deposited by rf sputtering in an Ar glow discharge. The substrate support is held at 400°C during deposition (the wafers reach ≥500°C) to obtain fine-grained polycrystalline films with low intrinsic stresses. It was necessary to use a small negative substrate bias (75 V) during deposition to obtain films of sufficient purity to have good superconducting properties [12]. Typical values for Nb film properties are given in Table 2.

The base-electrode layer (M_2) is formed by sequentially depositing films of Au (4.5 nm), Pb (160 nm), and In (35 nm) [9]. The three films readily interdiffuse (<1 h at 300 K), forming a two-phase alloy consisting of a Pb-In(13 at%) solid solution with ≈30-nm-size particles of the intermetallic compound $AuIn_2$. Auger spectroscopy and sputter-etch profile analysis of the M_2 layers show the first evidence of Au ≈30 nm below the M_2 surface [13]. A two-step, thermally grown In_2O_3 layer (≈2.5 nm) is formed on the layer at 2.7 Pa O_2 first at 24° and then at 75°C prior to its removal from the vacuum system [14]. This oxide provides chemical protection during subsequent photoprocessing and a more reproducible surface for subsequent tunnel barrier formation.

The Pb-Bi(29 wt%) counter-electrode layer (M_3) is deposited *in situ* after tunnel barrier formation by means of co-evaporation from an alloy source of the same composition. Films thus formed are a single phase (ε) of Pb-Bi having a higher T_c and a larger λ than pure Pb films [10, 15]. Through their use, improved junction cyclability and reduced subgap current levels have been obtained

[15]. However, the Pb-Bi films are susceptible to corrosion during photoprocessing and storage. Thus, a protective 100-nm layer of SiO is deposited onto them prior to stencil lift-off [16].

The control and interconnection layer (M_4) has the same composition as the base-electrode layer. In addition to its use for forming device controls, it serves as the primary layer from which interconnection lines are formed. Its thickness is 800 nm to ensure coverage over the edges of underlying layers and line continuity for relatively long lengths of 2.5-μm-wide lines [17]. The layer is formed by sequentially depositing films of Pb (250 nm), Au (18 nm), Pb (390 nm), and In (142 nm). Use of this deposition sequence has given good edge coverage without a significant reduction of the critical currents of lines formed from that layer [18].

The resistor layer (R) is formed by sequentially depositing films of Au and In. The films interdiffuse to form $AuIn_2$ layers 30 to 43 nm thick with sheet resistivities of 2 to 1 $\Omega/\square$, respectively. Deposition and annealing are carried out at a substrate temperature of 75°C to form stable layers. Interdiffusion is avoided at R-M_2 or R-M_4 interfaces because $AuIn_2$ is a phase of the M_2 and M_4 alloys [19]. The resistivity of $AuIn_2$ layers is believed to be determined primarily by grain-boundary scattering [20]. Thus, the control of factors influencing the thickness and grain size (*e.g.*, substrate cleaning, substrate temperature, layer composition, and deposition rates) is important in order to obtain reproducible sheet resistivities.

The ground-plane contact layer (C) is used primarily for forming superconducting contacts to the Nb ground plane. It is 300 nm thick and has the same composition as the base-electrode layer; it is formed by using the same deposition sequence. Prior to deposition, an rf Ar plasma is used to sputter-clean the Nb in order to ensure formation of contacts with adequate current-carrying capability. This layer is also used in logic interferometers to increase loop inductance and to ensure base-electrode continuity across I_{1c} edges [21] and ground-plane openings.

- *Insulating layers*

The low voltage levels and the superconductivity of the signal lines used for Josephson integrated circuits allow the use of thin-film insulators with relatively low values of breakdown voltage ($\geq$1 V) and resistivity ($\rho_0 \geq 10^6\ \Omega$-cm). Both the Nb_2O_5 and SiO layers allow substantial current flow at electric fields that are small compared to the breakdown field. Thus, they should be relatively unsusceptible to breakdown due to static charge buildup. Table 2 also gives, for Nb_2O_5 [10] and SiO [22] layers, their relative dielectric constants ϵ_r at 4.2 K, the typical breakdown fields E_B at 300 K, and their resistivities ρ at 300 K and at low biases, where conduction through the layers is ohmic. Both materials are amorphous (*i.e.* noncrystalline) when prepared as described here.

Insulation of the Nb ground plane is achieved by using a Nb_2O_5 layer (I_{1a}) formed by liquid anodization of the Nb film. The anodization is carried out at 20°C in an electrolyte of ammonium pentaborate, ethylene glycol, and H_2O [11]. The thickness of the Nb_2O_5 layer thus formed is determined by the anodization voltage used (2.2 nm/V). Although Nb_2O_5 has excellent insulating properties for Josephson circuit applications, only thin layers are used because the high dielectric constant of the material would cause reduction of the line characteristic impedance levels and an increase in propagation delays. Thus, for use in circuits, the Nb_2O_5 is usually covered with a thicker layer of SiO, the composite serving as the ground-plane insulation. Use of such a composite insulator results in fewer ground-plane insulation shorts.

The SiO layers are deposited in a vacuum of $\approx 5 \times 10^{-5}$ Pa by using a heated source (either rf or resistance). Deposition is carried out at a substrate temperature of $\approx$300 K, with Ga backing and a deposition rate of $\approx$1 nm/s. The resulting SiO films are reported to have low stress levels ($\approx 2 \times 10^7$ Pa) upon deposition [23], thus minimizing the stress to which the Pb-alloy films are subjected. Analysis of evaporated SiO films by nuclear backscattering shows that they have an Si:O atom ratio of approximately 1 $\pm$ 2% [24]. Electron spectroscopy for chemical analysis (ESCA) indicates that such SiO films are a single phase (*i.e.*, not a two-phase mixture of Si and SiO_2) and that they are relatively stable up to temperatures of $\approx$400°C [25].

- *Tunnel barrier*

The formation of the tunnel barrier is the key step in Josephson device fabrication. The Josephson current and the single-electron tunneling current depend exponentially on the product of the tunneling barrier thickness and the square root of the barrier height times the effective mass of tunneling electrons. Basavaiah *et al.* have confirmed such a dependence for Pb/PbO/Pb junctions [26]. Thus, precise control of the tunnel barrier oxide thickness and composition are required in order to achieve reproducible values of the tunneling current. For Pb-alloy junctions, a method of achieving this reproducibly has been developed; oxide tunnel barriers are formed on the base-electrode layer by sputter-etching its surface in a low-pressure rf oxygen discharge [27] (rf oxidation). See also the accompanying paper by R. F. Broom *et al.* [4(e)]. In the discharge, two competing processes occur that can be used to control the oxide thickness: oxide

growth and sputter-etching. As for thermal oxidation, the oxide growth rate decreases rapidly with oxide thickness, favoring formation of uniform oxide layers. In the competing process (sputter-etching) the oxide removal rate is independent of thickness. In the ideal case, these processes can be balanced so that the oxide thickness becomes independent of rf oxidation time and depends only upon the discharge conditions, *e.g.*, oxygen pressure and rf voltage. In practice, such behavior has been achieved for the rf oxidation of Pb films [27] and approached for Pb-In-Au alloy films [28]. The properties of oxides formed on the latter alloy films by rf oxidation are also found to depend on alloy composition, oxide growth kinetics, and backscattering of material sputtered from the surrounding regions of the rf electrode and sample surfaces [4(e), 14]. Nevertheless, the current densities of junctions made with Pb-In-Au base electrodes can be controlled on a fine scale by adjusting the rf discharge parameters. In addition, good-quality Josephson junctions can be made that cover the current density range of interest for logic and memory devices in a manner compatible with the fabrication of integrated circuits.

Tunnel barriers are formed on the Pb-In-Au M_2 layers by using a combination of thermal and rf oxidation. The thermal oxidation to form an In_2O_3 layer is carried out before the samples are removed from the M_2 deposition system at 2.7 Pa of O_2 for 30 min each at 24° and 75°C [14]. The processing steps required to prepare the I_{2a} layer defining the area of most of the junctions and the M_3 photoresist stencil are carried out next. The tunnel barrier oxide is completed by rf oxidizing regions of the M_2 surface exposed in the openings in these two layers. For rf oxidation, the substrates are mounted (Ga backing) onto a water-cooled rf electrode coated with Pb-Bi. Before rf oxidation, the vacuum system is exposed to an oxgyen discharge cleaning step with the samples shuttered. The first stage of the rf oxidation is carried out at 125 V (all rf voltages are peak-to-peak) and 10 Pa. This step has been found to remove residues from the preceding photoresist stencil formation step without significantly altering the previously formed In_2O_3 layer. The second stage of rf oxidation is carried out at 360 V under an oxygen pressure appropriate to complete formation of the tunnel barrier oxide (discussed later). Without breaking vacuum, the Pb-Bi counter-electrode layer is deposited at $\approx 5 \times 10^{-5}$ Pa. The resulting tunnel barrier oxide is composed of In_2O_3 and several forms of Pb oxide [14].

Layer patterning

The patterning processes reported here have been practiced primarily on 25-mm-diameter Si wafers that are subsequently sectioned into four $6.35 \times 6.35\text{-mm}^2$ chips. As already indicated, lift-off stencils are used for patterning the Pb-alloy, $AuIn_2$, and SiO layers; the Nb and Nb_2O_5 layers are patterned using photoresist masks and subtractive etching and anodizing, respectively.

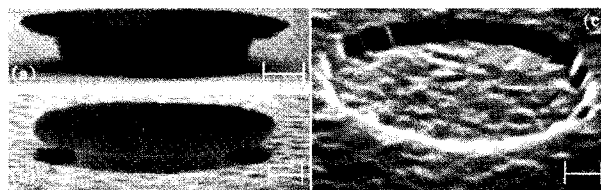

Figure 2 SEMs depicting junction area definition obtained by means of the photoresist stencil lift-off process. (a) A stencil prepared over the M_2 layer and prior to SiO deposition. (b) The stencil after deposition of 275 nm of SiO. (c) The completed SiO opening through which a tunnel barrier is to be formed. Size bars represent 0.5 μm.

Several types of photoresist stencils have been used [29, 30]; that used at present is formed by a single photoresist layer treated by immersion in chlorobenzene [31]. The upper surface of the photoresist is modified such that the development rate for the lower portion is relatively rapid. Using projection exposure, this results in the desired resist edge profile overhang of up to ≈ 0.5 μm. A stencil thickness of approximately 800 nm is used for the layers ≤ 500 nm thick. For the M_4 and I_4 layers, a stencil about twice as thick is used. Many factors, such as photoresist adhesion, substrate reflectivity, stencil sputtering in the rf discharge, and SiO scattering, influence the effectiveness of the stencil process. For example, to overcome photoresist adhesion problems, hexamethyldisilazane (HMDS) [32] is used prior to photoresist application and a layer of $TiO_x \approx 1$ nm thick is deposited on underlying SiO surfaces [18]; to ensure stencil lift-off after layer deposition, the stencil profile is formed in a manner adequate for use over the least reflective material (SiO). Also, the stencil overhang is sufficient to withstand the sputtering during rf discharge cleaning prior to deposition of the M_2, M_4, C, and R layers. Scattering of SiO beneath the stencil overhang during deposition affects SiO lift-off and junction area definition. The actual junction areas are defined at the interface between the photoresist and the base electrode [30]. Near-normal incidence of the SiO evaporant onto substrates is necessary for well-defined SiO film edges. Figures 2(a–c) show scanning electron micrographs (SEMs) of the junction area definition achieved by means of the photoresist stencil lift-off process.

Usually, a layer-to-layer registration of 2.5 μm is used to ensure SiO insulation coverage at metal layer edges and to reduce the possibility of coincident layer edges that might affect pattern definition. However, in some in-

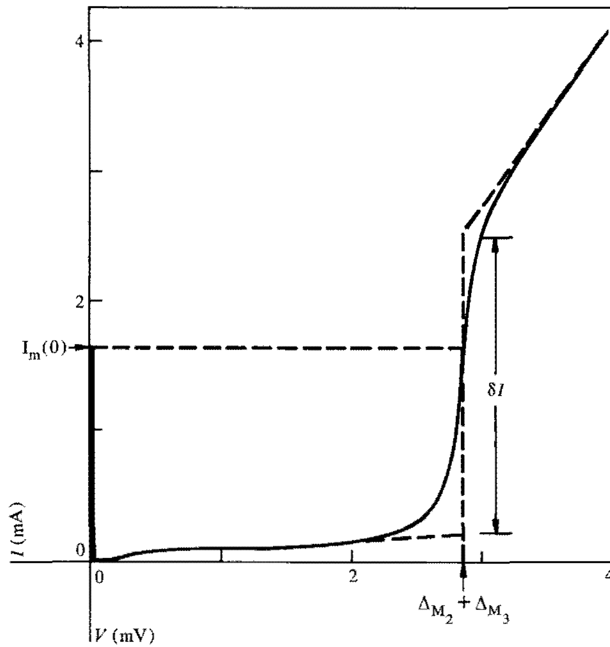

Figure 3 *I-V* characteristic of a logic interferometer similar to that shown in Fig. 1.

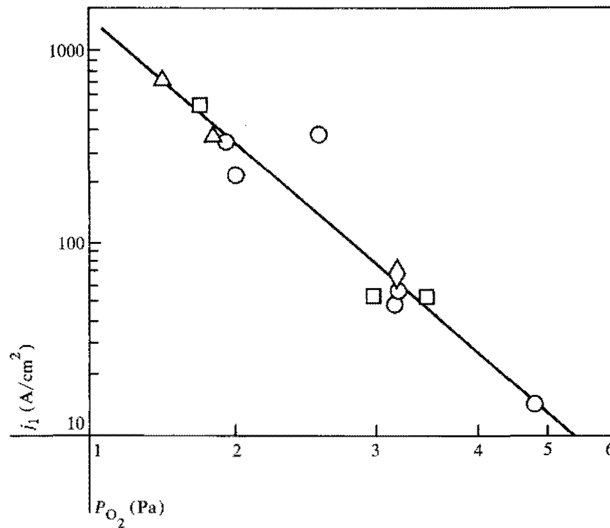

Figure 4 Dependence of junction current density on oxygen pressure used during the second stage of rf oxidation. Different symbols are used to distinguish junctions fabricated with base electrodes from different base-electrode deposition runs.

stances, in order to increase circuit density, a registration of 1.25 μm is used [33]. In addition, occasional use is made of layers having coincident edges; the effects of such edges on pattern definition are negligible provided the layers are relatively thin.

Characterization of circuit layers and circuit elements

The layers and circuit elements for a particular circuit experiment are characterized by using separate samples that are fabricated with the circuit samples and/or by incorporating test sites onto the circuit samples. The metal layers are characterized by measuring their electrical resistivity and (for the superconducting films) by measuring the critical current of a short line segment. The SiO and Nb_2O_5 insulating layers are evaluated using capacitor structures. For devices, the single-particle-tunneling current-voltage (*I-V*) characteristics are measured at 4.2 K. The various types of superconducting contacts are characterized by their critical current levels at 4.2 K. Other aspects, such as pattern definition and SiO step coverage by metal layers, are evaluated by test sites designed for electrical measurement and inspected by optical and/or scanning electron microscopy. The superconducting properties of the elements can in some cases be used to advantage in characterizing the behavior of large populations of similar elements, as are needed for circuits. For example, the distribution in Josephson threshold current levels can be obtained from a four-terminal measurement of a series-connected string of many devices [4, 34]; the spatial distribution can be obtained by using matrix selection of individual junctions in a large array [34]. The quality of the electrical contacts and of the step coverage by superconducting lines can be judged by comparing the critical currents of lines containing many contacts or steps with those of planar segments of similar lines. (See later discussion.)

- *Junctions and gates*

A quasistatic *I-V* characteristic for a typical logic interferometer having four 2.5-μm-diameter junctions is shown in Fig. 3. Circuit-design-related parameters, such as the Josephson current $I_m(0)$, the current density j_1, and the energy gap $\Delta_{M_2} + \Delta_{M_3}$, are determined from the *I-V* characteristics. The value of j_1 is determined from the relationship $j_1A = k\delta I$, where δI is the current jump at $\Delta_{M_2} + \Delta_{M_3}$, A is the junction area, and k is a constant that depends on the electrode materials ($\approx$0.7 for our junctions). The Josephson current $I_m(0)$ is related to j_1; for the interferometer junctions typically used for circuit designs, the Josephson current is uniformly distributed over the junction area and $I_m(0) = j_1A$.

Junctions having a desired j_1 are obtained by adjusting the oxygen pressure P_{O_2} used for the second stage of the rf oxidation portion of the tunnel-barrier formation process. The dependence of j_1 on P_{O_2} is shown in Fig. 4. Each data point gives the average current density for a group of 19 junctions on the same substrate. Each group was fabricated separately and measured after counter-electrode layer formation. Different symbols are used for junctions

fabricated with base electrodes from different deposition runs. It is evident from Fig. 4 that a wide range of j_1 values are obtainable with good control by an appropriate choice of P_{O_2}.

The j_1 values increase when junctions are annealed. The magnitude of the increase is sensitive to both the oxidation conditions used to form the tunnel barrier and the time and temperature of annealing. An increase in j_1 by a factor of 2-10 can be obtained after M_3 layer formation by annealing at 70°C for a period of 90 min. (Such annealing is equivalent to the cumulative heat treatment that the junctions experience during the subsequent fabrication of the I_{3b}, M_4, and I_4 layers). The j_1 changes observed for completed circuits are small at room temperature and can be arrested by using appropriate storage conditions [35].

The following procedure is used to achieve the $I_m(0)$ values desired for circuits. Interferometer test structures are fabricated that are similar to those on the circuits and that have been fabricated with the circuits up to formation of the M_3 stencil. A trial I_{2c}-M_3-I_{3a} run is then carried out using only the test interferometers. The thermal effects associated with formation of the I_{3b}, M_4, and I_4 layers are then simulated by annealing the interferometers at 70°C for 90 min. Using the j_1 value obtained from the trial run, the P_{O_2} value to be used for rf oxidation of the circuit samples is adjusted as needed to achieve the desired $I_m(0)$ value. This procedure reduces the effects of both short- and long-term run-to-run variations that can occur in base-electrode-layer formation, in instrumentation for measuring plasma parameters, in junction area, etc. By using this procedure, the run-to-run variations in j_1 for completed circuits can be made comparable to those shown for the junction data in Fig. 4.

The variation in $I_m(0)$ values across a chip has been measured [34] for several chips populated with an array of 784 individually measurable three-junction interferometers containing junctions having nominal diameters of 5, 7, and 5 μm, respectively. The distribution for a chip is shown in Fig. 5(a). The $I_m(0)$ distribution is nearly Gaussian [filled circles in Fig. 5(b)]; the data fall on a straight line when plotted using a cumulative normal distribution ordinate. The standard deviation σ is 7%. However, $I_m(0)$ varies systematically with the position of the junctions on the chip. (This variation is observed to correlate with the position the junctions occupied along the rf electrode radius during rf oxidation and in practice can be reduced by rotating the samples on the rf electrode during tunnel-barrier formation [36].) If this systematic component is removed from the data [open circles in Fig. 5(b)], the adjusted standard deviation σ' is 4%. The contributions to the $I_m(0)$ distributions of variations in j_1 and junction area

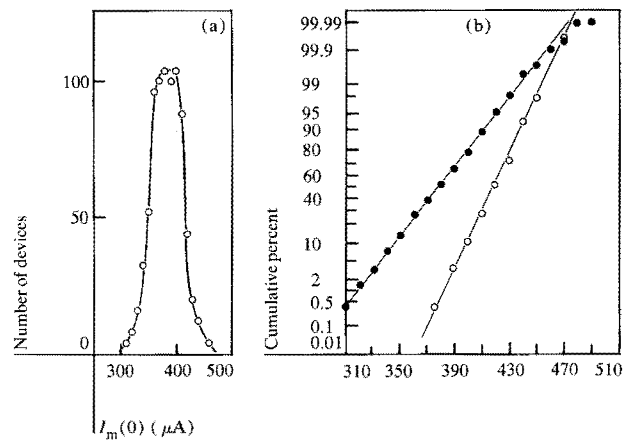

Figure 5 (a) The distribution of $I_m(0)$ having σ = 7% for a chip containing 784 three-junction interferometers. (b) The same distribution of $I_m(0)$ plotted using a cumulative normal distribution ordinate (●). Also included is the distribution after a systematic component has been removed from the data (○), where σ' = 4%.

were found from separate experiments to be comparable for 5-μm-diameter junctions and consistent with the σ' = 4% obtained for the data shown in Fig. 5(b).

• *Contacts*

The M_2, M_4, and C layers have nominally identical compositions, and interconnections between them are readily made. For example, M_2-M_4 contacts are used for forming x- and y-line connections, and C-M_4 contacts are used (in conjunction with M_1-C contacts) to form ground-plane contacts. These contacts are superconducting with a high critical current in the presence of a thin oxide layer between them, due in part to the presence of In in both electrodes [37]. This oxide layer results from the rf oxygen discharge utilized prior to deposition of the M_2 and M_4 layers for cleaning the surfaces exposed in the stencil used for patterning those layers. The discharge does not cause any significant alteration of the exposed SiO or Nb_2O_5 insulation layers. The oxide also prevents interdiffusion of the layers at the contacts during the sequential film deposition used to form the M_4 layer. The current level I_c at which such contacts become nonsuperconducting increases with contact width. For 2.5 × 2.5-μm^2 M_2-M_4 contacts $I_c \approx$ 8 mA. As indicated previously, the contacts can be characterized using series-connected contact strings; *e.g.*, for a string of 900 M_2-M_4 contacts, 7 × 7 μm^2, $I_c \approx$ 35 mA, as shown in Fig. 6. For comparison, I_c values of 7-μm-wide, 2.5-mm-long M_2 and M_4 lines are ≈45 and 150 mA, respectively; and for a 7-μm-wide, 20-mm-long M_4 line that crosses 1000 I_{3b} steps, it is ≈90 mA.

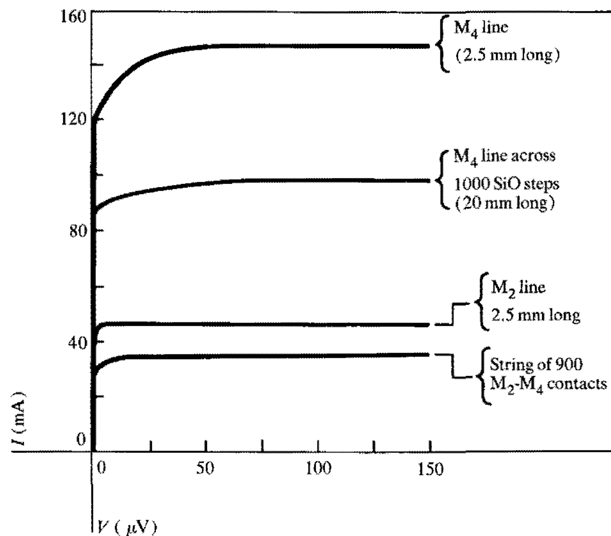

Figure 6 *I-V* characteristics of typical lines (7 μm wide) and a series-connected string of superconducting contacts.

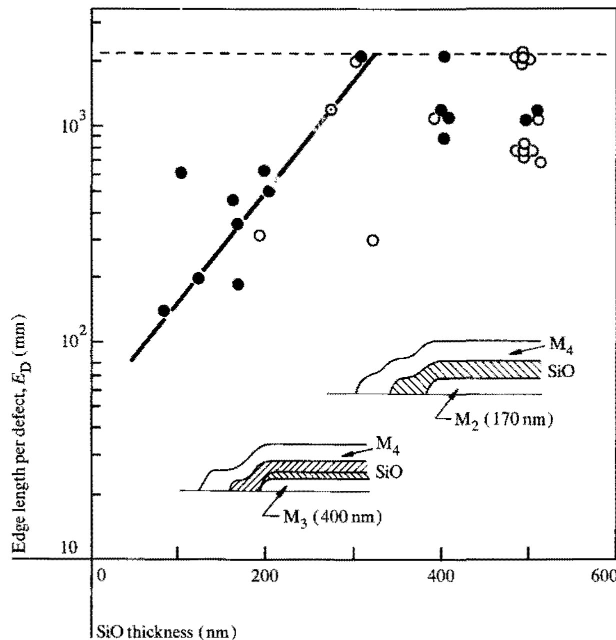

Figure 7 Edge length per insulator defect *versus* SiO thickness for $M_2/I_{3b}/M_4$ (●) and M_3/I_{3a} + I_{3b}/M_4 (○) crossings. The dashed line gives the total testable edge length per wafer. The insets show cross sections of structure edges.

Superconducting contacts to the Nb ground plane are made by using an rf Ar plasma to remove surface oxide followed by *in situ* deposition of the C layer. Sputter-etching parameters (360 V at 1.3 Pa of Ar for 15 min) are chosen to minimize photoresist polymerization (which affects stencil lift-off). For the M_1-C contacts, $I_c \approx 50$ mA for 8 × 13-μm^2 contacts.

Superconducting contacts to the M_3 layer are formed with the M_2 layer, *i.e.*, by forming Josephson junctions. This procedure allows low-resistance contacts to be formed without incurring interdiffusion of the M_2 and M_3 layers. The area of such "contact junctions" is chosen so that the $I_m(0)$ level is not exceeded in normal circuit operation.

- *Resistors*

Resistors of a desired value are obtained by choosing the geometry and sheet resistances at 4.2 K R_{so} of the $AuIn_2$ films. Values of R_{so} in the range of 0.1–4 Ω/□ can be obtained conveniently by using an appropriate $AuIn_2$ film thickness d, since in this range $R_{so} \approx d^{-1.8}$. See the accompanying paper by Kircher and Lahiri for details [20]. For circuit fabrication, a procedure has been adopted in which a "trial" resistor deposition is carried out immediately prior to that used for circuit fabrication. On the basis of the R_{so} obtained for the trial film, d is chosen for the circuit resistor deposition to be subsequently used for circuit samples. The ratios of the actual-to-target R_{so} values obtained using this procedure for a sequential series of 12 circuit fabrication runs varied from 0.8 to 1.25, with most falling between 0.96 and 1.1. The run-to-run variation of resistor values in circuits was somewhat larger than this, reflecting the added influences of other variables, *e.g.*, geometry, contact resistance, and R_{so} uniformity.

Contacts to the resistors are achieved with the M_2 or M_4 layers by following the previously described oxygen rf discharge stencil cleaning procedure; the contact resistances are typically ≈0.15 Ω for each 7 × 7-μm^2 contact. Lahiri has shown that such resistors are sufficiently stable during subsequent storage and annealing [19].

- *Lines*

The I_c levels of the superconducting M_2, M_3, M_4, and C lines vary linearly with linewidth for lines prepared over a superconducting ground plane. For linewidths of 2.5–40 μm, $I_c \approx 10$ mA/μm for the M_2, M_3, and C lines, and 20 mA/μm for the M_4 lines. A reduction in I_c can occur for long lengths of line because of line defects and/or inadequate edge coverage where lines cross the edges of underlying layers. For example, a line defect level of ≈1200 mm per defect was found in one experiment using a group of ≈500 test sites, each having 72 mm of 3.8-μm-wide M_4 lines [17].

- *Insulated crossing*

Insulating SiO layers can be prepared with low electrical defect densities. Using a 5-V test, SiO area per defect values typically obtained for unpatterned Pb-alloy films coated with unpatterned SiO films having thicknesses of

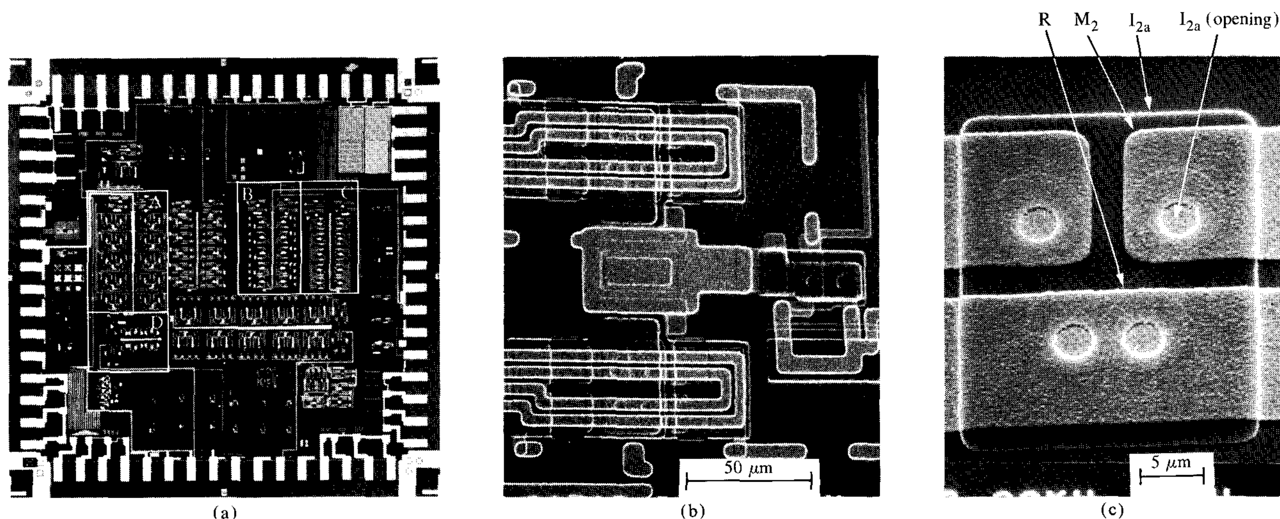

Figure 8 (a) Chip containing experimental current injection logic devices and circuits. Ten-stage chains of four-input AND circuits (A), four-input OR circuits (B), two-input AND circuits (C), and two-input OR circuits (D). (b) SEM of a portion of C showing two interconnected interferometers and a two-junction current injection gate (right, center). (c) SEM of the center portion of one interferometer after formation of its I_{2a} layer; ≈2.5-μm-diameter junction openings.

100–600 nm were >20 mm². The area per defect was smaller when patterned SiO and Pb-alloy films were used; however, these defect densities are adequate for coverage of ≈1 mm², the estimated active SiO area of a 6.35 × 6.35-mm² chip.

Insulation of metal edges by SiO is most demanding for x- and y-interconnection line crossings (M_2/SiO/M_4) and for device crossings (M_3/SiO/M_4). The insulation defect levels at M_2 and M_3 edges in such structures were estimated by comparing the defect levels obtained for two types of capacitor test sites that were interspersed on the same wafer. The test sites had the same active SiO area but had lengths of insulated M_2 or M_3 edge that differed by more than a factor of 10^3. Edge length per insulator defect levels E_D determined in this manner using a 5-V test are shown in Fig. 7. Each data point gives the E_D value obtained for a group of test sites on a single wafer having a total testable edge length of ≈2200 mm per wafer (dashed line). For wafers having one or no edge defects, E_D values are plotted on the dashed line. Typically, E_D > 500 mm for both M_2 and M_3 edges at SiO thicknesses ≥ 400 nm.

Devices and circuits

A photograph of a chip containing several experimental devices and circuits that were used to investigate the logic delay for current injection logic [38] is shown in Fig. 8(a). The 6.35 × 6.35-mm² chip has 64 peripheral contact pads and includes AND and OR circuit chains of logic interferometers. Illustratively, a ten-stage AND circuit chain containing about 75 interconnected interferometers is in region A; a ten-stage OR circuit chain containing about 25 interconnected interferometers is in Region B. Two such interconnected interferometers, which form a portion of the AND circuit chain in region C of Fig. 8(a), are shown in Fig. 8(b). The interferometers are identical to the one shown in Fig. 1; they contain four junctions of equal area (≈2.5-μm diameter) with underlying damping resistors (not visible) and overlying ≈2.5-μm-wide control line loops. They are connected to the ground plane at a central M_1-C-M_4 contact. The region shown in Fig. 8(b) contains a total of about 15 resistors (not visible). The center portion of a partially completed interferometer is shown in Fig. 8(c). The damping resistors, base electrode, and I_{2a} openings that define the junction areas are indicated. Measurements of the average logic delay obtained from the two-input AND and OR chains were 26 and 13 ps, respectively [38].

An experimental low-flux-quantum Josephson nondestructive read out (NDRO) memory cell [33] is shown in Fig. 9. The memory cell, 58 × 48 μm² in size, contains a write gate (a three-junction interferometer), a sense gate (a two-junction interferometer), lines (M_2 and M_4) for cell interconnections, a contact junction (M_2-M_3), contacts (M_2-M_4), and a damping resistor (not visible) between the write gate and contact junction. The cell design contains 2.5-μm linewidths and line spacings, and a layer-to-layer registration of 1.25 μm. Additionally, the design includes coincident edges between some overlying or adjacent lay-

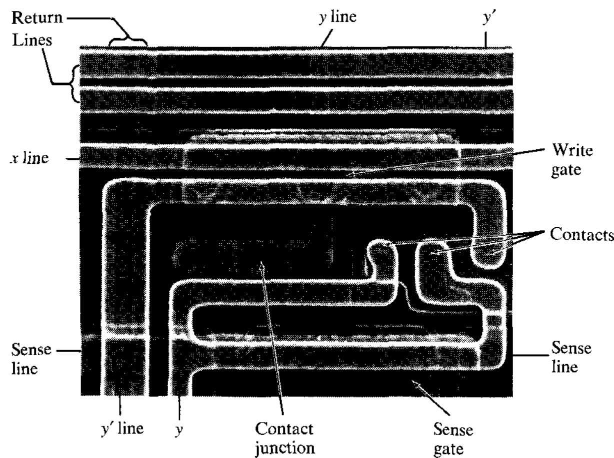

Figure 9 SEM of an experimental low-flux-quantum Josephson NDRO memory cell. The x- and y-interconnection lines are $\approx$2.5 μm wide.

ers. Such cells have been fabricated and operated successfully with a stored energy of only $\approx 6 \times 10^{-2}$ J. They are electrically attractive as the basis for a high-speed cache memory array [33].

Concluding remarks

Additional advances have been made in the previously described process for fabricating experimental Josephson circuits [3]. The process has been extended to the 2.5-μm-linewidth and junction-diameter levels. The circuits now utilize interferometers as active elements. Logic and memory circuits containing up to 14 layers and about 100 interferometers have been successfully fabricated [38, 39]. The circuits also contain lines, contacts and transformers, insulated crossings and capacitors, resistors, and power regulators, which are formed in an integrated manner with the interferometers.

Associated circuit performance studies continue to indicate that Josephson circuits have potential for the fabrication of ultrafast computing systems [1, 2]. In order to realize this potential, further development of the process described here will be necessary. Additionally, larger collections of logic and memory circuits having acceptable circuit parameters must be successfully fabricated and must be capable of surviving subsequent packaging and use conditions, including repeated cycling to 4.2 K.

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References and notes

1. J. Matisoo, *IBM J. Res. Develop.* **24** (1980, this issue).
2. W. Anacker, *IBM J. Res. Develop.* **24** (1980, this issue).
3. J. H. Greiner, S. Basavaiah, and I. Ames, *J. Vac. Sci. Technol.* **11,** 81 (1974).
4. (a) See for example A. F. Hebard and R. H. Eick, *J. Appl. Phys.* **49,** 339 (1978); (b) R. F. Broom, P. Guéret, W. Kotyczka, Th. O. Mohr, A. Moser, A. Oosenbrug, and P. Wolf, *International Solid-State Circuits Conference (ISSC78) Digest* **40,** 60 (1978); (c) R. H. Havemann, C. A. Hamilton, and R. E. Harris, *J. Vac. Sci. Technol.* **15,** 392 (1978); (d) A. Ishida, K. Kuroda, T. Wahs, and H. Yamada, presented at the Solid State Devices Conference, Tokyo, Japan, August 1978; (e) R. F. Broom, R. Jaggi, Th. O. Mohr, and A. Oosenbrug, *IBM J. Res. Develop.* **24** (1980, this issue).
5. I. Ames, *IBM J. Res. Develop.* **24** (1980, this issue).
6. C. Kircher, K. Grebe, I. Ames, and W. Anacker, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished work; H. C. Jones, D. J. Herrell, and Y. L. Yao, *IEEE Trans. Magnetics* **MAG-15,** 432 (1979); P. Geldermans and C. Y. Ting, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
7. S. Basavaiah and J. H. Greiner, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
8. W. Anacker, K. Grebe, J. H. Greiner, S. K. Lahiri, K. C. Park, and H. Zappe, U.S. Patent 3,733,526, 1973; S. K. Lahiri, U.S. Patent 3,999,203, 1976.
9. S. K. Lahiri, *J. Vac. Sci. Technol.* **13,** 148 (1976) and cited references; S. K. Lahiri and S. Basavaiah, *J. Appl. Phys.* **49,** 2880 (1978).
10. W. H. Henkels and C. J. Kircher, *IEEE Trans. Magnetics* **MAG-13,** 637 (1977).
11. R. E. Joynson, C. A. Neugebauer, and J. R. Rairden, *J. Vac. Sci. Technol.* **4,** 171 (1967).
12. K. Grebe, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
13. J. M. Baker, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
14. J. M. Baker, C. J. Kircher, and J. W. Matthews, *IBM J. Res. Develop.* **24** (1980, this issue).
15. S. K. Lahiri, *IBM Tech. Disclosure Bull.* **21,** 3403 (1979); S. K. Lahiri, S. Basavaiah, and C. Kircher, *Appl. Phys. Lett.*, in press.
16. S. K. Lahiri, *IBM Tech. Disclosure Bull.* **22,** 3886 (1980).
17. S. Klepner, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
18. E. Yen, IBM General Products Division laboratory, San Jose, CA, unpublished results.
19. S. K. Lahiri, *Thin Solid Films* **41,** 209 (1977).
20. C. J. Kircher and S. K. Lahiri, *IBM J. Res. Develop.* **24** (1980, this issue).
21. L. M. Geppert, J. H. Greiner, D. J. Herrell, and S. Klepner, *IEEE Trans. Magnetics* **MAG-15,** 412 (1979).
22. S. Basavaiah and C. J. Kircher, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
23. A. E. Hill and G. R. Hoffman, *Brit. J. Appl. Phys.* **18,** 13 (1967); J. Priest and H. L. Caswell, *Transactions of the 8th National Vacuum Symposium*, Pergamon Press, Elmsford, NY, 1961, p. 47.
24. W. Hammer and C. J. Kircher, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
25. S. I. Raider and R. Flitsch, *J. Electrochem. Soc.* **123,** 1755 (1976).

26. S. Basavaiah, J. M. Eldridge, and J. Matisoo, *J. Appl. Phys.* **45**, 457 (1974); also contained in that paper is a review of applicable theoretical studies.
27. J. H. Greiner, *J. Appl. Phys.* **42**, 5151 (1971); **45**, 32 (1974).
28. J. H. Greiner and S. Basavaiah, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
29. K. Grebe, I. Ames, and A. Ginzberg, *J. Vac. Sci. Technol.* **11**, 458 (1974).
30. A. Warnecke, R. M. Patt, and C. J. Johnson, Jr., *Kodak Microelectronics Seminar Proceedings* (INTERFACE '77), Eastman Kodak Company, Rochester, NY, 1978, p. 145.
31. B. J. Canavello, M. Hatzakis, and J. M. Shaw, *IBM Tech. Disclosure Bull.* **19**, 4048 (1977); M. Hatzakis, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
32. Purchased from SCM Organic Chemicals Division, SCM Corporation, Gainesville, FL 32602.
33. W. H. Henkels and J. H. Greiner, *IEEE J. Solid-State Circuits* **SC-14**, 794 (1979).
34. S. Basavaiah, J. H. Greiner, H. H. Zappe, and S. J. Singer, *J. Appl. Phys.*, in press.
35. S. Basavaiah, K. R. Grebe, J. H. Greiner, S. K. Lahiri, and A. Scott, *IBM Tech. Disclosure Bull.* **17**, 3488 (1975); R. F. Broom, R. Jaggi, Th. O. Mohr, and A. Oosenbrug, IBM Zurich Research Laboratory, unpublished results.
36. P. Brosious, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished results.
37. W. Anacker, J. Greiner, and K. Grebe, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, unpublished work; I. Ames, U.S. Patent 3,852,795, 1974.
38. T. R. Gheewala, *Appl. Phys. Lett.* **33**, 781 (1978); **34**, 670 (1979).
39. W. H. Henkels, *J. Appl. Phys.* **50** (Dec. 1979).

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E. T. Yen is located at the IBM General Products Division laboratory, San Jose, California 95150; the other authors are at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598.