User Manual

DG645
Digital Delay Generator

Revision 1.1 (9/9/08)

Certification

Stanford Research Systems certifies that this product met its published specifications at the time of shipment.

Warranty

This Stanford Research Systems product is warranted against defects in materials and workmanship for a period of one (1) year from the date of shipment.

Service

For warranty service or repair, this product must be returned to a Stanford Research Systems authorized service facility. Contact Stanford Research Systems or an authorized representative before returning this product for repair.

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Contents

Safety and Preparation for Use

Line Voltage

The DG645 operates from a 90 to 132 VAC or 175 to 264 VAC power source having a line frequency between 47 and 63 Hz. Power consumption is less than 100 VA total. In standby mode, power is turned off to the main board. However, power is maintained at all times to any optional timebases installed. Thus, a unit with an optional rubidium or ovenized quartz oscillator is expected to consume less than 25 VA and 15 VA of power, respectively, in standby mode.

Power Entry Module

A power entry module, labeled AC POWER on the back panel of the DG645, provides connection to the power source and to a protective ground.

Power Cord

The DG645 package includes a detachable, three-wire power cord for connection to the power source and protective ground.

The exposed metal parts of the box are connected to the power ground to protect against electrical shock. Always use an outlet which has a properly connected protective ground. Consult with an electrician if necessary.

Grounding

A chassis grounding lug is available on the back panel of the DG645. Connect a heavy duty ground wire, #12AWG or larger, from the chassis ground lug directly to a facility earth ground to provide additional protection against electrical shock.

BNC shields are connected to the chassis ground and the AC power source ground via the power cord. Do not apply any voltage to the shield.

Line Fuse

The line fuse is internal to the instrument and may not be serviced by the user.

Operate Only with Covers in Place

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without all covers and panels in place.

Serviceable Parts

The DG645 does not include any user serviceable parts inside. Refer service to a qualified technician.

Symbols you may Find on SRS Products

Symbol	Description
	Alternating current
	Caution - risk of electric shock
	Frame or chassis terminal
	Caution - refer to accompanying documents
	Earth (ground) terminal
	Battery
	Fuse
	On (supply)
	Off (supply)

Specifications

Delays

Channels	4 independent pulses controlled in position and width. 8 delay channels available as an option (see Output Options).	
Range	0 to 2000 s	
Resolution	5 ps	
Accuracy	1 ns + (timebase error × delay)	
Jitter (rms)		
Ext. trig to any output	Delay <100 µs	Delay >100 µs
100MHz/N trigger rate	<20 ps	<30 ps + (timebase jitter × delay)
Other trigger rates	<30 ps	<40 ps + (timebase jitter × delay)
T_0 to any output	<15 ps + (timebase jitter × delay)	
Trigger delay	85 ns (ext. trig. to T_0 output)	

Timebases (+20 °C to +30 °C ambient)

Model #	Type	Jitter (s/s)	Stability (20 to 30 °C)	Aging (ppm/yr)
Std.	crystal	10^{-8}	2×10^{-6}	5
Opt. 4	OCXO	10^{-11}	1×10^{-9}	0.2
Opt. 5	rubidium	10^{-11}	1×10^{-10}	0.0005

External input	10 MHz ± 10 ppm, sine >0.5 V_{pp}, 1 kΩ impedance
Output	10 MHz, 2 V_{pp} sine into 50 Ω

External Trigger

Rate	DC to 1/(100 ns + longest delay): maximum of 10 MHz
Prescaled rate	DC to 100 MHz
Threshold	±3.50 VDC
Slope	Trigger on rising or falling edge
Impedance	1 MΩ + 15 pF

Internal Rate Generator

Trigger modes	Continuous, line or single shot
Rate	100 µHz to 10 MHz
Resolution	1 µHz
Accuracy	Same as timebase
Jitter (rms)	<25 ps (10 MHz/N trigger rate) <100 ps (other trigger rates)

Burst Generator

Trigger to first T_0	
Range	0 to 2000 s
Resolution	5 ps
Period between pulses	
Range	100 ns to 42.9 s
Resolution	10 ns
Delay cycles per burst	1 to $2^{32} - 1$

Outputs (T_0, AB, CD, EF, and GH)

Source impedance	50 Ω
Transition time	<2 ns
Overshoot	<100 mV + 10 % of pulse amplitude
Offset	±2 V
Amplitude	0.5 to 5.0 V (level + offset <6.0 V)
Accuracy	100 mV + 5 % of pulse amplitude

General

Computer interfaces	GPIB (IEEE-488.2), RS-232, and Ethernet. All instrument functions can be controlled through the computer interfaces.
Non-volatile memory	Nine sets of instrument configurations can be stored and recalled.
Power	<100 W, 90 to 264 VAC, 47 Hz to 63 Hz
Dimensions	8.5” × 3.5” × 13” (WHD)
Weight	9 lbs.
Warranty	One year parts and labor on defects in materials and workmanship

Output Options

Option 1 (8 Delay Outputs on Rear Panel)

Outputs (BNC)	T_0, A, B, C, D, E, F, G and H
Source impedance	50 Ω
Transition time	<1 ns
Overshoot	<100 mV
Level	+5 V CMOS logic
Pulse characteristics	
Rising edge	At programmed delay
Falling edge	The longer of trigger holdoff or 25 ns after longest programmed delay

Option 2 (8 High Voltage Delay Outputs on Rear Panel)

Outputs (BNC)	T_0, A, B, C, D, E, F, G and H
Source impedance	50 Ω
Transition time	<5 ns
Levels	0 to 30 V into high impedance 0 to 15 V into 50 Ω (amplitude decreases by 1 %/kHz)
Pulse characteristics	
Rising edge	At programmed delay
Falling edge	100 ns after the rising edge

Option 3 (Combinatorial Outputs on Rear Panel)

Outputs (BNC)	T_0, AB, CD, EF, GH, (AB + CD), (EF + GH), (AB + CD + EF), (AB + CD + EF + GH)
Source impedance	50 Ω
Transition time	<1 ns
Overshoot	<100 mV + 10 % of pulse amplitude
Pulse characteristics	
T0, AB, CD, EF, GH	Logic high for time between the programmed delays
(AB + CD), (EF + GH)	Two pulses created by the logic OR of the given channels
(AB + CD + EF)	Three pulses created by the logic OR of the given channels
(AB + CD + EF + GH)	Four pulses created by the logic OR of the given channels

Option SRD1 (Fast Rise Time Module)

Rise time	<100 ps
Fall time	<3 ns
Offset	−0.8 V to −1.1 V.
Amplitude	0.5 V to 5.0 V
Load	50 Ω

Quick Start Instructions

Step by Step Example

1. With the power button in the Standby position, connect the DG645 to a grounded outlet using the power cord provided.

2. Press the power button “in” to turn on the unit.

3. Press the following keys sequentially to load default settings: ‘RCL’, ‘0’, ‘ENTER’.

4. Press the TRIGGER ▲ key five times until the INT LED in the trigger section of the front panel is highlighted. This selects internal triggering.

5. Trigger an oscilloscope on the rising edge of T0’s output, and display AB’s output on the 1 µs/div scale.

6. Press the ‘DELAY’ key to view the delay for channel A.

7. Press the CURSOR ◄ and ► keys to the change the step size for channel A.

8. Press the MODIFY ▲ and ▼ keys to modify the delay for channel A by the current step size.

9. Press ‘1’, ‘µs’ to set the delay for channel A to 1 µs. (Note that the ‘µs’ key is shared with the MODIFY ▼ key.) The oscilloscope should show the AB output move one division after the trigger.

10. Press the EDGE ◄ and ► keys to select different delays.

11. Refer to the detailed instructions that follow for more information on the operation of the DG645.

Introduction

DG645 Features and Performance

The DG645 Digital Delay Generator is a precision 8-channel delay generator that can output arbitrary delays from 0 to 2000 s with 5 ps resolution and typical rms jitter of 12 ps.

The DG645 provides front-panel BNC connectors for five delay outputs: T0, AB, CD, EF, and GH. Internally, the DG645 generates 8 user-defined time events: A, B, C, D, E, F, G, and H. The timing events have a range of 2000 s and precision of 5 ps. The front-panel outputs pair these timing events to produce four output pulses: AB, CD, EF, and GH. In addition, a T0 output is asserted at t=0 and remains asserted until the longer of the trigger holdoff or 25 ns after the longest delay. Outputs may be configured with offsets ranging over ±2 V and amplitude steps from 0.5 to 5.0 V with positive or negative polarity. Both rising and falling edges are <2 ns for all amplitudes. Figure 1 summarizes the relationships between the programmed delays and the front-panel outputs.

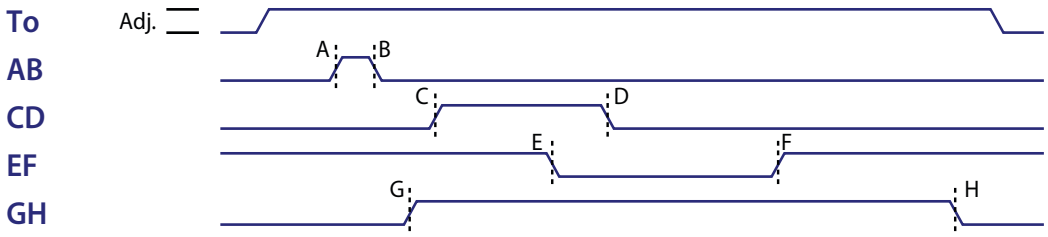

Figure 1: The DG645 Front Panel Outputs vs. Programmed Delay

An internal rate generator can generate triggers at rates ranging from 100 µHz to 10 MHz with 1 µHz resolution. The generator uses DDS technology to generate triggers with pulse to pulse rms jitter of <100 ps. This low jitter between triggers is maintained even at low trigger rates if the DG645's timebase is sufficiently stable.

The DG645 also supports externally triggered delays. It can be triggered on rising or falling edges with thresholds that range over ±3.5 V and insertion delays of approximately 85 ns.

The DG645 can also be synchronized to trigger sources operating at up to 100 MHz. A prescaler on the trigger input enables one to generate delay cycles at a sub-multiple of the trigger input frequency. Furthermore, each front-panel output has an additional prescaler that enables the output at a sub-multiple of the prescaled trigger input.

A burst generator enables the user to generate a burst of delay cycles with a single trigger. The trigger source can be internal or external. The user can configure the delay from the trigger to the first burst delay cycle, the period between delay cycles, and the number of delay cycles per burst.

A 10 MHz input enables the DG645 to synchronize its internal clock to an external reference. A 10 MHz output is provided to synchronize external instrumentation to the DG645.

The DG645 naturally supports remote control via a host computer. The DG645 comes standard with support for GPIB (IEEE 488.2), RS-232, and LAN TCP/IP connections. A host computer interfaced to the DG645 can perform virtually any operation that is accessible from the front panel.

Timebase Options

The DG645's standard timebase has an rms jitter of $<10^{-8}$ s/s. For improved performance, the DG645's timebase may be upgraded to an OCXO (Option 4) or a rubidium timebase (Option 5), both of which have rms jitter of about 10^{-11} s/s. Note that the DG645's jitter and accuracy are made up of two components: a baseline component and a timebase component. The baseline component dominates for short delays, but the timebase component dominates for long delays.

Figure 2 shows the typical timing error of the DG645 for the three timebases 1 year after calibration. A DG645 with a standard timebase will have the baseline error of 1 ns for time intervals <10 µs. For time intervals longer than 10 µs, the timebase component of the error will start to dominate. Thus, at 10 ms, the timing error is 100 ns. The OCXO's performance is about 50× better. The Rb's performance is still better by another factor of 100.

Figure 3 shows the DG645's typical rms jitter as a function of delay for the three timebases. As with the timing error, the DG645's performance at short delays is dominated by a baseline rms jitter of 25 ps. This baseline jitter is primarily due to the synchronization circuitry of the DG645. At long delays, however, the timebase component of the jitter dominates. At 10 ms, the stability of the standard timebase starts to degrade jitter performance. For the OCXO, baseline jitter performance extends out to about 5 s. For the Rb, baseline jitter performance extends out to about 100 s.

Note that the timebase component of the timing error and jitter can be eliminated if the DG645 is locked to an ideal external timing reference. The DG645 provides a 10 MHz input on the rear panel for locking the DG645 to an external reference.

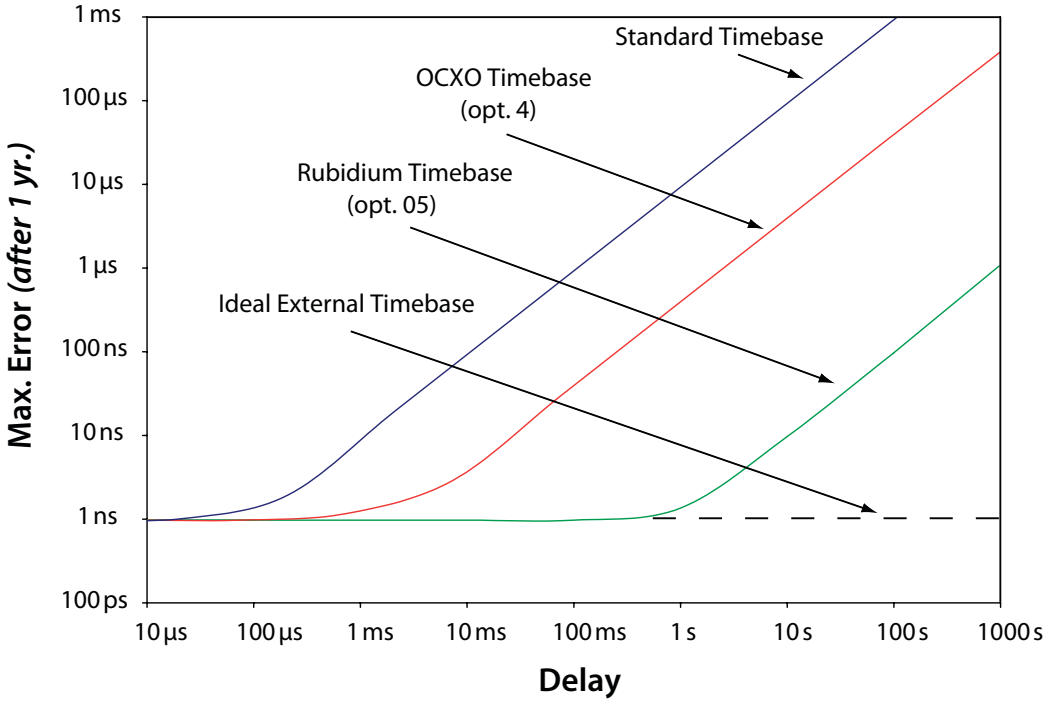

Figure 2: Typical DG645 Timing Error 1 Year after Calibration

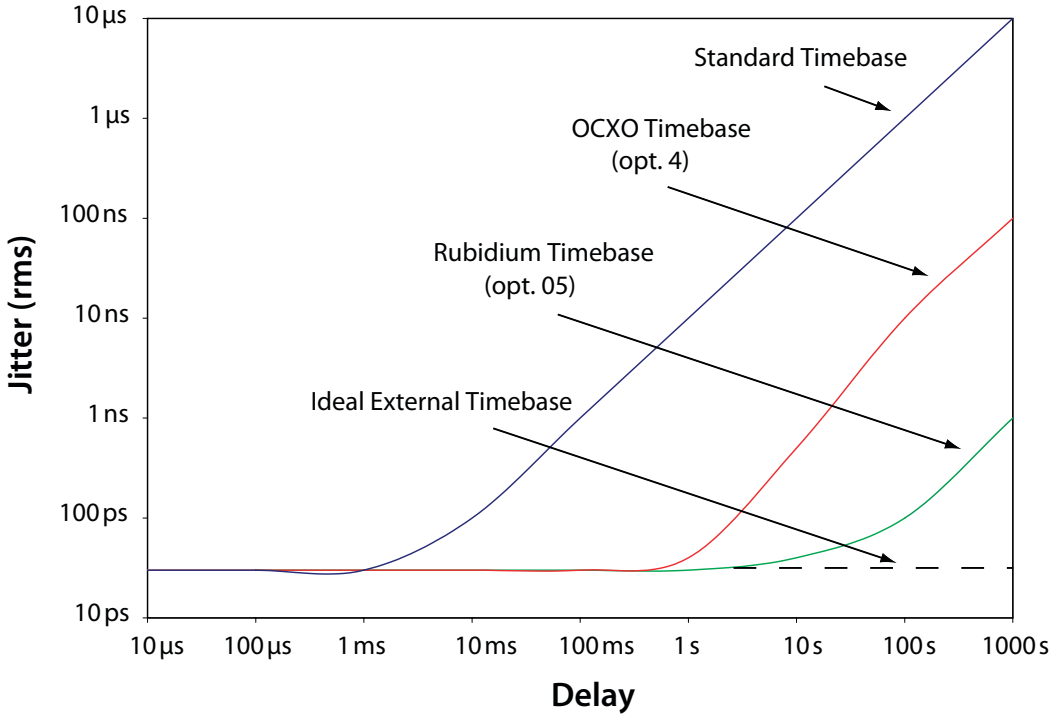

Figure 3: Typical rms Jitter vs. Delay Setting

Rear-Panel Options

Internally, the DG645 generates 8 user-defined time events: A, B, C, D, E, F, G, and H. The timing events have a range of 2000 s with 5 ps resolution. The front-panel outputs pair these timing events to produce four output pulses: AB, CD, EF, and GH. In addition, a T0 output is asserted at t=0 and remains asserted until the longer of the trigger holdoff or 25 ns after the longest delay. One of three rear-panel output modules may optionally be installed to provide the user with 9 additional delay outputs in various combinations.

Option 1: 8-Channel Outputs

Rear-panel Option 1 provides access to each of the 8 timing events, independently, by producing an output at T0 and at each of the 8 user-defined time events: A, B, C, D, E, F, G, and H. All of these outputs use positive 5 V logic (2.5 V into 50 Ω), going high at their programmed delay and going low after the longer of the trigger holdoff or 25 ns after the longest programmed delay. There is no duty cycle limitation for these outputs. Figure 4 summarizes these outputs.

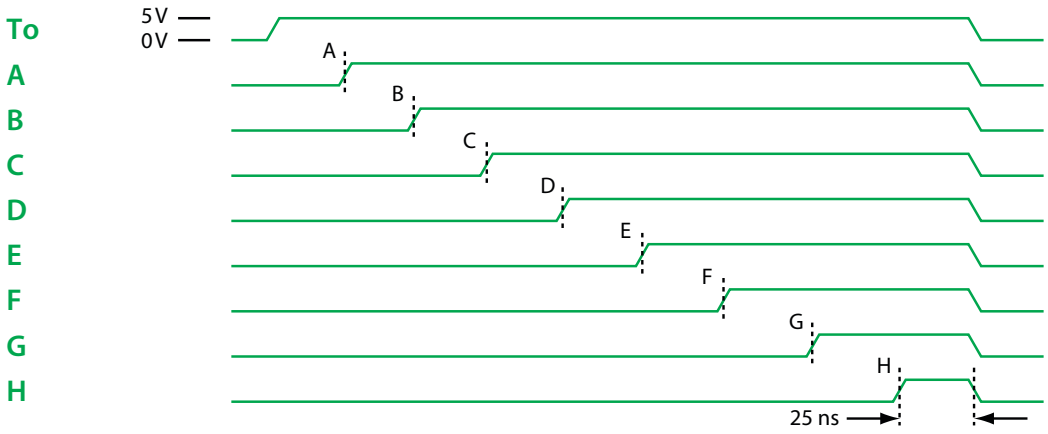

Figure 4: Option 1 Rear-Panel Outputs vs. Programmed Delay

Option 2: 8-Channel High Voltage Outputs

Rear-panel Option 2 provides 8 timing events independently by producing an output at T0 and at each of the 8 user-defined time events: A, B, C, D, E, F, G, and H. All of these outputs use positive 30 V logic (15 V into 50 Ω), going high at their programmed delay for a period of about 100 ns.

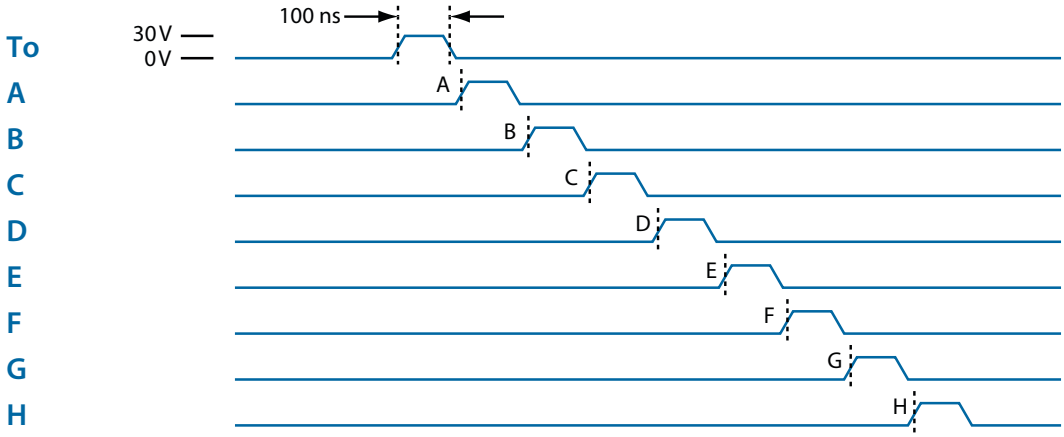

Figure 5: Option 2 Rear Panel Outputs vs Programmed Delay

Each of the nine outputs can drive a 50 Ω load to +15 V, requiring a total current of 9×15/50 = 2.7 A. The peak power of 108 W cannot be maintained, and so the output amplitude is reduced as the duty cycle is increased. As is detailed in Figure 6, the output pulse amplitude is reduced by less than 1 % per kHz of trigger rate.

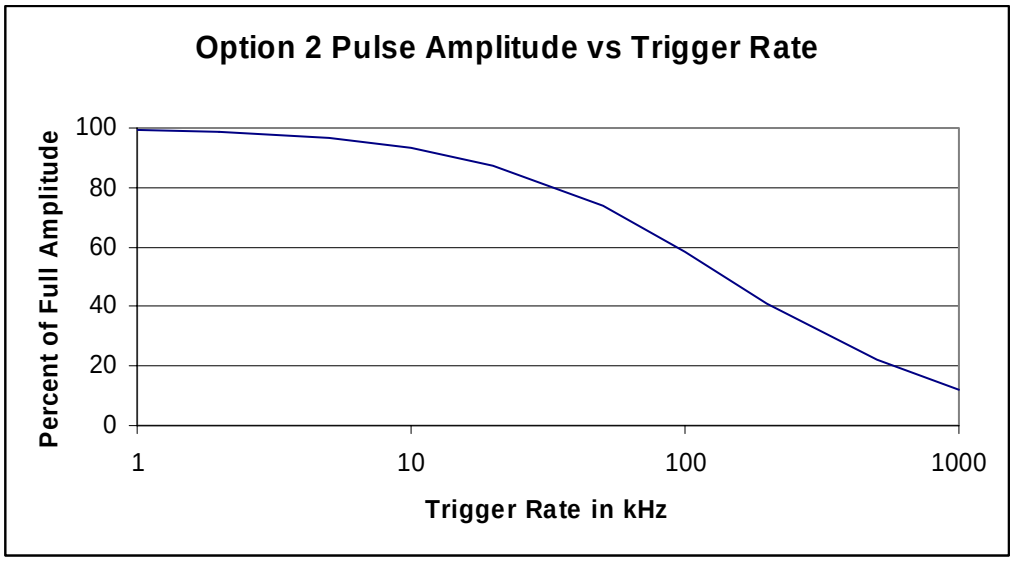

Figure 6: Option 2 Amplitude Reduction vs. Trigger Rate

Option 3: Combinatorial Logic Outputs

Rear-panel Option 3 provides copies of the front panel outputs on the rear panel. In addition, the logical OR of AB + CD, EF + GH, AB + CD + EF and AB + CD + EF + GH are also provided to give 1, 2, 3, or 4 precisely defined pulses on separate BNC outputs. All of these outputs use positive 5 V logic (2.5 V into 50 Ω), going high for the time between their programmed delays. There is no duty cycle limitation for these outputs.

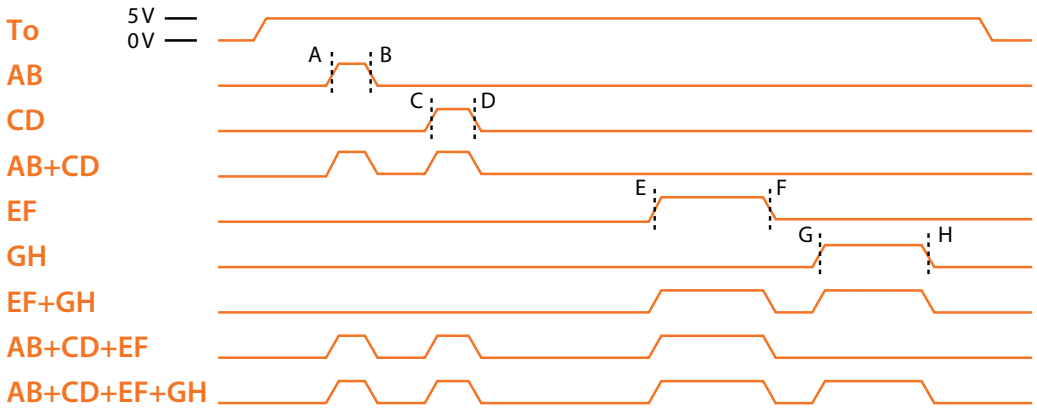

Figure 7: Option 3 Rear-Panel Outputs vs. Programmed Delay

Front Panel Accessory

SRD 1: Fast Rise Time Module

The SRD 1 is a front-panel accessory that can generate fast rise times of <100 ps. The module contains a male BNC connector on one end and a female BNC connector on the other for easy connection to the DG645 front-panel outputs. For proper operation, the DG645 outputs must be configured with a negative offset. Table 1 provides suggested offsets for various amplitudes to get an optimal pulse shape with the SRD 1.

Table 1: Suggested Output Configurations to Use with the SRD 1 for Optimum Pulse Shape

Amplitude (V)	Offset (V)
1.0	−0.8V
2.0	−0.9V
3.0	−0.9V
4.0	−1.0V
5.0	−1.1V

Front-Panel Overview

The front panel was designed to provide a simple, intuitive user interface to all the DG645 features (see Figure 8). The power switch is located in the lower right corner of the front panel. Pushing the switch enables power to the instrument. Pushing the switch again places the instrument in stand-by mode, where power is enabled only to optionally installed timebases. Power to the main board is turned off in stand-by mode.

The front panel is divided into four sections to indicate overall functionality: TRIGGER, DISPLAY, MODIFY, and STATUS. Keys in the TRIGGER section allow the user to select the type of triggering desired. Keys in the DISPLAY section control what is shown in the main display. Keys in the MODIFY section are used for changing the currently displayed item to a specific value or incrementing it by configurable steps. This section is also used to access secondary functions. LEDs in the STATUS section indicate the status of external timebases and remote interfaces.

The front panel also includes five BNC connectors which provide an external trigger input and five delay outputs for connecting the DG645 delay signals to user applications via standard BNC cables.

Figure 8: The DG645 Front Panel

Front-Panel BNCs

External Trigger Input

This BNC is labeled EXT TRIG, and it is located in the lower left corner of the front panel. If external triggering is selected, this input provides an external signal for triggering the five delay outputs. It has a 1 MΩ input resistance and can be configured for rising or falling edge triggers with thresholds that can range over ±3.5 V.

Delay Signal Outputs

There are five delay channel outputs on the front panel. They are labeled T0, AB, CD, EF, and GH. All the outputs have 50 Ω source impedances and should be terminated into 50 Ω loads. The amplitude, offset, and polarity of each output is programmable from the front panel. Amplitudes can range from 0.5 V to 5.0 V. Offsets can range over ±2.0 V. Polarities can be positive or negative. Channel T0 is always programmed to output a pulse that starts at a time defined as T ≡ 0 s and ends after the longer of the trigger holdoff or 25 ns after all other programmed delays have completed. The rest of the channels, AB through GH, have user programmable delay outputs. Channel AB has two programmable delays associated with it: delay A and delay B. Delay A is typically the starting edge and delay B, the trailing edge. Together, these two delays enable the user to control both the delay and the pulse width of the output relative to the T0 output. Channels CD, EF and GH behave similarly.

Triggering

The TRIGGER section of the front-panel display controls the triggering of the DG645. The ▲ and ▼ keys in this section select one of seven different triggering modes listed in Table 2.

Table 2: DG645 Triggering Modes

Label	Description
INT	Internal triggering at rates from 100 μHz to 10 MHz.
EXT ↗	External triggering on rising edges
EXT ↘	External triggering on falling edges
SNGL EXT ↗	Externally triggered single shot on a rising edge*
SNGL EXT ↘	Externally triggered single shot on a falling edges*
SNGL ↻	Single shot triggering
LINE	Trigger at the power line frequency

* Note that externally triggered single shots are denoted when both SNGL and the given EXT LEDs are lit.

LEDs in the TRIGGER section indicate which triggering mode is currently active as well as the triggered status of the DG645. The trigger rate and external trigger threshold may be displayed and modified by pressing the 'TRIG' key in the display section. Single shot triggering can be initiated from the front panel by pressing the 'ENTER' key when the main display reads 'TRG SINGLE SHOT.'

The DG645 can be synchronized with trigger sources operating at up to 100 MHz by programming a trigger hold off time or enabling the trigger input prescaler. For detailed information about configuring these options, see Trigger Holdoff (page 24) or Trigger Prescaling (page 24).

Trigger status of the DG645 is indicated by the four LEDs shown in Table 3.

Table 3: DG645 Trigger Status

Label	Description
TRIG'D	Turns on when the DG645 receives a valid trigger. Turns off when all delays are complete.
BURST	Turns on when burst mode is active. Otherwise, off.
RATE	Flashes when the DG645 receives a trigger while a delay is still in progress. The trigger is ignored.
INH	Flashes when the DG645 receives a trigger that was inhibited via the rear-panel INHIBIT input or while instrument settings are being modified

Display

The DISPLAY section allows the user to select which values are reported in the main front-panel display. The four basic displays for viewing and modifying instrument settings are shown in Table 4. Each display is activated by pressing the corresponding labeled key.

Table 4: DG645 Basic Displays

Label	Value Shown in Main Display When Pressed
TRIG	Trigger rate, trigger threshold, trigger holdoff, or trigger prescaler configuration
BURST	Burst configuration
DELAY	Channel delay settings
LEVEL	Front-panel output configuration including offset, amplitude and polarity.

Display Navigation

Pressing a given display key multiple times allows the user to cycle through all configuration parameters associated with a given display. The DELAY and LEVEL displays are associated with a given output BNC. LEDs located above the output BNCs indicate which edge of a given BNC's output is being displayed or modified. The user navigates between edges with the EDGE ◄ and ► keys.

Many of the main displays will have a digit that is blinking. This is called the cursor. The cursor indicates which digit will be modified when the MODIFY ▲ and ▼ keys are pressed. In many cases the user can move the cursor to the left or right with the CURSOR ◄ and ► keys located in the display section.

Modify

Numeric Entry

The MODIFY section is used to modify the current settings of the DG645. In most cases, the currently displayed item can be changed by entering a new value with the numeric

keys, and pressing an appropriate units key to complete the entry. Note that the units keys are shared with the MODIFY ▲, ▼, 'STEP SIZE' and 'ENTER' keys. For example, if a delay is currently being displayed, pressing the keys '1', '0', 'ns', sequentially will change the given delay to 10 ns. Similarly, if the trigger rate is displayed, pressing the keys '2', 'kHz' will set the internal trigger rate to 2 kHz.

Stepping Up and Down

Most instrument settings can be stepped up or down by a programmed amount. Normally, pressing the MODIFY ▲ and ▼ keys causes the displayed item to increment and decrement, respectively, by the associated step size. The blinking digit identifies the current cursor position and step size. It shows the digit that will change if it is incremented or decremented via the MODIFY ▲ and ▼ keys.

Step Size

The step size can be changed by factors of 10× by using the CURSOR ◄ and ► keys located in the display section. As the step size is changed, the blinking cursor will move appropriately, providing a visual cue of the current step size.

In addition to looking at the current cursor position, the step size for the current standard display can be viewed by pressing the 'STEP SIZE' key. Pressing 'STEP SIZE' a second time toggles the view back to the standard display. When the step size is being viewed, the STEP LED in the main display will be on.

When the current step size is being displayed, the user can modify it in one of two ways. First, the user may set an arbitrary step size by entering a value with the numeric keys in the MODIFY section and completing the entry by pressing an appropriate units key. Second, he can increment and decrement the current step size by exact factors of ten by pressing the MODIFY ▲ and ▼ keys respectively. For example, to set a delay step size to 25.000 ns, press the keys 'STEP SIZE', '2', '5', 'ns' sequentially. Pressing 'STEP SIZE' causes the step size to be displayed. The subsequent key presses set the new step size. With the step size set to 25.000 ns, pressing the MODIFY ▲ and ▼ keys, respectively, will increment or decrement the given delay by 25.000 ns.

Store and Recall Settings

The 'STO' and 'RCL' keys are for storing and recalling instrument settings. Instrument settings including trigger configuration, burst configuration, channel delays, level configurations, and all associated step sizes. Up to 9 different instrument settings may be stored in the locations 1 to 9. To save the current settings to location 5, press the keys 'STO', '5', 'ENTER' sequentially. To recall instrument settings from location 5, press the keys 'RCL', '5', 'ENTER' sequentially. Location 0 is reserved for recalling default instrument settings. See Factory Default Settings on page 36 for a list of default settings.

Secondary Functions

Many of the keys in the MODIFY section have secondary functions associated with them. The names of these functions are printed above the key. The '4' key, for example, has RS232 above it. The meaning of the secondary functions is summarized in Table 5.

Table 5: Secondary Functions

Label	Function Description
TTL	Set the selected output to TTL levels: 0 to 4 V
NIM	Set the selected output to NIM levels: -0.8 to 0 V
⎍ OUT	Configure selected output with positive polarity
⎏ OUT	Configure selected output with negative polarity
NET	Configure TCPIP interface
GPIB	Configure GPIB interface
RS232	Configure RS232 interface
DATA	Display the most recent data received over any remote interface
STATUS	View TCPIP, error, or instrument status
AB→ALL	Copy channel AB settings to all other channels
DISP OFF	Turn off the front-panel display
LOCAL	Go to local. Enables front-panel keys if in remote mode.
INIT	Load default instrument settings
CAL	Auto cal the front-panel delays for optimum jitter performance.
INHIBIT	Configure the rear-panel INHIBIT input.

A more detailed description of each of the secondary functions is given in the Secondary Functions section of the Operation chapter (page 29).

The secondary functions can only be accessed when SHIFT mode is active, which is indicated by the SHIFT LED being turned on. The SHIFT mode can be toggled on and off by pressing the 'SHIFT' key. Therefore, to configure the current channel to output TTL levels, you would press the 'SHIFT' key to activate SHIFT mode, and then press 'BACK SPACE' to execute the TTL secondary function.

Most of the secondary functions will automatically toggle SHIFT mode off when executed. NET, GPIB, RS232, and STATUS are exceptions to this rule because they have multiple menu options to display. Use the MODIFY ▲ and ▼ keys to modify a parameter. Press the secondary function key repeatedly to move between menu options. For example, pressing 'SHIFT', 'STO' sequentially causes the TCPIP configuration menu to be displayed. The first option is TCPIP ENABLE/DISABLE. Use the MODIFY ▲ and ▼ keys to change the setting as desired. Then press 'STO' again to move to the next option which is DHCP ENABLE/DISABLE. Continue pressing 'STO' until all TCPIP settings have been configured as desired.

Secondary functions that have an arrow (↵) printed after them, such as AB→ALL, INIT, CAL, and INHIBIT, require that the user press the 'ENTER' key to complete the action. For example, to initialize the instrument to its default settings, you would sequentially press 'SHIFT', 'INIT', 'ENTER'.

Cancel

The 'SHIFT' key also functions as a general purpose CANCEL key. Any numeric entry, which has not been completed by pressing a units key, can be canceled by pressing the 'SHIFT' key. Because of the dual role played by the SHIFT key, the user may have to press 'SHIFT' twice to reactivate SHIFT mode. The first key press cancels the current action, and the second key press activates SHIFT mode.

Status Indicators

TIMEBASE

In the upper right portion of the front panel are two groups of LED indicators. The upper group is labeled TIMEBASE. This contains the EXT and ERR LEDs. The EXT LED indicates that the DG645 has detected an external 10 MHz reference at the 10 MHz input BNC on the rear panel of the DG645. The DG645 will lock its internal clock to this external reference.

The ERR LED indicates that DG645 has not yet locked its internal timebase to an external input 10 MHz timebase. Normally, this LED will only flash momentarily when an external timebase is first applied to the rear input. If the LED stays on, it indicates that the DG645 may be unable to lock to the external timebase. This is most commonly caused by an input frequency which is offset from 10 MHz by more than 10 ppm.

INTERFACE

The lower group of LED indicators is labeled INTERFACE. These LEDs indicate the current status of the TCP/IP, RS-232, or GPIB remote programming interfaces. The REM LED turns on when the DG645 is placed in remote mode by one of the remote interfaces. In this mode, all the front-panel keys are disabled and the instrument can only be controlled via the remote interface. The user can return to normal, local mode by pressing the ‘3’ key once. The ‘LOCAL’ label above the key indicates the dual functionality of this key. The ACT LED flashes when a character is received or sent over one of the interfaces. This is helpful when troubleshooting communication problems. If a command received over the remote interface fails to execute due to either a parsing error or an execution error, the ERR LED will turn on and stay on until the status display is accessed. Information about the error is available in the STATUS secondary display.

Rear-Panel Overview

The rear panel provides connectors for AC power, GPIB/RS-232/TCPIP computer interfaces, chassis ground, external timing references, inhibit input, and various optional additional delay outputs (see Figure 9).

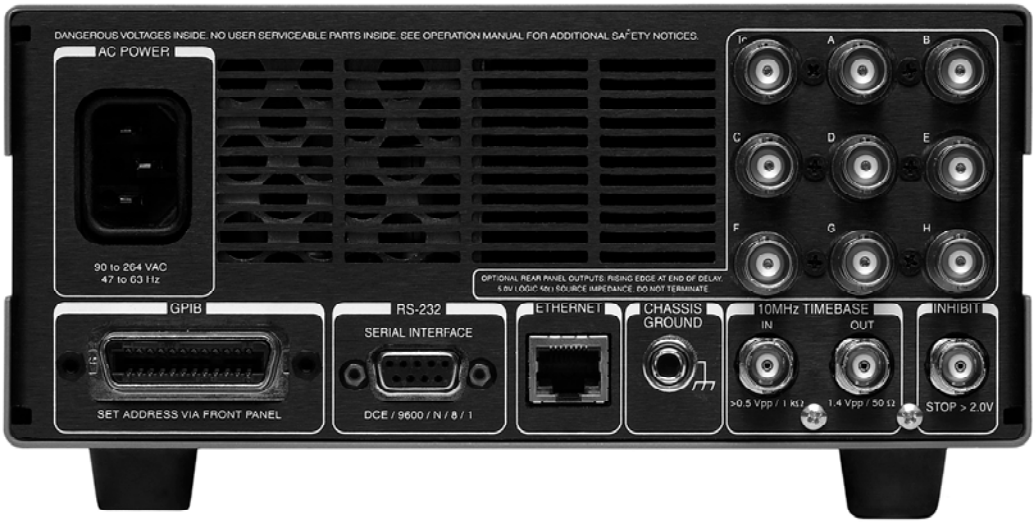

Figure 9: The DG645 Rear Panel

AC Power

The Power Entry Module is used to connect the DG645 to a power source through the power cord provided with the instrument. The center pin is connected to the DG645 chassis so that the entire box is grounded.

The source voltage requirements are 90 to 132 VAC or 175 to 264 VAC, 47 to 63 Hz (100 VA total).

Connect the DG645 to a properly grounded outlet. Consult an electrician if necessary.

GPIB

The DG645 comes standard with a GPIB (IEEE-488) communications port for communications over a GPIB bus. The DG645 supports the IEEE-488.1 (1978) interface standard. It also supports the required common commands of the IEEE-488.2 (1987) standard.

Before attempting to communicate with the DG645 over the GPIB interface, the GPIB address must configured by pressing the keys ‘SHIFT’, ‘GPIB’, ‘GPIB’. Use the MODIFY ▲ and ▼ keys to select the desired address. Then, either power-cycle the unit or reset the interface to ensure that the new interface settings are active.

A host computer interfaced to the DG645 can perform virtually any operation that is accessible from the front panel. Programming the DG645 is discussed in the DG645 Remote Programming chapter.

RS-232

The DG645 comes standard with an RS-232 communications port. The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 3, receive on pin 2). The baud rate is configurable from the front panel, but the rest of the communication parameters are fixed at 8 data bits, 1 stop bit, no parity, RTS/CTS hardware flow control.

Before attempting to communicate with the DG645 over RS-232, the baud rate must be configured by pressing the following keys: 'SHIFT', 'RS232', 'RS232'. Use the MODIFY ▲ and ▼ keys to select the desired baud rate. Then, either power-cycle the unit or reset the interface to ensure that the new interface settings are active.

A host computer interfaced to the DG645 can perform virtually any operation that is accessible from the front panel. Programming the DG645 is discussed in the DG645 Remote Programming chapter.

Ethernet

The DG645 comes standard with an RJ-45 connector for connecting it to an Ethernet based local area network (LAN) using standard Category-5 or Category-6 cable. It supports 100 Base-T Ethernet connections.

Before attempting to communicate with the DG645 over a LAN, the IP address, subnet mask address, and the default router must be configured. The DG645 supports automatic configuration of these parameters via DHCP or AUTO-IP. Manual configuration of a static IP address is also supported. Refer to the LAN Configuration section of the DG645 Remote Programming chapter for details on configuring the TCPIP interface.

A host computer interfaced to the DG645 can perform virtually any operation that is accessible from the front panel. Programming the DG645 is discussed in the DG645 Remote Programming chapter.

Chassis Ground

Use this grounding lug to connect the DG645 chassis directly to facility ground.

Timebase

10 MHz IN

The DG645 provides a 10 MHz BNC input for synchronizing its internal clock to an external 10 MHz reference. The external reference should provide greater than 0.5 V_{pp} into a 1 kΩ impedance. The DG645 will automatically detect the presence of an external 10 MHz reference and lock to it if possible. If the DG645 is unable to lock to the external reference, the front-panel TIMEBASE ERR LED will turn on and stay on until the DG645 either successfully locks to the external reference or the reference is removed.

10 MHz OUT

The DG645 provides a 10 MHz BNC output for synchronizing other instrumentation to the DG645's timebase.

Inhibit

The DG645 provides an inhibit BNC input for inhibiting triggers or various delay outputs. When the inhibit input is logic high (>2.0 V) either the trigger or the configured output is inhibited for that delay cycle. See the Inhibit section of the Operation chapter (page 36) for more information about configuring the inhibit functionality.

Optional Rear-Panel Outputs

The DG645 may be extended with 9 additional delay outputs on the rear panel. Three different combinations of outputs are available: 8-Channel CMOS logic outputs, 8-Channel HV outputs, or 4-Channel CMOS combinatorial logic outputs. For more information about these optional outputs, see Rear-Panel Options on page 4.

Operation

Front-Panel User Interface

The previous chapter described the function of the front-panel keys based on their location on the front panel. This section provides guidelines for viewing and changing instrument parameters independent of their location on the front panel.

Power On

At power on, the DG645 will briefly display “DG645” followed by the firmware version and the unit serial number. When power on initialization has completed, the DG645 will recall the latest known instrument settings from nonvolatile memory and be ready for use.

The DG645 continuously monitors front-panel key presses and will save the current instrument settings to nonvolatile memory after approximately five seconds of inactivity. To prevent the nonvolatile memory from wearing out, however, the DG645 will not automatically save instrument settings that change due to commands executed over the remote interface. The remote commands *SAV and *RCL can be used to explicitly save instrument settings over the remote interface, if desired. See the DG645 Remote Programming chapter for more information about these commands.

The DG645 can be forced to boot up at factory default settings. This is accomplished by pressing and holding the ‘BACK SPACE’ key during power up, until the initialization is complete. All instrument settings, except for the remote interface configurations, will be set back to their default values. All calibration bytes will be reset to the values set at the factory at the time of shipment. See the Factory Default Settings section on page 36 for a list of default settings.

The remote interface configurations can also be forced back to their factory default settings by pressing and holding the ‘STO’ key during power up initialization.

DG645 Main Display

Display Menus

The DG645 has four main display menus which are activated by dedicated keys in the DISPLAY section of the front panel. The function of each key is summarized in Table 6.

Table 6: DISPLAY Section Keys

Label	Value Shown in Main Display When Pressed
TRIG	Trigger rate, trigger threshold, trigger holdoff, or trigger prescaler configuration
BURST	Burst configuration
DELAY	Channel delay settings
LEVEL	Front-panel output configuration including offset, amplitude and polarity.

Display Navigation

Each display menu contains one or more instrument settings which may be successively viewed by pressing the given display key multiple times. For example, the LEVEL menu has three parameters that may be changed: offset, amplitude (step), and polarity. When 'LEVEL' is pressed the first time, output offset is displayed. Pressing 'LEVEL' a second time causes the output amplitude to be displayed. Pressing 'LEVEL' a third time causes output polarity to be displayed. Pressing 'LEVEL' yet again causes the output offset to be displayed again.

Edge Keys

The DELAY and LEVEL menus are tied to one of the five front-panel outputs labeled T0, AB, CD, EF, and GH. LEDs above the outputs indicate the currently selected output. The EDGE ◄ and ► keys enable the user to navigate among the leading and trailing edges of the various outputs. For example, if the delay menu is active and the LED on the left side of the AB output is lit, then the channel A delay will be shown in the main display. Pressing EDGE ► once will cause the LED on the right side of the AB output to light and the channel B delay to be displayed. Pressing EDGE ► again will cause the channel C LED and delay to display.

Cursor Keys

Most instrument settings have an independent step size associated with it. This is indicated by a blinking digit called the cursor. The cursor indicates which digit will be changed when the MODIFY ▲ and ▼ keys are pressed. The CURSOR ◄ and ► keys in the DISPLAY section enable the user to move the cursor left and right respectively. Each press of a CURSOR key increases or decreases the associated step size for the displayed parameter by a factor of 10.

Step Sizes

Although the CURSOR keys enable the user to quickly change the step size by exact factors of 10, sometimes it is desirable to set an arbitrary step size. Located below the

MODIFY ▲ and ▼ keys is the 'STEP SIZE' key. Pressing 'STEP SIZE' enables the user to view and modify the current step size associated with a parameter. When the step size for a parameter is displayed, the STEP LED in the main display will be highlighted. Once displayed, the step size may be increased or decreased by exact factors of 10 by pressing the MODIFY ▲ and ▼ keys. Alternatively, an arbitrary step size may be entered with the numeric keys and completing the entry by pressing an appropriate units key. (Note that the units keys are shared with the MODIFY ▲, ▼, 'STEP SIZE' and 'ENTER' keys.)

For example, if the channel A delay is currently displayed and the 1 ns digit is blinking, then the current step size for channel A is 1 ns. Pressing 'STEP SIZE' once will cause the display to show 'STP 000.000000001000'. Pressing the keys '2', '5', 'ns' sequentially, will change the current step size to 25 ns. Pressing 'STEP SIZE' again will cause channel A delay to display again, except that now the current step size is 25 ns and so the 10 ns digit will be blinking to indicate that the 10 ns digit will change when the delay is stepped. Continuing with the example, if the current delay for channel A is 0 ns, then pressing MODIFY ▲ will step up the delay to 25 ns.

Changing a Parameter

To change a parameter, enter a new value using the numeric keys in the MODIFY section of the front panel, and complete the entry by pressing an appropriate units key. (Note that the units keys are shared with the MODIFY ▲, ▼, 'STEP SIZE' and 'ENTER' keys.) Generally speaking, only the parameter shown in the main display can be changed. For example, to change the delay for channel A, press the 'DELAY' key to show delays. Then use EDGE ◄ and ► keys to navigate the display to channel A. To set the delay to 10 µs press the following keys sequentially: '1', '0' 'µs'. Pressing '1' initiates the parameter change, while pressing 'µs' completes entry and sets the delay to 10 µs.

If the user enters extra digits beyond the allowed resolution of a parameter, the extra digits will be rounded to the nearest allowed digit. For example, entering a voltage offset of 2.005 V will result in the offset being rounded to 2.01 V. (Outputs have a voltage resolution of 10 mV.)

Stepping a Parameter

Most parameters can be stepped up and down by their associated step sizes by respectively pressing the ▲ and ▼ keys in the MODIFY section of the front panel. For example, if channel A delay is currently being displayed as 'A=0+000.001234567890' and 4 is blinking, then the current step size is 1 µs. Pressing MODIFY ▲ will change the delay to 'A=0+000.001235567890'. Pressing MODIFY ▼ will bring the delay back to 'A=0+000.001234567890'.

Store and Recall Settings

The 'STO' and 'RCL' keys are for storing and recalling instrument settings. The instrument saves the trigger mode, burst configuration, all delays, all levels, all associated step sizes, and the current display. Up to nine different instrument settings may be stored in the locations 1 to 9. To save the current settings to location 5, for example, press the keys 'STO', '5', 'ENTER'. To recall instrument settings from location 5, press the keys 'RCL', '5', 'ENTER'. The user may also use the MODIFY ▲ and ▼ keys to select the

desired location, rather than enter the location directly with the numeric keys. The DG645 will remember the last location used for store and recall. To reuse the remembered location, simply skip the numeric entry when storing or recalling settings. For example, to recall settings from the remembered location, the user should simply press 'RCL', 'ENTER.' Location 0 is reserved for recalling default instrument settings. See Factory Default Settings on page 36 for a list of default settings.

Secondary Functions

Most of the keys in the MODIFY section of the front panel have secondary functions associated with them. The names of these functions are printed above the key. The '4' key, for example, has RS232 above it.

The secondary functions can only be accessed when SHIFT mode is active, which is indicated by the SHIFT LED being turned on. The SHIFT mode can be toggled on and off by pressing the 'SHIFT' key. Therefore, to configure the currently highlighted output BNC with positive polarity, you would press the 'SHIFT' key to activate SHIFT mode, and then press '8' to execute ⎍ OUT.

Most of the secondary functions will automatically toggle SHIFT mode off when executed. NET, GPIB, RS232 and STATUS are exceptions to this rule because they have multiple menu options to display. Use the MODIFY ▲ and ▼ keys to modify a parameter. Press the secondary function key repeatedly to move between menu options. For example, pressing 'SHIFT', 'STO' sequentially causes the TCPIP configuration menu to be displayed. The first option is TCPIP ENABLE/DISABLE. Use the MODIFY ▲ and ▼ keys to change the setting as desired. Then press 'STO' again to move to the next option, which is DHCP ENABLE/DISABLE. Continue pressing 'STO' until all TCP/IP settings have been configured as desired.

Secondary functions that have an arrow (↵) printed after them, such as AB→ALL, INIT, CAL, and INHIBIT, require that the user press the key 'ENTER' to complete the action. For example, to initialize the instrument to its default settings, you would sequentially press 'SHIFT', 'INIT', 'ENTER.'

Detailed descriptions of each of the secondary functions can be found later in this chapter.

Triggering

The DG645 supports seven different triggering modes listed in Table 7. The ▲ and ▼ keys in TRIGGER section of the front-panel display enable the user to select the desired triggering mode. LEDs in the TRIGGER section indicate which triggering mode is currently active as well as the trigger status of the DG645.

Table 7: DG645 Triggering Modes

Label	Description
INT	Internal triggering at rates from 100 µHz to 10 MHz.
EXT ⨍	External triggering on rising edges
EXT ⨏	External triggering on falling edges
SNGL EXT ⨍	Externally triggered single shot on a rising edge*
SNGL EXT ⨏	Externally triggered single shot on a falling edges*
SNGL ↻	Single shot triggering
LINE	Trigger at the power line frequency

* Note that externally triggered single shots are denoted when both SNGL and the given EXT LEDs are lit.

To access the trigger configuration from the front panel, press the 'TRIG' key in the DISPLAY section of the front panel. The trigger menu options are summarized in Table 8. Press the 'TRIG' key to cycle between menu options. Use the MODIFY ▲ and ▼ keys or the numeric keypad to modify parameters.

Table 8: DG645 Trigger Menu

LED Label	Example Display	Description
TRIG RATE	'TRG 1000.000000'	Internal trigger rate
TRIG THRES	'TRG THRES 1.00'	External trigger input threshold
STATUS	'ADV. TRIGGERING ON'	Enable/disable advanced triggering
STATUS	'HOLD 0.000010000000'	Trigger holdoff time
STATUS	'TRG PRESCALE 100'	Prescaler configuration parameter

Note that the trigger holdoff and prescaler configurations menu items will only be accessible if advanced triggering is enabled.

The prescaler configuration parameters are tied to a given front-panel output. Use the EDGE ◄ and ► keys to select the various parameters. The prescaler configuration parameters are summarized in Table 9.

Table 9: DG645 Prescaler Configuration

Edge	Example Display	Description
T0	'TRG PRESCALE 1000'	Prescale triggers by the given count. In this case, a delay cycle will be generated once every 1000 triggers.
A,C,E,G	'AB PRESCALE 10	Prescale the front-panel AB output by the given count. In this case, the AB output would be enabled once every 10 successfully triggered delay cycles.
B,D,F,H	'AB PHASE 5'	Shift the phase of the AB output enable to the given cycle. In this case, the 5^{th} delay cycle would be enabled. This would be followed by the 15^{th}, 25^{th}, etc.

Internal Triggering

The DG645 has an internal rate generator that can generate triggers at rates from 100 µHz to 10 MHz with 1 µHz resolution. The generator uses DDS technology to generate triggers with pulse-to-pulse rms jitter of <100 ps. This low jitter between triggers is maintained even at low trigger rates, if the DG645's timebase is sufficiently stable. Furthermore, the use of DDS technology enables the DG645 to change frequencies quickly. No settling time is required.

To select internal triggering, press the TRIGGER ▲ key until the INT LED is highlighted.

Once internal triggering is selected, the user can view and modify the trigger rate by pressing the 'TRIG' key in the DISPLAY section of the front panel. If the trigger rate is currently 1 kHz, then the main display will show 'TRG 1000.000000', and the TRIG RATE LED just below the main display will be highlighted. Once displayed, the user can modify the trigger rate using any of the methods discussed in the section Front-Panel Interface earlier in this chapter.

External Triggering

The DG645 can be externally triggered via the EXT TRIG input BNC on the front panel. The trigger input can be configured for rising or falling edges with trigger thresholds that can range over ±3.5 V. It has a fixed input impedance of 1 MΩ. There will be approximately 85 ns of insertion delay between an externally applied trigger and the T0 output. As with internal triggering, the DG645 can accommodate trigger rates up to 10 MHz.

To select external triggering press the TRIGGER ▲ and ▼ keys until EXT ⨍ or EXT ⨏ LED is highlighted for rising and falling edge triggers, respectively.

Once external triggering is selected, the user can view and modify the trigger threshold by pressing the 'TRIG' key in the DISPLAY section of the front panel. If the trigger threshold is 1.0 V, then the main display will show 'TRG THRES 1.00', and the TRIG THRES LED just below the main display will be highlighted. Once displayed, the user can modify the trigger rate using any of the methods discussed in the section Front-Panel Interface earlier in this chapter.

Single Shot Triggering

The DG645 supports single shot triggering. Single shot triggering enables the user to trigger the DG645 one shot at a time.

Normal Single Shot

Normal single shot triggering is selected by pressing the TRIGGER ▲ and ▼ keys until the SNGL ⟲ LED is highlighted by itself. To initiate a single shot, first press the 'TRIG' key in the DISPLAY section once or twice until the display shows 'TRG SINGLE SHOT.' Once this is displayed, the user initiates single shots by pressing the 'ENTER' key.

Externally Triggered Single Shot

Externally triggered single shots are selected by pressing the TRIGGER ▲ and ▼ keys until the SNGL ⟲ LED and either EXT ⨍ or EXT ⨏ LED is highlighted for rising and falling edge triggers. To initiate a single shot, first press the 'TRIG' key in the DISPLAY section successively until the display shows 'TRG SINGLE SHOT.' Once this is displayed, the user arms the DG645 to accept a single external trigger by pressing the 'ENTER' key. The display will show 'TRG RDY SINGLE SHOT' when the unit is armed, but not yet triggered.

Line Triggering

The DG645 can be triggered at the power line frequency by selecting line triggering. This will typically be at either 50 or 60 Hz, depending on in which country the unit is operated.

To select line triggering, press the TRIGGER ▼ key until the LINE LED is highlighted. When line triggering is selected, pressing the 'TRIG' key in the DISPLAY section will cause the main display to show 'TRG LINE' and the TRIG RATE LED just below the main display to be highlighted.

Advanced Triggering

The DG645 supports a number of complex triggering requirements via trigger holdoff and prescaling registers. These features are normally disabled, but they become enabled and accessible when advanced triggering is turned on. To enable advanced triggering, press 'TRIG' until the display shows 'ADV. TRIGGERING OFF', and then press MODIFY ▲ to turn it on.

Trigger Holdoff

Trigger holdoff sets the minimum allowed time between successive triggers. For example, if the trigger holdoff is set to 10 µs, then successive triggers will be ignored until at least 10 µs have passed since the last trigger. The red RATE LED will flash with each ignored trigger. Specifying holdoff is useful if a trigger event in your application generates a significant noise transient that must have time to decay away before the next trigger is generated.

Trigger holdoff can also be used to trigger the DG645 at a sub-multiple of a known input trigger rate. For example, by selecting LINE as the trigger source and setting the holdoff to 0.99 s, the DG645 can be triggered synchronously with the power line, but at 1 Hz. This technique works as long as the timebase of the trigger source doesn't vary significantly relative to the DG645's timebase. Otherwise, trigger prescaling should be used.

Note that trigger holdoff is available only after advanced triggering is enabled. Once advanced triggering is enabled, the user can view and modify the trigger holdoff by successively pressing the 'TRIG' key in the DISPLAY section of the front panel until the display prefix is 'HOLD'. If the trigger holdoff is 10 µs, then the main display will show 'HOLD 0.000010000000', and the STATUS LED just below the main display will be highlighted. Once displayed, the user can modify the trigger holdoff using any of the methods discussed in the section Front-Panel Interface earlier in this chapter.

Trigger Prescaling

The DG645 supports a number of complex triggering requirements through a set of prescaling registers. Trigger prescaling enables the DG645 to be triggered synchronously with a much faster source, but at a sub-multiple of the original trigger frequency. For example, the DG645 can be triggered at 1 kHz, but synchronously with a mode locked laser running at 80 MHz, by prescaling the trigger input by 80,000.

Furthermore, the DG645 also contains a separate prescaler for each front panel output that enables it to operate at a sub-multiple of the prescaled trigger input frequency. Continuing with the example above, if the AB prescaler is set to 100, the AB output will only be enabled for 1 out of every 100 delay cycles which is equivalent to a rate of 1 kHz/100 = 10 Hz.

Lastly, the DG645 contains a separate phase register for each output prescaler that determines the phase of the prescaler output relative to the other prescaled outputs. For example, if both the AB and CD prescalers are set to 100 and their phase registers to 0 and 50, respectively, then AB and CD will both run at 10 Hz, but CD's output will be enabled 50 delay cycles after AB's output.

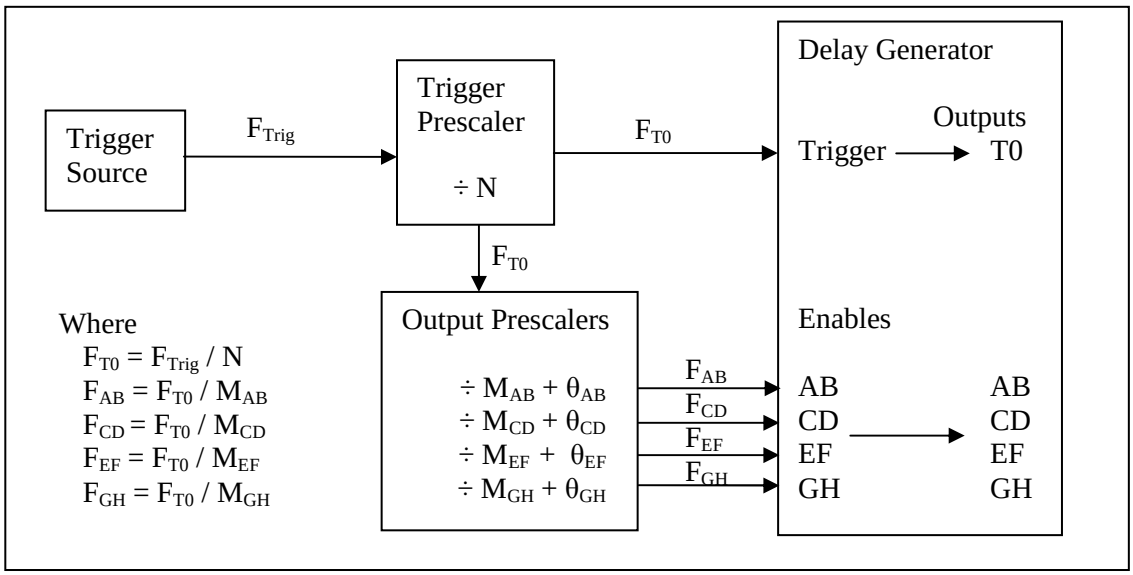

Figure 10: The DG645 Trigger Prescaling

The DG645's trigger prescaling operation is summarized in Figure 10. The trigger prescaler value, N, can range from 1 to $2^{30} - 1$. The channel prescaler values, M, can range from 1 to $2^{16} - 1$. Phase values may range from 0 to M – 1.

Note that trigger prescaling is not available in single shot modes. In other modes, trigger prescaling is available only after advanced triggering is enabled. Once advanced triggering is enabled, the user can access the prescaler configuration by pressing the 'TRIG' until the display shows 'TRG PRESCALE 1', and then pressing the EDGE ◄ and ► keys to select the desired prescaler configuration parameter. The user can modify the various prescale factors using any of the methods discussed in the section Front-Panel Interface earlier in this chapter.

Trigger Status

Trigger status of the DG645 is indicated by the four LEDs shown in Table 10.

Table 10: DG645 Trigger Status

Label	Description
TRIG'D	Turns on when the DG645 receives a valid trigger. Turns off when all delays are complete.
BURST	Turns on when burst mode is active. Otherwise, off.
RATE	Flashes when the DG645 receives a trigger while a delay is still in progress. The trigger is ignored.
INH	Flashes when the DG645 receives a trigger that was inhibited via the rear-panel INHIBIT input or while instrument settings are being modified

Burst Mode

The DG645 has the ability to generate a burst of N delay cycles on each trigger. The trigger which generates the burst may come from any of the DG645 trigger modes. The user can configure the number of delay cycles in the burst, the period between delay cycles, and the delay before the first delay cycle is initiated. These parameters are named burst count, burst period, and burst delay. The relationship between these parameters is summarized in Figure 11. In addition, to simplify triggering of other instruments synchronously with the burst, the T_0 output may be configured to fire on the first delay cycle of the burst, rather than for all delay cycles as is normally the case.

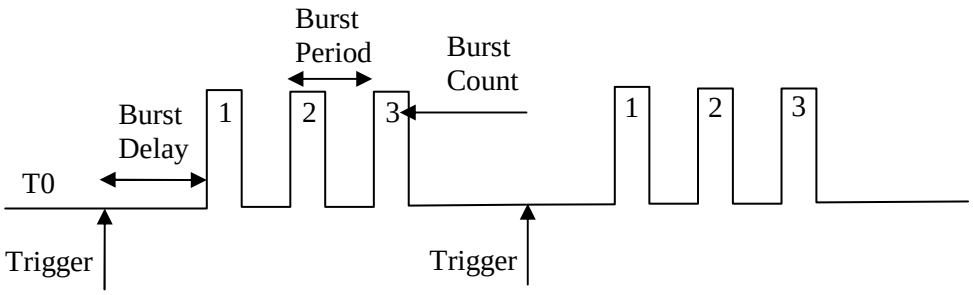

Figure 11: T0 Output in Burst Mode

To access the burst configuration from the front panel, press the 'BURST' key in the DISPLAY section of the front panel. The burst menu options are summarized in Table 11

Table 11: DG645 Burst Menu

LED Label	Example Display	Description
STATUS	'BURST ON'	Enable or disable burst mode
STATUS	'T0 OUTPUT ON ALL'	Configure T_0 to fire on all delay cycles of the burst, or just the first delay cycle of the burst.
BURST CNT	'CNT 5'	Number of delay cycles per burst
BURST PERIOD	'PER 0.00010000'	Period between delay cycles
BURST DELAY	'DLY 0.000000000000'	Added insertion delay from the trigger to the first delay cycle

Press the 'BURST' key to cycle between menu options. Use the MODIFY ▲ and ▼ keys or the numeric keypad to modify parameters. Burst count can be any number from 1 to $2^{32} - 1$. Burst period can be set with 10 ns resolution. Burst delay can be set with 5 ps resolution.

When burst mode is active, the BURST LED in the TRIGGER section of the front panel will be highlighted.

Delays

The DG645 has 8 independent delay channels labeled A through H. Each delay may range from 0 to 1,999.999,999,999,995 s and be set with 5 ps resolution. Each front-panel output has a pair of delays associated with it labeled AB, CD, EF and GH. For output AB, delay A normally defines the leading edge of the pulse, and delay B, the trailing edge. The other outputs behave similarly. Thus, both the delay and the pulse width of each output may be independently defined.

Output T0 is a reference pulse predefined to start at time T ≡ 0 s and end after the longer of the trigger holdoff or 25 ns after all delays have completed. There is approximately 85 ns of insertion delay between an external trigger and the T0 output.

Delays may be configured from the front panel by pressing the 'DELAY' key in the DISPLAY section of the front panel. Different channels are selected by using the EDGE ◄ and ► keys. LEDs above the output BNCs indicate which channel is currently selected. Once a given delay is displayed, the user can modify it using any of the methods discussed in the section Front-Panel Interface earlier in this chapter.

Example delay settings are shown in Table 12. Output T0 is always defined to be 0 s. The trailing edge of output T0, called T1, is predefined to be the longer of the trigger holdoff or 25 ns more than the longest delay, which is delay D in this example. Output AB will go high 0.123456789125 s after T0. It will have a pulse width of 1 ms. Output EF will go high coincident with T0 and stay high for 0.987654321235 s. 0.1 s before output EF goes low, output GH will go high for 1 ms.

Table 12: Example Delay Settings

Channel	Delay
T0	'0≡0+000.000000000000'
T1	'T≡0+123.456789158455'
A	'A=0+000.123456789125'
B	'B=A+000.001000000000'
C	'C=0+123.456789123455'
D	'D=C+000.000000010000'
E	'E=0+000.000000000000'
F	'F=E+000.987654321235'
G	'G=F−000.100000000000'
H	'H=G+000.001000000000'

Linked Delays

The example delay settings shown in Table 12 illustrate that delays may be linked to one another. In the example, F is linked to E, G is linked to F, and H is linked to G. To modify the linkage of a channel, press 'SHIFT', CURSOR ◄ to place the cursor on the LINK digit (pressing CURSUR ◄ multiple times also works). Then use the MODIFY ▲ and ▼ keys to change the linkage. Delays may be linked arbitrarily as long as no circular links are created. For example, If B is linked to A, it is not possible to then link A to B.

Note that changing the linkage does not change the actual delay. It does, however, change the display for the delay to reflect the new linkage. Continuing with the example in Table 12, if the linkage for G was changed from F to T0, the G delay would read 'G=0+000.887654321235', which is the same actual delay, but it reflects the new linkage.

Levels

The DG645 has five delay outputs on the front panel labeled T0, AB, CD, EF, and GH. The outputs may be configured to have offsets ranging over ±2.0 V and amplitudes ranging from 0.5 to 5.0 V with 0.01 V resolution as long as the absolute level does not exceed 6.0 V. They may be configured with positive or negative polarity. Rising and falling edges are <2 ns, independent of amplitude. Each output has a fixed source impedance of 50 Ω and should be terminated into 50 Ω. When left unterminated, output levels will double up to a maximum voltage of about 7 V.

Levels may be configured from the front panel by pressing the 'LEVEL' key in the DISPLAY section of the front panel multiple times until the desired parameter is displayed. Different channels are selected by using the EDGE ◄ and ► keys. LEDs above the output BNCs indicate which channel is currently selected. Once a given level parameter is displayed, the user can modify it using any of the methods discussed in the section Front-Panel Interface earlier in this chapter.

Table 13: Level Menu Options

Parameter	Example Display	Description
Offset	'AB OFFSET 0.00' V	Offset of low level from ground
Amplitude	'AB STEP 2.50' V	The step or amplitude from the low level to the high level
Polarity	'AB POLARITY POS'	The polarity of the pulse may be positive or negative.

For clarity, the meaning of the three output configuration parameters is diagrammed in Figure 12.

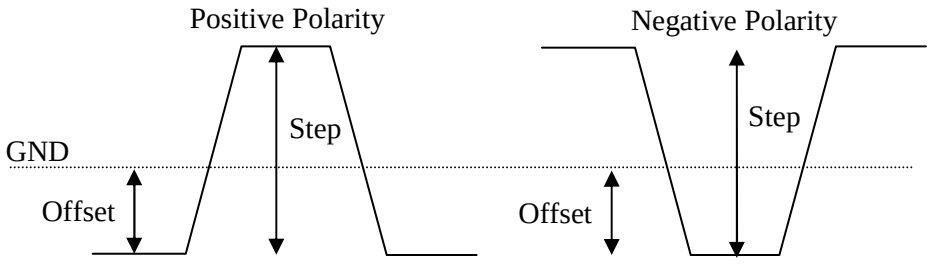

Figure 12: Output Level Configuration

Secondary Functions

Most of the keys in the MODIFY section of the front panel have secondary functions associated with them. The names of these functions are printed above the key. The ‘4’ key, for example, has RS232 above it.

To access these secondary functions, follow the instructions described in the Front-Panel User Interface section at the beginning of this chapter. Details about each of the functions follow.

TTL

The TTL function configures the currently selected output for TTL levels. The offset is 0.0 V and the amplitude step is 4.0 V. The polarity of the output is unchanged.

NIM

The NIM function configures the currently selected output for NIM levels. The offset is −0.8 V and the amplitude step is 0.8 V. The polarity of the output is unchanged.

Positive OUT

The ⎍ OUT function configures the currently selected output with positive polarity. The offset and amplitude step for the output is unchanged.

Negative OUT

The ⎎ OUT function configures the currently selected output with negative polarity. The offset and amplitude step for the output is unchanged.

NET

The NET menu enables the user to configure the TCP/IP based remote interfaces. This is where the means for assigning the DG645 with an IP address, subnet mask, and default router are configured. To find out what the DG645’s current operating TCP/IP parameters are, see the STATUS menu later in this chapter. Before connecting the DG645 to your LAN, check with your network administrator for the proper method of configuration of networked instruments on your network.

The NET menu has several options. Press the ‘NET’ key to cycle through the options. Use the MODIFY ▲ and ▼ keys to change an option. Use the numeric keypad to enter an IP address when appropriate. Note that changes to the TCP/IP configuration do not take effect until the interface is reset or the instrument is power cycled. The NET menu parameters are summarized in Table 14.

Table 14: NET Menu Options for TCP/IP Configuration

Parameter	Example Display	Description
TCP/IP	'TCPIP enabled'	Enable or disable all TCP/IP access
DHCP	'DHCP enabled'	Enable or disable the DHCP client to automatically obtain an appropriate TCP/IP configuration from a DHCP server
Auto-IP	'AutoIP enabled'	Enable or disable the AUTO-IP protocol for automatically obtaining an appropriate link-local TCP/IP configuration in the 169.254.x.x IP address space.
Static IP	'Static IP enabled'	Enable or disable a static IP configuration.
IP	'IP 192.168.0.5'	IP address to use if static IP is enabled.
Subnet	'Subnet 255.255.0.0'	Subnet mask to use if static IP is enabled.
Default gateway	'Def Gty 192.168.0.1'	Default gateway or router to use for routing packets not on the local network if static IP is enabled
Bare socket interface	'Bare enabled'	Enable or disable raw socket access on TCP/IP port 5025.
Telnet interface	'Telnet enabled'	Enable or disable telnet access on TCP/IP port 5024.
VXI-11 Interface	'Net instr enabled'	Enable or disable the VXI-11 net instrument remote interface.
Link speed	'Speed 100 Base-T'	Set the Ethernet link speed.
Reset	'Reset no'	Select 'yes' and press 'ENTER' to reset the TCP/IP interface to use the latest TCP/IP configuration settings.

TCP/IP Configuration Methods

In order to function properly on an Ethernet based local area network (LAN), the DG645 needs to obtain a valid IP address, a subnet mask, and a default gateway or router address. The DG645 supports three methods for obtaining these parameters: DHCP, Auto-IP, and Static IP. Check with your network administrator for the proper method of configuration of networked instruments on your network.

If the DHCP client is enabled, the DG645 will try to obtain its TCP/IP configuration from a DHCP server located somewhere on the local network. If the Auto-IP protocol is enabled, the DG645 will try to obtain a valid link-local IP configuration in the 169.254.x.x address space. If the static IP configuration is enabled, the DG645 will use the given TCPIP configuration. When all three methods are enabled, the TCPIP configuration will be determined in the following order of preference: DHCP, Auto-IP, static IP. Given that Auto-IP is virtually guaranteed to succeed, it should be disabled if a static IP configuration is desired.

In order to view the TCP/IP configuration the DG645 obtained via DHCP or Auto-IP, see the STATUS menu.

TCP/IP Based Remote Interfaces

The DG645 supports three TCP/IP based remote interfaces: raw socket, telnet, and VXI-11 net instrument. Raw socket access is available on port 5025. Telnet access is available on port 5024. The VXI-11 interface enables IEEE 488.2 GPIB like access to the DG645 over TCP/IP. It enables controlled reads and writes and the ability to generate service requests. Most recent VISA instrument software libraries support this protocol.

Link Speed

The DG645's physical Ethernet layer supports 10 Base-T and 100 Base-T link speeds. Due to a known bug in the silicon of the microprocessor, the DG645 may fail to auto-negotiate its link speed correctly. To avoid this possibility, the default link speed is set to 100 Base-T, but it can be set to 10 Base-T or to auto-negotiate if desired.

Reset the TCP/IP Interface

Note that changes to the TCP/IP configuration do not take affect until the TCP/IP interface is either reset or the instrument is power cycled. To reset the TCP/IP interface, navigate through the NET menu options until 'reset no' is displayed. Press MODIFY ▲ to change the display to 'reset yes' and then press 'ENTER.' Any active connections will be aborted. The TCP/IP stack will be re-initialized and configured using the latest configuration options.

GPIB

The GPIB menu enables the user to configure the GPIB remote interface. The GPIB menu has several options. Press the 'GPIB' key, successively, to cycle through the options. Use the MODIFY ▲ and ▼ keys to change an option. Note that changes to the GPIB configuration do not take effect until the interface is reset or the instrument is power cycled. The GPIB menu parameters are summarized in Table 15.

Table 15: GPIB Menu Options

Parameter	Example Display	Description
GPIB	'GPIB enabled'	Enable or disable all GPIB access
Address	'Address 15'	GPIB address
Reset	'Reset no'	Select 'yes' and press 'ENTER' to reset the GPIB interface.

GPIB Address

In order to communicate properly on the GPIB bus, the DG645 must be configured with a unique address. Use the Address menu option to set the DG645's GPIB address. Then reset the interface to make sure the new address is active.

Reset the GPIB Interface

Note that changes to the GPIB configuration do not take affect until the GPIB interface is either reset or the instrument is power cycled. To reset the GPIB interface, navigate through the GPIB menu options until 'reset no' is displayed. Press MODIFY ▲ to change the display to 'reset yes', and then press 'ENTER'.

RS232

The RS232 menu enables the user to configure the RS-232 remote interface. The RS232 menu has several options. Press the 'RS232' key to cycle through the options. Use the MODIFY ▲ and ▼ keys to change an option. Note that changes to the RS-232 configuration do not take effect until the interface is reset or the instrument is power cycled. The RS232 menu parameters are summarized in Table 16.

Table 16: RS232 Menu Options

Parameter	Example Display	Description
RS-232	'RS232 enabled'	Enable or disable all RS-232 access
Baud rate	'Baud 9600'	The baud rate to use for RS-232 connections
Reset	'Reset no'	Select 'yes' and press 'ENTER' to reset the RS-232 interface.

RS-232 Configuration

In order to communicate properly over RS-232, the DG645 and the host computer both must be configured to use the same configuration. The DG645 supports the following baud rates: 115200, 57600, 38400, 19200, 9600, and 4800. The rest of the communication parameters are fixed at 8 data bits, 1 stop bit, no parity, and RTS/CTS hardware flow control.

Use the baud rate menu option to set the DG645's baud rate. Then reset the interface to make sure the new baud rate is active.

Reset the RS-232 Interface

Note that changes to the RS-232 configuration do not take affect until the RS-232 interface is either reset or the instrument is power cycled. To reset the RS-232 interface, navigate through the RS232 menu options until 'reset no' is displayed. Press MODIFY ▲ to change the display to 'reset yes' and then press 'ENTER.'

DATA

The DATA function enables the user to see the hexadecimal ASCII characters received by the DG645 from the most recently used remote interface. This functionality is useful when trying to debug problems in communicating with the DG645. Use the MODIFY ▲ and ▼ keys to scroll through the data. The decimal point indicates the last character received.

STATUS

The STATUS function enables the user to view status information about the DG645. The DG645 has four status menus: TCP/IP status, error status, instrument status, and self test. Use the MODIFY ▲ and ▼ keys to select the desired status. Then press the 'STATUS' key to view each item of status.

TCP/IP Status

TCP/IP status contains status information on the current IP configuration of the DG645. Table 17 summarizes the TCP/IP status information reported by the DG645.

Table 17: TCP/IP Status Menu

Parameter	Example Display	Description
Ethernet mac address	'Phy Adr 00.19.b3.02.00.01'	This is the ethernet mac address assigned to this DG645 at the factory.
Link status	'Connected'	Indicates if the Ethernet hardware has established a link to the network.
IP address	'IP 192.168.0.5'	The current IP address.
Subnet mask	'Subnet 255.255.0.0'	The current subnet mask.
Default gateway	'Def Gty 192.168.0.1'	The current default gateway or router.

Error Status

The error status menu enables the user to view the number and cause of execution and parsing errors. Table 18 summarizes the error status items reported by the DG645. See section Error Codes on page 62 for a complete list of error codes.

Table 18: Error Status Menu

Parameter	Example Display	Description
Error count	'Error cnt 1'	Indicates the number of errors detected.
Error code	'111 Parse Error'	Provides the error number and description of the error.

Instrument Status

The instrument status menu enables the user to view the instrument configuration. It reports on installed timebases and rear panel options.

Table 19: Instrument Status Menu

Parameter	Example Display	Description
Serial Number	'Serial 001013'	Unit serial number
Version	'Version 1.00.10A	Firmware version
Rear option	'Rear opt. 3'	Indicates which rear option, if any, is installed.
Oscillator	'Osc. standard'	Indicates which timebase is installed.
Rb lock	'Rb stable'	If a Rb timebase is installed, this item indicates if the Rb has stabilized.

Self Test

The instrument self test runs a series of tests to check the operation of the unit. Three sets of tests are run. They are summarized in Table 20.

Table 20: Instrument Self Test

Self Test	Description
1	Tests communication to various peripherals on the motherboard including GPIB chip, the PLL chip, the DDS chip, the octal DACs, the FPGA, the temperature sensor, and the serial EEPROM.
2	Tests the operation of the front-panel outputs. Basic offset and amplitude functionality is tested for each channel.
3	Tests delay generation operation for all 10 delays.

After the self test completes, the unit is reset to default instrument settings. If errors are encountered, they will be reported on the front-panel display when detected. The errors detected are stored in the instrument error buffer and may be accessed via the error status menu after the self test completes. See section Error Codes on page 62 for a complete list of error codes.

AB→ALL

The AB→ALL function enables the user to quickly copy the delays and levels of output AB to all other channels. All delay and level settings and associated step sizes are copied. Delay linkage is mimicked if A and B are linked. Otherwise linkage is set to T0 for all channels.

DISPL OFF

The DISPL OFF function enables the user to turn off the front-panel display if desired.

LOCAL

When the DG645 is in remote mode, the REM LED is highlighted and front-panel instrument control is disabled. Pressing the 'LOCAL' key, '3' on the numeric keypad, re-enables local front-panel control.

INIT

Executing the INIT function forces the DG645 to default settings. This is equivalent to a Recall 0 or executing the *RST remote command. See Factory Default Settings on page 36 for a list of the DG645's default settings.

CAL

Executing the CAL function automatically recalibrates the DG645 delay channels for optimum jitter performance. The sample and hold DAC, Vjitter, and analog delays for T0, T1, A, B, C, D, E, F, G, and H are all calibrated by executing this function. After the automatic calibration completes the original instrument settings are restored. If errors are encountered, they will be reported on the front-panel display when detected. The errors detected are stored in the instrument error buffer and may be accessed via the error status menu after the calibration completes. See section Error Codes on page 62 for a complete list of error codes.

In addition to automatic calibration, this function also provides manual user access to the timebase calibration and all the cal bytes modified by the auto calibration. Press the 'CAL' key to cycle through the various cal bytes. Use the MODIFY ▲ and ▼ keys or the numeric key pad to modify a given cal byte. The cal bytes that can be accessed via the front panel are shown in Table 21.

Table 21: DG645 Cal Menu

Label	Description
Auto cal	Press 'ENTER' to automatically calibrate the delay channels for optimum jitter performance
Cal cloc	Timebase calibration byte. Adjust to calibrate the frequency of the installed timebase.
Cal jit	Vjitter calibration byte
Cal ins	Global insertion delay calibration byte
Cal t0	Channel T0 calibration byte
Cal t1	Channel T1 calibration byte
Cal A	Channel A calibration byte
Cal B	Channel B calibration byte
Cal C	Channel C calibration byte
Cal D	Channel D calibration byte
Cal E	Channel E calibration byte
Cal F	Channel F calibration byte
Cal G	Channel G calibration byte
Cal H	Channel H calibration byte
Cal sh offset	Sample and hold offset calibration byte
Cal sh slope	Sample and hold slope calibration byte

INHIBIT

The INHIBIT menu enables the user to configure the rear-panel inhibit input. The DG645 may be configured to inhibit triggers, or individual delay outputs. The options are summarized in Table 22. Use the MODIFY ▲ and ▼ keys to make a selection and press 'ENTER' to activate the selection.

Table 22: DG645 Inhibit Configuration

Configuration Option	Description
Off	The rear panel input is disabled
Trig	A logic high inhibits triggers
AB	A logic high inhibits output AB
AB CD	A logic high inhibits outputs AB and CD
AB CD EF	A logic high inhibits outputs AB, CD, and EF
AB CD EF GH	A logic high inhibits outputs AB, CD, EF, and GH

Factory Default Settings

The factory default settings are listed in Table 23. The DG645 may be forced to assume its factory default settings by power cycling the unit with the 'BACK SPACE' key depressed. This forces all instrument settings except for communication parameters to the factory defaults. It is similar to the INIT secondary function and the *RST remote command, which also reset the unit to factory default settings, but it also performs these additional actions:

1. Resets *PSC to 1
2. Forces nonvolatile copies of *SRE and *ESE to 0.
3. Resets all stored settings from 1 to 9 back to default settings
4. Restores all cal bytes to the values determined at the factory at the time of shipment.

Table 23: DG645 Factory Default Settings

Parameter	Setting
Delay A	0 s
Delay B	A + 10 ns
Delay C	0 s
Delay D	C + 10 ns
Delay E	0 s
Delay F	E + 10 ns
Delay G	0 s
Delay H	G + 10 ns
Delay Step Size	1 ns
Trigger Mode	Single Shot
Trigger Threshold	1.0 V
Trigger Threshold Step Size	0.1 V
Trigger Rate	1 kHz
Trigger Rate Step Size	1 kHz
Trigger Holdoff	0 s
Trigger Holdoff Step Size	1 ns
Trigger Prescaling	Disabled
All Prescale Factors	1
All Prescale Factor Step Sizes	1
All Output Prescale Shift Factors	0
All Output Prescale Shift Factor Step Sizes	1
Burst Mode	Off
Burst T_0 Configuration	T_0 Output on All
Burst Count	5
Burst Count Step Size	1
Burst Period	100 µs
Burst Period Step Size	100 ns
Burst Delay	0 s
Burst Delay Step Size	1 ns
Output Offset	0.0 V
Output Offset Step Size	0.1 V
Output Amplitude	2.5 V
Output Amplitude Step Size	0.1 V
Output Polarity	Positive
Inhibit Configuration	Inhibit Trigger
Display	Delay for Channel A
Remote Interface Terminator	<CR><LF>: (13, 10)

The factory default settings of the various communications interfaces for the DG645 are listed in Table 24. The DG645 may be forced to assume its factory default communication settings by power cycling the unit with the 'STO' key depressed.

Table 24: DG645 Factory Default Settings for Communications Parameters

Parameter	Setting
RS-232	Enabled
RS-232 Baud Rate	9600
GPIB	Enabled
GPIB Address	15
TCP/IP	Enabled
DHCP	Enabled
Auto-IP	Enabled
Static IP	Enabled
IP	0.0.0.0
Subnet Mask	0.0.0.0
Default Gateway	0.0.0.0
Bare (Raw) Socket Interface at TCP/IP port 5025	Enabled
Telnet Interface at TCP/IP port 5024	Enabled
VXI-11 Net Instrument Interface	Enabled
Ethernet Speed	100 Base-T

Troubleshooting

The DG645 does not include any user serviceable parts inside. The line fuse is internal to the instrument and may not be serviced by the user. In the event of instrument failure, refer service to a qualified technician.

Table 25 contains a list of troubleshooting tips for various symptoms which may occur in a normally functioning unit. Please consult this list before contacting SRS regarding a potential instrument failure.

Table 25: Troubleshooting Tips

Symptom	Resolution
Single shot triggering doesn't work	Make sure the SNGL LED is lit. Press the TRIGGER ▲ and ▼ keys until is. Then press 'TRIG' successively until the display shows 'TRG SINGLE SHOT'. Finally, press 'ENTER' to initiate a single shot.
External triggers are being applied, but no delay cycle is generated. No other trigger LEDs are highlighted or flashing.	Make sure the external triggering is selected. Press TRIGGER ▲ and ▼ keys until only the EXT LED with the desired slope is selected. Make sure the trigger threshold is set correctly. Press 'TRIG' until the display shows 'TRG THRES 1.00'. Set the threshold appropriate for your trigger source.

Triggers are being applied but no delay cycle is generated. The TRIG'D LED may or may not be on and the RATE LED flashes.	A delay cycle or a burst of delay cycles is still in progress. Check that trigger holdoff is set to zero. Check that burst mode is turned off. Check the length of the longest delay by pressing 'DELAY' followed by EDGE ◄ or ► until the display reads something like 'T ≡ 0+123.123456789123'. Make sure this number isn't larger than expected.
Triggers are being applied but no delay cycle is generated and the INH LED flashes.	Triggers are being inhibited. Remove any signal being applied to the rear-panel inhibit input.
Triggers are being applied but no delay cycle is generated, and neither RATE or INH flashes, but the trigger mode is flashing once a second.	The trigger input is being prescaled. Turn off prescaling by pressing 'TRIG' successively until the display shows 'TRIG PRESCALE ON'. Press MODIFY ▼ to turn off prescaling.
Channel T0 works, but the others don't and the INH LED flashes	The inhibit signal is configured to disable the channel. Remove any signal being applied to the rear-panel inhibit input.
Channel T0 works, but the others don't and the trigger mode LED is flashing once a second.	Output prescaling is enabled. Turn off prescaling by pressing 'TRIG' successively until the display shows 'TRIG PRESCALE ON.' Press MODIFY ▼ to turn off prescaling.
TIMEBASE ERR LED flashes once a second	An optional rubidium oscillator is installed, but it has not yet stabilized. Wait 10 minutes for the rubidium to warm up and stabilize.
No RS-232 communication	Check that RS-232 is enabled. Press 'SHIFT', 'RS232' to verify that it is enabled. Press 'RS232' again to verify that the baud rate is correct. If the settings must be changed, power cycle the unit to ensure that the new configuration is in effect.
No GPIB communication	Check that GPIB is enabled. Press 'SHIFT', 'GPIB' to verify that it is enabled. Press 'GPIB' again to verify that the GPIB address is correct. Make sure no other instrument on the GPIB bus is using the same address. If the settings must be changed, power cycle the unit to ensure that the new configuration is in effect.
No TCP/IP communication	Check that the DG645 has established a valid connection to the Ethernet. Press 'SHIFT', 'STATUS', MODIFY ▲, 'STATUS', 'STATUS'. The display should read 'CONNECTED'. Press 'STATUS' three more times to verify that the TCP/IP configuration is as expected. Refer to the remote programming chapter for more information on configuring TCP/IP communication.

DG645 Remote Programming

Introduction

The DG645 may be remotely programmed via the GPIB interface, the RS-232 serial interface, or the LAN Ethernet interface. Any host computer interfaced to the DG645 can easily control and monitor the operation of the DG645.

Interface Configuration

All of the DG645 interface configuration parameters can be accessed via the front panel through shifted functions dedicated to the interface. Table 26 identifies the shifted functions that are used to configure each interface.

Table 26: DG645 Interface Configuration

Shifted Function	Interface Configuration
NET	LAN, TCP/IP interface
GPIB	GPIB 488.2 interface
RS232	RS-232 serial interface

Each interface's configuration is accessed by pressing 'SHIFT' followed by one of the interface keys ('NET', 'GPIB', or 'RS232'). Once a given interface configuration is activated, parameters for the interface are selected by successive key presses of the given interface key. For example, pressing 'SHIFT', 'RS232' activates the RS-232 configuration. The first menu item is RS-232 Enable/Disable. Pressing 'RS232' again moves the selection to RS232 baud rate.

Once a parameter is selected, it is modified by pressing the MODIFY ▲ and ▼ keys. The only exception to this is for selections that require an internet address, such as static IP address, network mask, and default gateway address. In this case the address is modified by entering the new address with the numeric keys and pressing 'ENTER'.

All interfaces are enabled by default, but each interface may be disabled individually if desired. Any modifications made to an interface do not take effect until the interface is reset or the unit is power cycled.

GPIB

The DG645 comes with an IEEE 488 standard port for communicating over GPIB. The port is located on the rear panel of the DG645. The configuration parameters for the GPIB interface are shown in Table 27.

Table 27: DG645 GPIB Configuration

Interface Parameter	Default	Meaning
GPIB Enable/Disable	Enabled	Enable or disable the interface
GPIB Address (0-30)	15	Primary GPIB address.
Reset interface (Yes/No)	No	Force a reset of the interface.

Any changes made will not take effect until the interface is reset or the unit is power cycled.

RS-232

The DG645 comes standard with an RS-232 communications port. The port is located on the rear panel of the DG645. The configuration parameters for the RS-232 interface are shown in Table 28.

Table 28: DG645 RS-232 Configuration

Interface Parameter	Default	Meaning
RS-232 enable/disable	Enabled	Enable or disable the interface
Baud rate (4800-115200)	9600	RS-232 baud rate
Reset interface (yes/no)	No	Force a reset of the interface.

The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin3, receive on pin2). The factory default communication parameters are set to: 9600 baud rate, 8 data bits, 1 stop bit, no parity, RTS/CTS hardware flow control. All of these communication parameters are fixed except for the baud rate. Any changes made to the interface configuration will not take effect until the interface is reset or the unit is power cycled.

LAN

The DG645 comes standard with an RJ-45 network communications port located on the rear panel of the DG645. The port may be used to communicate with the DG645 over a 10/100 Base-T Ethernet connected network or LAN. Before connecting the DG645 to your LAN, check with your network administrator for the proper method of configuration of networked instruments on your network. The TCP/IP configuration options for the LAN interface are shown in Table 29.

Table 29: DG645 LAN Configuration

Interface Parameter	Default	Meaning
TCP/IP Enable/Disable	Enabled	Enable or disable all TCP/IP based interfaces.
DHCP Enable/Disable	Enabled	Enable or disable automatic network configuration via DHCP.
Auto-IP Enable/Disable	Enabled	Enable or disable automatic network configuration in the 169.254.x.x internet address space if DHCP fails or is disabled.
Static IP Enable/Disable	Enabled	Enable manual configured network configuration in the event that the automatic configuration fails or is disabled.
IP Address	0.0.0.0	Static IP address to use when manual configuration is active.
Subnet Address	0.0.0.0	Network mask to use when manual configuration is active. The network mask is used to determine which IP addresses are on the local network.
Default Gateway	0.0.0.0	Default gateway or router to use when manual configuration is active. The gateway is the ip address that packets are sent to if the destination IP address is not on the local network.
Bare Socket Enable/Disable	Enabled	Enable or disable raw socket access to the DG645 via TCP port 5025.
Telnet Enable/Disable	Enabled	Enable or disable access to the DG645 via telnet to port 5024.
Net Instr. Enable/Disable	Enabled	Enable or disable access to the DG645 via VXI-11 net instrument protocols.
Ethernet Speed 10/100/Auto	100 Base-T	Ethernet physical layer link speed.
Reset interface (Yes/No)	No	Force a reset of the interface.

The DG645 supports automatic and static network configuration. When more than one configuration is enabled, the DG645 selects network configuration parameters with the following priority: DHCP, Auto-Ip, Manual. Note that since Auto-Ip will virtually always succeed, it should be disabled if static configuration is desired. Any changes made to the

interface configuration will not take effect until the interface is reset or the unit is power cycled.

Network Security

Network security is an important consideration for all TCP/IP networks. Please bear in mind that the DG645 does NOT provide security controls, such as passwords or encryption, for controlling access to the DG645. If such controls are needed, you must provide it at a higher level on your network. This might be achieved, for example, by setting up a firewall and operating the DG645 behind it.

Front-Panel Indicators

To assist in programming, the DG645 has three front-panel indicators located under the INTERFACE section: REM, ACT, and ERR. The REM LED is on when the DG645 is in remote lock out. In this mode, the front-panel interface is locked out and the DG645 can only be controlled via the remote interface. To go back to local mode, the user must press the LOCAL key, '3'. The ACT LED serves as an activity indicator that flashes every time a character is received or transmitted over one of the remote interfaces.

The ERR LED will be highlighted when a remote command fails to execute due to illegal syntax or invalid parameters. The user may view the cause of errors from the front panel by pressing the keys 'SHIFT', 'STATUS', sequentially. Next press MODIFY ▲ until the display reads 'Error Status.' Finally, press 'STATUS,' successively, to view the total error count followed by the individual errors. The error codes are described in section Error Codes on page 62.

Command Syntax

Communications with the DG645 uses ASCII characters. All commands are 4-characters long and are case-insensitive. Standard IEEE-488.2 defined commands begin with the '*' character followed by 3 letters. DG645 specific commands are composed of 4 letters.

The four letter mnemonic (shown in CAPS) in each command sequence specifies the command. The rest of the sequence consists of parameters.

Commands may take either *set* or *query* form, depending on whether the '?' character follows the mnemonic. *Set only* commands are listed without the '?', *query only* commands show the '?' after the mnemonic, and *optionally query* commands are marked with a '(?)'.

Parameters shown in { } and [ ] are not always required. Parameters in { } are required to set a value, and are omitted for queries. Parameters in [ ] are optional in both set and query commands. Parameters listed without any surrounding characters are always required.

Do NOT send () or {} or [] or spaces as part of the command.

The command buffer is limited to 255 bytes, with 25 byte buffers allocated to each of up to 3 parameters per command. If the command buffer overflows, both the input and

output buffers will be flushed and reset. If a parameter buffer overflows, a command error will be generated and the offending command discarded.

Commands are terminated by a semicolon, a <CR> (ASCII 13), or a <LF> (ASCII 10). If the communications interface is GPIB, then the terminating character may optionally be accompanied by an EOI signal. If the EOI accompanies a character other than a <LF>, a <LF> will be appended to the command to terminate it. Execution of the command does not begin until a command terminator is received.

Aside from communication errors, commands may fail due to either syntax or execution errors. Syntax errors can be detected by looking at bit 5 (CME) of the event status register (*ESR?). Execution errors can be detected by looking at bit 4 (EXE) of the event status register. In both cases, an error code, indicating the specific cause of the error, is appended to the error queue. The error queue may be queried with the LERR? command. Descriptions of all error codes can be found in the section Error Codes, starting on page 62.

Parameter Conventions

The command descriptions use parameters, such as i, f, and v. These parameters represent integers or floating point values expected by the command. The parameters follow the conventions summarized in Table 30. Parameters specific to delays and outputs are summarized in Table 31 in the Delay and Output Commands section.

Table 30: Command Parameter Conventions

Parameter	Meaning
i, j, k	An integer value
f	A floating point value representing a frequency in Hz
t	A floating point value representing time in seconds.
v	A floating point value representing voltage in volts.

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Common IEEE-488.2 Commands

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Command List

Common IEEE-488.2 Commands

***CAL?** — **Auto calibration**

Runs the instrument auto calibration routine and returns 0 if successful and 17 (EXE_FAIL_AUTO_CAL) if unsuccessful. If unsuccessful the error buffer will include device dependent errors related to the parts of the self test that failed.

Example

*CAL?<CR> Run the instrument auto calibration routine and return the result.

***CLS** — **Clear Status**

Clear Status immediately clears the ESR and INSR registers as well as the LERR error buffer.

***ESE(?){i}** — **Standard Event Status Enable**

Set (query) the Standard Event Status Enable register {to i}. Bits set in this register cause ESB (in STB) to be set when the corresponding bit is set in the ESR register.

***ESR?** — **Standard Event Status Register**

Query the Standard Event Status Register. Upon executing a *ESR? query, the returned bits of the *ESR register are cleared. The bits in the ESR register have the following meaning:

Bit	Meaning
0	OPC – operation complete
1	Reserved
2	QYE – query error
3	DDE – device dependent error
4	EXE – execution error
5	CME – command error
6	Reserved
7	PON – power-on

Example

*ESR?<CR> A return of ‘176’ would indicate that PON, CME, and EXE are set.

***IDN?** — **Identification String**

Query the instrument identification string.

Example

*IDN?<CR> Returns a string similar to ‘Stanford Research Systems,DG645,s/n004025,ver1.00.00E’

***OPC(?)** — **Operation Complete**

The set form sets the OPC flag in the ESR register when all prior commands have completed. The query form returns ‘1’ when all prior commands have completed, but does not affect the ESR register.

***PSC(?){i}** — **Power-on Status Clear**

Set (query) the Power-on Status Clear flag {to i}. The Power-on Status Clear flag is stored in nonvolatile memory in the DG645, and thus, maintains its value through power-cycle events.

If the value of the flag is 0, then the Service Request Enable and Standard Event Status Enable Registers (*SRE, *ESE) are stored in non-volatile memory, and retain their values through power-cycle events. If the value of the flag is 1, then these two registers are cleared upon power-cycle.

Example

*PSC 1<CR>	Set the Power-on Status Clear to 1.
*PSC?<CR>	Returns the current value of Power-on Status Clear.

***RCL i** — **Recall Instrument Settings**

Recall instrument settings from location i. The parameter i may range from 0 to 9. Locations 1 to 9 are for arbitrary use. Location 0 is reserved for the recall of default instrument settings.

Example

*RCL 3<CR>	Recall instruments settings from location 3.

***RST** — **Reset the Instrument**

Reset the instrument to default settings. This is equivalent to *RCL 0. It is also equivalent to pressing the keys ‘SHIFT’, ‘INIT’, ‘ENTER’ on the front panel. See Factory Default Settings on page 36 for a list of default settings.

Example

*RST<CR>	Resets the instrument to default settings

***SAV i** — **Save Instrument Settings**

Save instrument settings to location i. The parameter i may range from 1 to 9. Location 0 is reserved for default instrument settings. The following settings are saved:

1.TODO

Example

*SAV 3<CR>	Save current settings to location 3.

***SRE(?){i}** — **Service Request Enable**

Set (query) the Service Request Enable register {to i}. Bits set in this register cause the DG645 to generate a service request when the corresponding bit is set in the STB register.

***STB?** — **Status Byte**

Query the standard IEEE 488.2 serial poll status byte. The bits in the STB register have the following meaning:

Bit	Meaning
0	INSB – INSR summary bit
1	BUSY – Set if delay cycle is in progress, otherwise cleared
2	Reserved
3	Reserved

4	MAV – message available
5	ESB – ESR summary bit
6	MSS – master summary bit
7	Reserved

Example

*STB?<CR> A return of '113' would indicate that INSB, MAV, ESB, and MSS are set. INSB indicates that an enabled bit in INSR is set. MAV indicates that a message is available in the output queue. ESB indicates that an enabled bit in ESR is set. MSS reflects the fact that at least one of the summary bits is set.

*TRG — Trigger a Delay

When the DG645 is configured for single shot triggers, this command initiates a single trigger. When it is configured for externally triggered single shots, this command arms the DG645 to trigger on the next detected external trigger.

*TST? — Self Test

Runs the instrument self test and returns 0 if successful and 16 (EXE_FAIL_SELF_TEST) if unsuccessful. If unsuccessful the error buffer will include device dependent errors related to the parts of the self test that failed.

Example

*TST?<CR> Run the instrument self test and return the result.

*WAI — Wait for Command Execution

The instrument will not process further commands until all prior commands including this one have completed.

Example

*WAI<CR> Wait for all prior commands to execute before continuing.

Status and Display Commands

DISP(?){i,c} — Display

Set (query) the current display value {to i}. Set the displayed channel to c. Parameter c may range from 0–9 for channels T0–H. The parameter i selects the display type.

i	Display
0	Trigger rate
1	Trigger threshold
2	Trigger single shot
3	Trigger line
4	Advanced triggering enable
5	Trigger holdoff
6	Prescale configuration
7	Burst mode
8	Burst delay
9	Burst count
10	Burst period
11	Channel delay

12	Channel output levels
13	Channel output polarity
14	Burst T_0 configuration

Example

DISP 11,2	Show delay for channel A
DISP 12,4	Show offset for channel CD
DISP 12,5	Show amplitude for channel CD
DISP 13,5	Show polarity for channel CD

INSE(?){i} Instrument Status Enable

Set (query) the Instrument Status Enable register {to i}. }. Bits set in this register cause INSB (in STB) to be set when the corresponding bit is set in the INSR register.

INSR? Instrument Status Register

Query the Instrument Status Register. Upon executing a INSR? query, the returned bits of the INSR register are cleared. The bits in the INSR register have the following meaning:

Bit	Meaning
0	TRIG – Got a trigger.
1	RATE – Got a trigger while a delay or burst was in progress.
2	END_OF_DELAY – a delay cycle has completed.
3	END_OF_BURST – a burst cycle has completed.
4	INHIBIT – a trigger or output delay cycle was inhibited.
5	ABORT_DELAY – a delay cycle was aborted early.
6	PLL_UNLOCK – the 100 MHZ PLL came unlocked.
7	RB_UNLOCK – the installed Rb oscillator is unlocked.

Example

INSR?<CR>	A return of ‘5’ would indicate that the DG645 was triggered and a delay cycle completed since the last time this status was queried.

LERR? Last Error

Query the last error in the error buffer. Upon executing a LERR? query, the returned error is removed from the error buffer. See the section Error Codes later in this chapter for a description of the possible error codes returned by LERR?. The error buffer has space to store up to 20 errors. If more than 19 errors occur without being queried, the 20th error will be 254 (Too Many Errors), indicating that errors were dropped.

SHDP?{i} Show Display

Set (query) the on/off state of the display {to i}. If i is 1 the display is turned on. If i is 0, the display is turned off.

TIMB? Timebase

Query the current timebase for the DG645. The returned value identifies the timebase.

Value	Meaning
0	Internal timebase
1	OCXO timebase
2	Rubidium timebase
3	External timebase

Trigger Commands

ADVT(?){i} — **Advanced Triggering Mode Enable**

Set (query) the advanced triggering enable register {to i}. If i is 0, advanced triggering is disabled. If i is 1 advanced triggering is enabled.

HOLD?{t} — **Holdoff**

Set (query) the trigger holdoff {to t}.

Example

HOLD 1e-6<CR> Holdoff triggers for 1 µs after each delay cycle is initiated.

INHB(?){i} — **Inhibit**

Set (query) the trigger inhibit state {to i}. The parameter i may be one of the following:

i	Inhibit
0	Off
1	Triggers
2	AB
3	AB and CD
4	AB, CD, and EF
5	AB, CD, EF, and GH

This command determines the behavior of the rear panel inhibit input. If the rear panel inhibit input is logic high when a trigger is detected, then the given channel delays are inhibited.

Example

INHB 2<CR> Inhibit the AB channel delays if the rear-panel inhibit input is logic high when the trigger was detected.

PHAS(?)i{,j} — **Prescale Phase Factor**

Set (query) the prescale phase factor for channel i {to j}. The parameter i selects the prescaler according to the following table:

i	Prescaler
1	Output AB
2	Output CD
3	Output EF
4	Output GH

The prescale phase factor determines the phase at which the associated output is enabled. The output is enabled when the prescaler counter equals the phase factor.

PRES(?)i{,j} **Prescale Factor**

Set (query) the prescale factor for channel i {to j}. The parameter i selects the prescaler according to the following table:

i	Prescaler
0	Trigger input
1	Output AB
2	Output CD
3	Output EF
4	Output GH

Example

PRES 0,100<CR>	Set the trigger input prescale factor to 100. If prescaling is enabled, every 100th trigger will initiate a delay cycle
PRES 1,5<CR>	Set output AB's prescale factor to 5. If prescaling is enabled, AB's output will be enabled only once every 5 delay cycles.

SPHD i **Step Holdoff**

Step trigger hold off by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SPPH i,j **Step Prescale Phase**

Step the prescale phase factor i by the current step size in the direction j. If j is 1, then step up. If j is 0, then step down. The parameter i selects the prescaler according to the following table:

i	Prescaler
1	Output AB
2	Output CD
3	Output EF
4	Output GH

SPPS i,j **Step Prescale Factor**

Step the prescale factor i by the current step size in the direction j. If j is 1, then step up. If j is 0, then step down. The parameter i selects the prescaler according to the following table:

i	Prescaler
0	Trigger input
1	Output AB
2	Output CD
3	Output EF
4	Output GH

SPTL i **Step Trigger Level**

Step trigger level by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SPTR i **Step Trigger Rate**

Step the internal trigger rate by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SSHD(?){t} **Step Size Trigger Holdoff**

Set (query) current step size for the trigger holdoff {to t}.

SSPH(?)i{,j} **Step Size Prescale Phase Factor**

Set (query) current step size for the prescale phase factor i {to j}.

SSPS(?)i{,j} **Step Size Prescale Factor**

Set (query) current step size for the prescale factor i {to j}.

SSTL(?){v} **Step Size Trigger Level**

Set (query) current step size for the trigger level {to v}.

SSTR(?){f} **Step Size Trigger Rate**

Set (query) current step size for the internal trigger rate {to f}.

TLVL(?){v} **Trigger Level**

Set (query) the trigger level for external triggers {to v}.

TRAT(?){f} **Trigger Rate**

Set (query) the internal trigger rate {to f}.

Example

TRAT 1e3<CR> Set the internal trigger rate to 1 kHz.

TSRC(?){i} **Trigger Source**

Set (query) the trigger source {to i}. The parameter i determines the trigger source according to the following table:

i	Trigger Source
0	Internal
1	External rising edges
2	External falling edges
3	Single shot external rising edges
4	Single shot external falling edges
5	Single shot
6	Line

Example

TSRC 5<CR> Set up the DG645 for single shot triggering.

Burst Commands

BURC(?){i} **Burst Count**

Set (query) the burst count {to i}. When burst mode is enabled, the DG645 outputs burst count delay cycles per trigger.

Example

BURC 10<CR> Set the burst count to 10 so that the DG645 will output 10 delay cycles per triggered burst.

BURD(?){t} **Burst Delay**

Set (query) the burst delay {to t}. When burst mode is enabled the DG645 delays the first burst pulse relative to the trigger by the burst delay.

Example

BURD 5e-6<CR> Set the burst delay to 5 µs so that the DG645 will delay the first cycle of the burst by 5 µs relative to the trigger.

BURM(?){i} **Burst Mode**

Set (query) the burst mode {to i}. If i is 0, burst mode is disabled. If i is 1, burst mode is enabled.

BURP(?){t} **Burst Period**

Set (query) the burst period {to t}. The burst period sets the time between delay cycles during a burst. The burst period may range from 100 ns to 2000 – 10 ns in 10 ns steps.

Example

BURP 1e-3<CR> Set burst period to 1 ms. When a burst is triggered, the DG645 will generate burst count delay cycles at a 1 kHz rate.

BURT(?){i} **Burst T_0 Configuration**

Set (query) the burst T_0 configuration {to i}. If i is 0, the T0 output is enabled for all delay cycles of the burst. If i is 1, the T_0 output is enabled for first delay cycle of the burst only.

SPBC i **Step Burst Count**

Step burst count by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SPBD i **Step Burst Delay**

Step burst delay by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SPBP i **Step Burst Period**

Step burst period by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SSBC(?){i} **Step Size Burst Count**

Set (query) current step size for the burst count {to i}

SSBD(?){t} **Step Size Burst Delay**

Set (query) current step size for the burst delay {to t}.

SSBP(?){t} **Step Size Burst Period**

Set (query) current step size for the burst period {to t}.

Delay and Output Commands

The delay the output commands have parameters which identify the delay channel or output to be modified. Table 31 summarizes how outputs and delay channels are identified in the commands.

Table 31: Delay and Output Parameter Conventions

Parameter	Meaning
b	An output BNC: **Value** **Output** 0 T0 1 AB 2 CD 3 EF 4 GH
c, d	A delay channel: **Value** **Channel** 0 T0 1 T1 2 A 3 B 4 C 5 D 6 E 7 F 8 G 9 H

DLAY(?)c{,d,t} — Delay

Set (query) the delay for channel c {to t relative to channel d}.

Example

DLAY 2,0,10e-6<CR> Set channel A delay to equal channel T0 plus 10 µs.
DLAY 3,2,1e-3<CR> Set channel B delay to equal channel A delay plus 1 ms.
DLAY?3<CR> Query channel B. Should return '2,+0.001000000000' to indicate that B = A + 1 ms.

LAMP(?)b{,v} — Level Amplitude

Set (query) the amplitude for output b {to v}.

Example

LAMP 2,3.5<CR> Set the CD output amplitude to 3.5 V.
LAMP?3<CR> Query the EF output amplitude.

LINK(?)c{,d} — Link Channel

Set (query) the link for channel c {to channel d}. Parameter c can not be T0, and neither channel can be T1.

Example

LINK 3,2<CR>	Link channel B to channel A.
LINK?3<CR>	Query linkage for channel B. Should return 2 to indicate that channel B is linked to channel A.

LOFF(?)b{,v} **Level Offset**

Set (query) the offset for output b {to v}.

Example

LOFF 0,-1.0<CR>	Set the T0 output offset to -1.0 V.
LOFF?1<CR>	Query the AB output offset.

LPOL(?)b{,i} **Level Polarity**

Set (query) the polarity for output b {to i}. If i is 1, the polarity is positive. If i is 0, the polarity is negative.

Example

LPOL 1,0<CR>	Configure the AB output as negative polarity.

SPDL c,i **Step Delay**

Step delay for channel c by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SPLA b,i **Step Level Amplitude**

Step level amplitude for output b by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SPLO b,i **Step Level Offset**

Step level offset for output b by the current step size in the direction i. If i is 1, then step up. If i is 0, then step down.

SSDL(?)c{,f} **Step Size Delay**

Set (query) current step size for channel c delay {to f}.

SSLA(?)b{,v} **Step Size Level Amplitude**

Set (query) current step size for output b level amplitude {to v}.

SSLO(?)b{,v} **Step Size Level Offset**

Set (query) current step size for output b level offset {to v}.

Interface Commands

EMAC? **Ethernet MAC Address**

Query the DG645's Ethernet MAC address.

EPHY(?)i{,j} **Ethernet Physical Layer Configuration**

Set (query) the physical configuration item i {to j}. The parameter i may be one of the following:

i	Configuration
0	Enable/disable Auto-negotiation of link speed
1	Set link speed to 10 Base-T or 100 Base-T

When auto-negotiation is enabled, the manual link speed selection is ignored. When auto-negotiation is disabled, the manual speed selection is used to configure the link. Due to a bug in the silicon for the microprocessor, the auto-negotiation of link speed can fail. To avoid this bug, the DG645 defaults to manually configured 100 Base-T link speed.

Example

EPHYS0,0	Disable auto-negotiation of link speed
EPHYS1,1	Manually configure link for 100 Base-T operation.

IFCF(?)i{,j} Interface Configuration

Set (query) interface configuration parameter i {to j}. The parameter i may be one of the following:

i	Configuration Parameter
0	RS-232 Enable/Disable
1	RS-232 Baud Rate
2	GPIB Enable/Disable
3	GPIB Address
4	LAN TCP/IP Enable/Disable.
5	DHCP Enable/Disable
6	Auto-Ip Enable/Disable
7	Static Ip Enable/Disable
8	Bare Socket Enable/Disable
9	Telnet Enable/Disable
10	VXI-11 Net Instrument Enable/Disable
11	Static IP Address
12	Subnet Address/Network Mask
13	Default Gateway

Set j to 0 to disable a setting and 1 to enable it. Valid RS-232 baud rates include 4800, 9600, 19200, 38400, 57600, and 115200. Valid GPIB addresses are in the range 0–30. Parameters 10–12 require an IP address in the form ‘a.b.c.d’ where each letter is a decimal integer in the range 0–255.

Example

IFCF 6,0<CR>	Disable Auto-Ip
IFCF 1,19200<CR>	Set RS-232 baud rate to 19200
IFCF 3,16<CR>	Set primary GPIB address to 16
IFCF 11,192.168.10.5<CR>	Set IP address to 192.168.10.5
IFCF 12,255.255.255.0<CR>	Set network mask to 255.255.255.0
IFCF 13,192.168.10.1<CR>	Set default gateway to 192.168.10.1

IFRS i Interface Reset

Reset interface i. The parameter i identifies the interface to reset:

i	Interface
0	RS-232
1	GPIB
2	LAN TCP/IP

When an interface is reset all connections on that interface are reset to the power-on state.

LCAL — **Go to Local**

Go back to local control of the instrument. This enables the front-panel key pad for instrument control. This command is only active on telnet and RS-232 connections. The other interfaces have built in functionality for implementing this functionality.

LOCK? — **Request Lock**

Request the instrument lock. The DG645 returns 1 if the lock is granted and 0 otherwise. When the lock is granted, no other instrument interface may alter instrument settings until the lock is released via the UNLK command.

REMT — **Go to Remote**

Enable remote control of the instrument. In this mode, the front panel key pad is disabled, so that control of the instrument can only occur via the remote interface. This command is only active on raw socket, telnet and RS-232 connections. The other interfaces have built in functionality for implementing this functionality.

UNLK? — **Release Lock**

Release the instrument lock previously acquired by the LOCK? command. Returns 1 if the lock was released, otherwise 0.

XTRM i{,j,k} — **Interface Terminator**

Set the interface terminator that is appended to each response to i, j, k. The default terminator is 13, 10.

Status Byte Definitions

The DG645 reports on its status by means of the serial poll status byte and two event status registers: the standard event status (*ESR) and the instrument event status (INSR). These read-only registers record the occurrence of defined events inside the DG645. If the event occurs, the corresponding bit is set to one. Bits in the status registers are latched. Once an event bit is set, subsequent state changes do not clear the bit. Bits are cleared when the registers are queried, with a *ESR?, for example. The bits are also cleared with the clear status command, *CLS. The bits are not cleared, however, with an instrument reset (*RST) or a device clear.

Each of the DG645's event status registers has an associated enable register. The enable registers control the reporting of events in the serial poll status byte (*STB). If a bit in the event status register is set and its corresponding bit in the enable register is set, then the summary bit in the serial poll status byte (*STB) will be set. The enable registers are readable and writable. Reading the enable registers or clearing the status registers does not clear the enable registers. Bits in the enable registers must be set or cleared explicitly. To set bits in the enable registers, write an integer value equal to the binary weighted sum of the bits you wish to set.

The serial poll status byte (*STB) also has an associated enable register called the service request enable register (*SRE). This register functions in a similar manner to the other enable registers, except that it controls the setting of the master summary bit (bit 6) of the serial poll status byte. It also controls whether the DG645 will issue a request for service on the GPIB bus.

Serial Poll Status Byte

Bit	Name	Meaning
0	INSB	An unmasked bit in the instrument status register (INSR) has been set.
1	BUSY	Set if a delay cycle is in progress. Otherwise cleared.
2	BURST	Set if a burst cycle is in progress. Otherwise cleared.
3	Reserved	
4	MAV	The interface output buffer is non-empty.
5	ESB	An unmasked bit in the standard event status register (*ESR) has been set.
6	MSS	Master summary bit. Indicates that the CG635 is requesting service because an unmasked bit in this register has been set.
7	Reserved	

The serial poll status byte may be queried with the *STB? command. The service request enable register (*SRE) may be used to control when the DG645 asserts the request-for-service line on the GPIB bus.

Standard Event Status Register

Bit	Name	Meaning
0	OPC	Operation complete. All previous commands have completed. See command *OPC.
1	Reserved	
2	QYE	Query error occurred.
3	DDE	Device dependent error.
4	EXE	Execution error. A command failed to execute correctly because a parameter was out of range.
5	CME	Command error. The parser detected a syntax error
6	Reserved	
7	PON	Power on. The CG635 has been power cycled.

The standard event status register may be queried with the *ESR? command. The standard event status enable register (*ESE) may be used to control the setting of the ESB summary bit in the serial poll status byte.

Instrument Status Register

Bit	Name	Meaning
0	TRIG	A trigger has been detected.
1	RATE	A trigger was detected while a delay or burst cycle was in progress.
2	END_OF_DELAY	A delay cycle has completed.
3	END_OF_BURST	A burst of delay cycles has completed.
4	INHIBIT	A delay cycle was inhibited.
5	ABORT_DELAY	A delay cycle was aborted prematurely in order to change instrument delay settings.
6	PLL_UNLOCK	The 100 MHz PLL came unlocked.
7	RB_UNLOCK	The Rb timebase came unlocked.

The instrument status register may be queried with the INSR? command. The instrument status enable register (INSE) may be used to control the setting of the INSB summary bit in the serial poll status byte.

Error Codes

The DG645 contains an error buffer that may store up to 20 error codes associated with errors encountered during power-on self tests, command parsing, or command execution. The ERR LED will be highlighted when a remote command fails for any reason. The errors in the buffer may be read one by one by executing successive LERR? commands. The user may also view the errors from the front panel by pressing the keys 'SHIFT', 'STATUS', sequentially, followed by MODIFY ▲ until the display reads 'Error Status.' Finally, press 'STATUS' successively to view the error count and individual errors. The ERR LED will go off when all errors have been retrieved.

The meaning of each of the error codes is described below.

Execution Errors

0 **No Error**

No more errors left in the queue.

10 **Illegal Value**

A parameter was out of range.

11 **Illegal Mode**

The action is illegal in the current mode. This might happen, for instance, if a single shot is requested when the trigger source is not single shot.

12 **Illegal Delay**

The requested delay is out of range.

13 **Illegal Link**

The requested delay linkage is illegal.

14 **Recall Failed**

The recall of instrument settings from nonvolatile storage failed. The instrument settings were invalid.

15 **Not Allowed**

The requested action is not allowed because the instrument is locked by another interface.

16 **Failed Self Test**

The DG645 self test failed.

17 **Failed Auto Calibration**

The DG645 auto calibration failed.

Query Errors

30 **Lost Data**

Data in the output buffer was lost. This occurs if the output buffer overflows, or if a communications error occurs and data in output buffer is discarded.

32 **No Listener**

This is a communications error that occurs if the DG645 is addressed to talk on the GPIB bus, but there are no listeners. The DG645 discards any pending output.

Device Dependent Errors

40 **Failed ROM Check**

The ROM checksum failed. The firmware code is likely corrupted.

41 **Failed Offset T0 Test**

Self test of offset functionality for output T0 failed.

42 **Failed Offset AB Test**

Self test of offset functionality for output AB failed.

43 **Failed Offset CD Test**

Self test of offset functionality for output CD failed.

44 **Failed Offset EF Test**

Self test of offset functionality for output EF failed.

45 **Failed Offset GH Test**

Self test of offset functionality for output GH failed.

46 **Failed Amplitude T0 Test**

Self test of amplitude functionality for output T0 failed.

47 **Failed Amplitude AB Test**

Self test of amplitude functionality for output AB failed.

48 **Failed Amplitude CD Test**

Self test of amplitude functionality for output CD failed.

49 **Failed Amplitude EF Test**

Self test of amplitude functionality for output EF failed.

50 **Failed Amplitude GH Test**

Self test of amplitude functionality for output GH failed.

51 **Failed FPGA Communications Test**

Self test of FPGA communications failed.

52 **Failed GPIB Communications Test**

Self test of GPIB communications failed.

53 **Failed DDS Communications Test**

Self test of DDS communications failed.

54 **Failed Serial EEPROM Communications Test**

Self test of serial EEPROM communications failed.

55 **Failed Temperature Sensor Communications Test**

Self test of the temperature sensor communications failed.

56 **Failed PLL Communications Test**

Self test of PLL communications failed.

57 **Failed DAC 0 Communications Test**

Self test of DAC 0 communications failed.

58 **Failed DAC 1 Communications Test**

Self test of DAC 1 communications failed.

59 **Failed DAC 2 Communications Test**

Self test of DAC 2 communications failed.

60 **Failed Sample and Hold Operations Test**

Self test of sample and hold operations failed.

61 **Failed Vjitter Operations Test**

Self test of Vjitter operation failed.

62 **Failed Channel T0 Analog Delay Test**

Self test of channel T0 analog delay failed.

63 **Failed Channel T1 Analog Delay Test**

Self test of channel T1 analog delay failed.

64 **Failed Channel A Analog Delay Test**

Self test of channel A analog delay failed.

65 **Failed Channel B Analog Delay Test**

Self test of channel B analog delay failed.

66 **Failed Channel C Analog Delay Test**

Self test of channel C analog delay failed.

67 **Failed Channel D Analog Delay Test**

Self test of channel D analog delay failed.

68 **Failed Channel E Analog Delay Test**

Self test of channel E analog delay failed.

69 **Failed Channel F Analog Delay Test**

Self test of channel F analog delay failed.

70 **Failed Channel G Analog Delay Test**

Self test of channel G analog delay failed.

71 **Failed Channel H Analog Delay Test**

Self test of channel H analog delay failed.

80 **Failed Sample and Hold Calibration**

Auto calibration of sample and hold DAC failed.

81 **Failed T0 Calibration**

Auto calibration of channel T0 failed.

82 **Failed T1 Calibration**

Auto calibration of channel T1 failed.

83 **Failed A Calibration**

Auto calibration of channel A failed.

84 **Failed B Calibration**

Auto calibration of channel B failed.

85 **Failed C Calibration**

Auto calibration of channel C failed.

86 **Failed D Calibration**

Auto calibration of channel D failed.

87 **Failed E Calibration**

Auto calibration of channel E failed.

88 **Failed F Calibration**

Auto calibration of channel F failed.

89 **Failed G Calibration**

Auto calibration of channel G failed.

90 **Failed H Calibration**

Auto calibration of channel H failed.

91 **Failed Vjitter Calibration**

Auto calibration of Vjitter failed.

Parsing Errors

110 **Illegal Command**

The command syntax used was illegal. A command is normally a sequence of four letters, or a '*' followed by three letters.

111 **Undefined Command**

The specified command does not exist.

112 **Illegal Query**

The specified command does not permit queries

113 **Illegal Set**

The specified command can only be queried.

114 **Null Parameter**

The parser detected an empty parameter.

115 **Extra Parameters**

The parser detected more parameters than allowed by the command.

116 **Missing Parameters**

The parser detected missing parameters required by the command.

117 **Parameter Overflow**

The buffer for storing parameter values overflowed. This probably indicates a syntax error.

118 **Invalid Floating Point Number**

The parser expected a floating point number, but was unable to parse it.

120 **Invalid Integer**

The parser expected an integer, but was unable to parse it.

121 **Integer Overflow**

A parsed integer was too large to store correctly.

122 Invalid Hexadecimal

The parser expected hexadecimal characters but was unable to parse them.

126 Syntax Error

The parser detected a syntax error in the command.

Communication Errors

170 Communication Error

A communication error was detected. This is reported if the hardware detects a framing, or parity error in the data stream.

171 Over run

The input buffer of the remote interface overflowed. All data in both the input and output buffers will be flushed.

Other Errors

254 Too Many Errors

The error buffer is full. Subsequent errors have been dropped.

DG535 Compatibility

The DG645 is not generally compatible with the DG535. Users that require complete DG535 compatibility should purchase a DG535. The architecture of the two instruments is too different to enable full compatibility. In particular, the DG645 front-panel outputs have two delays associated with them rather than one and a total of 8 delays rather than 4. In the DG645 all outputs should be terminated into 50 Ω, while the DG535 could be configured for either 50 Ω or high impedance terminations. The DG535 trigger input supports 50 Ω termination, but the DG645 does not.

Nevertheless, the DG645 does support a subset of the DG535 command set with the following assumptions and limitations:

1. The 8-channel rear-panel option is assumed to be installed.

2. Outputs A, B, C, and D of the DG535 map to the DG645 rear-panel outputs.

3. Outputs T0, AB, and CD of the DG535 map to the same outputs on the DG645. The negative polarity versions of AB and CD map to outputs EF and GH, respectively.

4. All output configuration commands to A, B, C, and D are silently ignored.

5. Outputs T0, AB, and CD are assumed to be in variable mode. The level offset, amplitude, and polarity commands are supported, but the termination is always 50 Ω.

6. Trigger input terminations is always forced to be high impedance.

Most of the DG535's delay, trigger, and burst configuration commands are supported. The architecture of the burst generators for the two instruments is dramatically different, but the DG645 will mimic the DG535 behavior as best it can.

Generally speaking, one can expect that simple programs written for the DG535 that use TTL levels, and scan delays will work on the DG645. More complex programs that require output configuration will not.

Example Programming Code

The following program can be used as sample code for communicating with the DG645 over TCP/IP. The program is written in the C language and should compile correctly on a Windows based computer. It could be made to work on other platforms with minor modifications. In order to use the program, you will need to connect the DG645 to your LAN and configure it with an appropriate IP address. Contact your network administrator for details on how to do this. To identify the DG645's current IP address from the front panel press 'SHIFT', 'STATUS', MODIFY ▲, 'STATUS', 'STATUS', 'STATUS'.

Copy the program into a file named "dg_ctrl.c". To avoid typing in the program manually, download the electronic version of this manual from the SRS website (www.thinksrs.com). Select the program text and copy/paste it into the text editor of your choice. Compile the program into the executable "dg_ctrl.exe". At the command line type something like the following:

```
dg_ctrl 192.168.0.5
```

where you will replace "192.168.0.5" with the IP address of the DG645. You should see the something like the following:

```
Connection Succeeded
Stanford Research Systems,DG645,s/n001013,ver1.00.10A
Closed connection
```

The program connects to the DG645 at the supplied IP address sets several parameters and then closes. If successful, the trigger mode should be set to internal with a 2 kHz rate. Delay A should be 10 µs and B should be set to A + 1 µs.

```
/* dg_ctrl.c : Sample program for controlling the DG645 via TCP/IP */
#include "Winsock2.h"
#include <stdio.h>

/* prototypes */
void init_tcpip(void);
int dg_connect(unsigned long ip);
int dg_close(void);
int dg_write(char *str);
int dg_read(char *buffer, unsigned num);

SOCKET sDG645;               /* DG645 tcpip socket */
unsigned dg_timeout = 3000;  /* Read timeout in milliseconds */

int main(int argc, char * argv[])
{
  char buffer[1024];

  /* Make sure ip address is supplied on the command line */
  if ( argc < 2 ) {
    printf("Usage: dg_ctrl IP_ADDRESS\n");
    exit(1);
  }

  /* Initialize the sockets library */
  init_tcpip();

  /* Connect to the dg645 */
  if ( dg_connect( inet_addr(argv[1]) ) ) {
    printf("Connection Succeeded\n");

    /* Get identification string */
    dg_write("*idn?\n");
    if ( dg_read(buffer,sizeof(buffer)) )
      printf(buffer);
    else
      printf("Timeout\n");
    /* Load default settings */
    dg_write("*rst\n");
    /* Set internal triggering */
    dg_write("tsrc 0\n");
    /* Set trigger rate to 2kHz */
    dg_write("trat 2000\n");
    /* Set A = 0 + 10 us */
    dg_write("dlay 2,0,10e-6\n");
    /* Set B = A + 1 us */
    dg_write("dlay 3,2,1e-6\n");
    /* Make sure all commands have executed before closing connection */
    dg_write("*opc?\n");
    if ( !dg_read(buffer,sizeof(buffer)) )
      printf("Timeout\n");
    /* Close the connection */
    if (dg_close())
      printf("Closed connection\n");
    else
      printf("Unable to close connection");
  }
  else
    printf("Connection Failed\n");

      return 0;
}
```

```
void init_tcpip(void)
{
  WSADATA wsadata;
  if ( WSAStartup(2, &wsadata) != 0 ) {
    printf("Unable to load windows socket library\n");
    exit(1);
  }
}

int dg_connect(unsigned long ip)
{
  /* Connect to the DG645 */
  struct sockaddr_in intrAddr;
  int status;

  sDG645 = socket(AF_INET,SOCK_STREAM,0);
  if ( sDG645 == INVALID_SOCKET )
    return 0;

  /* Bind to a local port */
  memset(&intrAddr,0,sizeof(intrAddr));
  intrAddr.sin_family = AF_INET;
  intrAddr.sin_port = htons(0);
  intrAddr.sin_addr.S_un.S_addr = htonl(INADDR_ANY);
  if ( SOCKET_ERROR == bind(sDG645,(const struct sockaddr *)&intrAddr,sizeof(intrAddr)) ) {
    closesocket(sDG645);
    sDG645 = INVALID_SOCKET;
    return 0;
  }

  /* Setup address for the connection to dg on port 5025 */
  memset(&intrAddr,0,sizeof(intrAddr));
  intrAddr.sin_family = AF_INET;
  intrAddr.sin_port = htons(5025);
  intrAddr.sin_addr.S_un.S_addr = ip;
  status = connect(sDG645,(const struct sockaddr *)&intrAddr,sizeof(intrAddr));
  if ( status ) {
    closesocket(sDG645);
    sDG645 = INVALID_SOCKET;
    return 0;
  }
  return 1;
}

int dg_close(void)
{
  if ( closesocket(sDG645) != SOCKET_ERROR )
    return 1;
  else
    return 0;
}

int dg_write(char *str)
{
  /* Write string to connection */
  int result;

  result = send(sDG645,str,(int)strlen(str),0);
  if ( SOCKET_ERROR == result )
    result = 0;
  return result;
}
```

```
int dg_read(char *buffer, unsigned num)
{
  /* Read up to num bytes from connection */
  int count;
  fd_set setRead, setWrite, setExcept;
  TIMEVAL tm;

  /* Use select() so we can timeout gracefully */
  tm.tv_sec = dg_timeout/1000;
  tm.tv_usec = (dg_timeout % 1000) * 1000;

  FD_ZERO(&setRead);
  FD_ZERO(&setWrite);
  FD_ZERO(&setExcept);
  FD_SET(sDG645,&setRead);
  count = select(0,&setRead,&setWrite,&setExcept,&tm);
  if ( count == SOCKET_ERROR ) {
    printf("select failed: connection aborted\n");
    closesocket(sDG645);
    exit(1);
  }
  count = 0;
  if ( FD_ISSET(sDG645,&setRead) ) {
    /* We've received something */
    count = (int)recv(sDG645,buffer,num-1,0);
    if ( SOCKET_ERROR == count ) {
      printf("Receive failed: connection aborted\n");
      closesocket(sDG645);
      exit(1);
    }
    else if (count ) {
      buffer[count] = '\0';
    }
    else {
      printf("Connection closed by remote host\n");
      closesocket(sDG645);
      exit(1);
    }
  }

  return count;
}
```

DG645 Calibration

Calibration Bytes

The DG645 has hundreds of bytes of calibration data which are determined when the instrument is calibrated at the factory. Most of these calibration bytes will never need to be adjusted; they correct for unit-to-unit variations which will not change with aging. All the calibration bytes are stored in nonvolatile serial EEPROM.

Calibration bytes are accessed via commands sent over a remote interface. The commands and the calibration bytes are discussed in detail below.

Automatic Delay Calibration

The sample and hold DAC, Vjitter, and all 10 channels of analog delay can be automatically calibrated by running the self calibration routine. This may be accomplished by executing the following command:

***CAL?** **Automatic Calibration**

Runs the instrument auto calibration routine and returns 0 if successful and 17 (EXE_FAIL_AUTO_CAL) if unsuccessful. If unsuccessful, the error buffer will include device dependent errors related to the parts of the self test that failed.

The automatic calibration may also be executed from the front panel by pressing the keys ‘SHIFT’, ‘CAL’, ‘ENTER.’

Timebase Calibration

There is one cal byte for setting the frequency of the DG645’s installed timebase. The cal byte is accessed with the following command:

CALT(?)0{,i} **Calibrate Timebase**

Set (query) the timebase calibration byte.

This cal byte can also be access from the front panel by pressing the keys: ‘SHIFT’, ‘CAL’, ‘CAL.’ The display should show ‘CAL CLOCK 2094.’ Use the MODIFY ▲ and ▼ keys or the numeric key pad to change the current setting.

The DG645 may have one of three different timebases installed: a standard timebase, an OCXO, or a rubidium oscillator. In order to calibrate the DG645’s timebase, the technician must compare it to a reference timebase with superior accuracy. If a rubidium is installed, the reference will likely have to be of cesium quality.

The procedure is to adjust CALT to calibrate the frequency.

1. Be certain that the DG645 has been operating continuously for at least 2 hours for the standard and OCXO timebases, and at least 24 hours for a rubidium timebase. Also make sure that nothing is connected to the rear panel 10 MHz input.

2. Connect the reference to the timebase input of a frequency counter with sufficient resolution and accuracy to perform the measurement. The SR620 Time Interval Counter, for example, will work.

3. Connect the DG645 10 MHz output on the rear panel to the frequency input of the frequency counter.

4. Set the counter to frequency mode with a gate of 10 s for the standard and OCXO timebases, and 100 s for a rubidium timebase.

5. Record the current value of CALT so that you can return to the current calibration if needed. Next adjust CALT until the frequency counter measures 10 MHz to the desired accuracy.

Output Level Calibration

NOTE: This calibration will not be required in most circumstances. Output level calibration may be desired after repair of an output driver.

The DG645 has five front-panel outputs: T0, AB, CD, EF, and GH. Each output has four cal bytes associated with it: offset intercept, offset slope, amplitude intercept, and amplitude slope. These cal bytes correct for deviations from nominal circuit operation.

The calibration bytes for output levels are accessed with the following command:

CALL(?)i{,j} **Calibrate Level**

Set (query) the i^{th} calibration byte {to j}. The parameter i may be one of the following:

i	Calibration Byte
0	T0 offset intercept
1	T0 offset slope
2	T0 amplitude intercept
3	T0 amplitude slope
4	AB offset intercept
5	AB offset slope
6	AB amplitude intercept
7	AB amplitude slope
8	CD offset intercept
9	CD offset slope
10	CD amplitude intercept
11	CD amplitude slope
12	EF offset intercept
13	EF offset slope
14	EF amplitude intercept
15	EF amplitude slope

16 GH offset intercept
17 GH offset slope
18 GH amplitude intercept
19 GH amplitude slope

Offset Calibration

The DG645 output offset can range over ±2 V. Calibration bytes, offset intercept and offset slope, correct the output offset voltage for deviations from nominal operation. To calibrate the offset voltage, follow this procedure:

1. Reset the DG645 by pressing the keys ‘SHIFT’, ‘0’, ‘ENTER’ sequentially.
2. Press ‘LEVEL’ to select the level menu.
3. Press the EDGE ◄ and ► keys to select the offset voltage of the channel to be calibrated.
4. Connect the channel to be calibrated to a 4-digit or better voltmeter and terminate it into 50 Ω.
5. Set the front-panel output offset to +2.00 V and record the measured voltage V_PLUS. Then set the front-panel output offset to −2.00 V and record the measured voltage V_MINUS.
6. Adjust the offset intercept calibration byte for the output and repeat step 5 until the recorded voltages satisfy the relation: V_PLUS + V_MINUS = 0.000 V
7. Adjust the offset slope calibration byte for the output and repeat step 5 until the recorded voltages satisfy the relation V_PLUS − V_MINUS = 4.000 V

Amplitude Calibration

The DG645 output amplitude can range from 0.5 to 5.0 V. Calibration bytes, amplitude intercept and amplitude slope, correct the output amplitude step for deviations from nominal operation. The output driver has a significant temperature coefficient that limits the accuracy with which the amplitude can be calibrated. The output amplitude will drift by 50 mV or more at full duty cycle, compared to the same amplitude measured at low duty cycle. We expect that most users will operate at low duty cycle. Therefore, the calibration is performed with low duty cycle pulses, rather than at DC. Follow the procedure below to calibrate the amplitude step for channels T0, AB, CD, EF, and GH.

1. Reset the DG645 by pressing the keys ‘SHIFT’, ‘0’, ‘ENTER’ sequentially.
2. Press Trigger ▲ 5 times to select internal triggering.
3. Press ‘1’, ‘0’, ‘Hz’ sequentially to set the trigger rate to 10 Hz.
4. Press ‘Delay’ to switch to the delay menu.
5. Press EDGE ► to select channel B.

6. Press ‘1’, ‘ms’ to set the delay to 1 ms relative to channel A.

7. Press ‘SHIFT’, ‘1’, ‘ENTER’ to copy AB settings to all other channels.

8. Press ‘LEVEL’ to switch to the level menu.

9. Press the EDGE ◄ and ► keys to select the step voltage of the channel to be calibrated.

10. Connect the channel to be calibrated to a voltmeter and terminate it into 50 Ω. The voltmeter should have 4 digit or better accuracy. It should be configured for external triggers and to complete measurements within 1 ms of the trigger.

11. Connect one of the other DG645 outputs to the external trigger input of the voltmeter.

12. Set the front-panel output amplitude to 1.50 V and record the measured voltage V_LOW. Then set the front panel output amplitude to 4.50 V and record the measured voltage V_HIGH.

13. Adjust the amplitude intercept calibration byte and repeat step 12 until the recorded voltages satisfy the relation: 3 × V_LOW = V_HIGH.

14. Adjust the amplitude slope calibration byte and repeat step 12 until the recorded voltages satisfy the relation: V_HIGH − V_LOW = 3.0 V.

Trigger Threshold Calibration

NOTE: This calibration will not be required in most circumstances. Trigger threshold calibration may be desired after repair of the trigger input circuitry.

The DG645 can trigger be externally triggered at voltage thresholds that range over ±3.5 V.

The calibration bytes for trigger threshold levels are accessed with the following command:

CALL(?)i{,j} **Calibrate Level**

Set (query) the i^{th} calibration byte {to j}. The parameter i may be one of the following:

i	Calibration Byte
20	Positive trigger intercept
21	Positive trigger slope
22	Negative trigger intercept
23	Negative trigger slope

To calibrate the trigger threshold use the following procedure:

1. Reset the DG645 by pressing the keys ‘SHIFT’, ‘0’, ‘ENTER’ sequentially.

2. Press Trigger ▲ 4 times to select external triggering on rising edges.
3. Press ‘0’, ‘ENTER’ sequentially to set the trigger threshold to 0.0 V.
4. Ground the trigger input with a 50 Ω terminator.
5. Set positive intercept to 200.
6. Set the positive intercept to 20.
7. Decrease the positive intercept by single steps until the TRIG’D LED flashes. Then increase the positive intercept by one.
8. Press Trigger ▼ once to select external triggering on rising edges.
9. Set the negative intercept to −200.
10. Set the negative intercept to −20.
11. Increase the negative intercept by single steps until the TRIG’D LED flashes. Then decrease the negative intercept by one.
12. Press Trigger ▲ once to select external triggering on rising edges.
13. Press ‘3’, ‘.’, ‘5’, ‘ENTER’ sequentially to set the trigger threshold to 3.5 V.
14. Remove the 50 Ω terminator, and apply 3.5 VDC to the trigger input.
15. Set the positive trigger slope calibration byte to 3000.
16. Set the positive trigger slope to 2000. And then decrease it by steps of 200 until the TRIG’D LED flashes. Record the trigger value, COARSE_SLOPE.
17. Set the positive trigger slope back to 3000 and then to COARSE_SLOPE + 200.
18. Decrease the positive trigger slope by steps of 20 until the TRIG’D LED flashes and then increase it by 20.
19. Set the negative trigger slope calibration byte to the same value as the positive trigger slope calibration byte.

Circuit Description

Overview

The DG645 builds upon the legacy of the original DG535, while doubling the number of timing channels, improving the jitter, and implementing a Direct Digital Synthesizer (DDS) for the rate generator. Basic timing diagrams for delays and bursts generated by the DG645 are shown in Figure 13 and Figure 14.

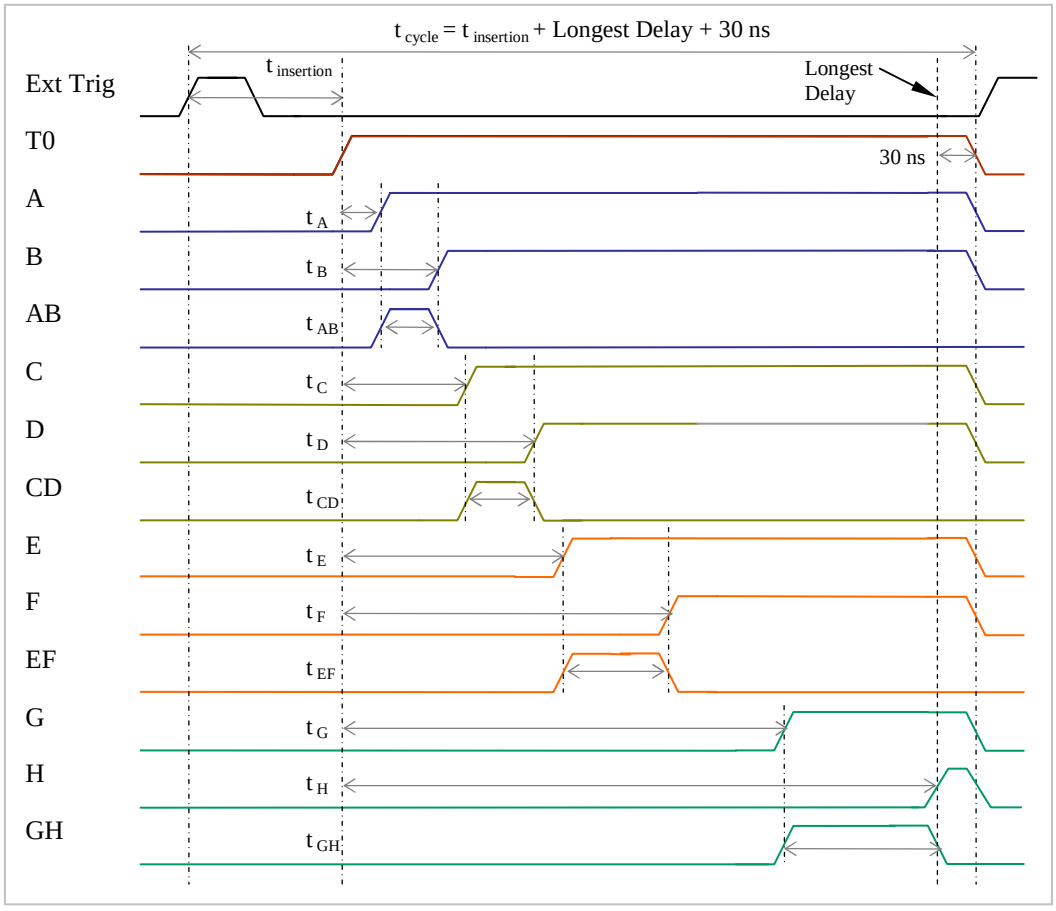

Figure 13: Channel Timing

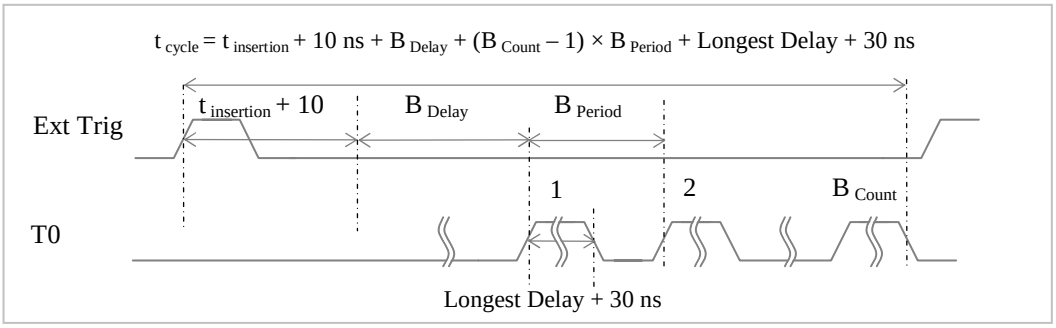

Figure 14: Burst Timing

The DG645 is comprised of a number of PCBs (power supply, display, amplifiers, optional oscillator, …) that interconnect through a motherboard. The motherboard is comprised of numerous internal sub-systems (timebase, microcontroller, ...)

At the heart of the DG645, all delays are comprised of two components: (1) A coarse 39-bit digital 10 ns component, and (2) a fine 12-bit analog 5 ps component. The coarse component is implemented in the FPGA, and the fine component is implemented in the verniers. This allows the generation of delays with durations of 2000 s and 5 ps resolution.

The schematics are drawn in a two level hierarchy to reflect the “modules” in a logical and (relatively) sequential fashion.

The DG_MB_BLOCK is the top level drawing and contains all external and PCB to PCB connectors. It has various functional blocks (microcontroller, FPGA, etc.).

The DG_MB_CPU is the central module. This contains the microcontroller, U50, which is the “brains” of the DG645. It interfaces to all systems components (DDS, PLL), PCBs (display, outputs), as well as the various external interfaces (RS-232, Ethernet, GPIB).

Most communication both within and between PCBs is accomplished using the native serial peripheral interface (SPI) present on the microcontroller. To reduce the interference of data transfers into various modules, the raw SPI is buffered and gated by the FPGA to all modules except the display. The GPIB uses a byte bus comprised of general purpose I/O pins on the microcontroller.

The DG_MB_FPGA implements the bulk of moderate speed logic contained in the DG645 (local SPI interface, counters, state machines), and sits between the time-to-amplitude converter (TAC) and the verniers. The FPGA implements ten 39-bit coarse delay channels, with 10 ns resolution.

The DG_MB_TIMEBASE generates the master 100 MHz clock. It also contains circuitry allowing the master clock to be locked to internal or external sources.

The DG_MB_TRIG implements a DDS synthesizer and trigger select logic (External, Line, DDS) and routes the source to the TAC.

The DG_MB_TAC implements (in conjunction with the verniers) synchronization of the trigger and the 100 MHz timebase, and in turn triggers the FPGA to begin the counting.

The DG_MB_VERNIER_xys works in conjunction with the TAC to eliminate trigger jitter. They also allow 12-bit analog delays of up to 9.995 ns at 5 ps resolution.

The DG_MB_CHANNEL_LOGIC_xx processes the resulting edges from the verniers into waveforms useful for the output amplifiers, and allow polarity control and gating. The channel logic drives the front- and rear-panel output amplifier boards. These circuits generate the five combined widths (T0, AB, CD, EF, and GH) and the nine discrete edges (T0, A, B, C, D, E, F, G, and H)

The DG_MB_GPIB implements the IEEE-488 compliant interface.

The DG_MB_PSIO implements decoupling and post regulation of the master power supply inputs. This sheet implements the regulators used in the analog portion of the circuitry—+12VA, +3.3VA, +2.5VA, and the +4.096VREF supplies. It also implements a power supply monitor to notify the microcontroller in the event that the power is removed or the DG645 is switched 'OFF'.

Block Diagram and IO

Schematic sheet "DG_MB_BLOCK"

This diagrams all of the connectors for interfacing to the various sub-systems and blocks that represent the modules contained within the motherboard. Certain modules are repeated (verniers and waveform conditioning). Where possible the interconnections between modules are directly connected.

External and PCB Interfaces

Table 32 summarizes the various connectors and their function. The first five items interconnect the other PCBs in the DG645 with the motherboard. The last seven items are external interfaces.

Table 32: Connectors

Connector	Type	Description
J4	HEADER 7 X 1 X 0.1"	Display keypad PCB
J6	HEADER 20 X 2 X 0.1"	Main pulse output PCB
J11	HEADER 13 X 1 X 0.156"	Power supply PCB
J7	HEADER 10 X 1 X 0.156"	(Optional) oscillator PCB(s)
J8	HEADER 18 X 2 X 0.1"	(Optional) rear pulse output PCB(s)
J10	DPDT	Power switch
J3	D-24	GPIB
J2	DB-9	RS-232
J10	RJ45	Ethernet
J5	BNC	10MHz reference out
J9	BNC	10MHz reference in
J1	BNC	Trigger inhibit

Display PCB – J4

The display-keyboard interface utilizes the SPI for communication. The display-keyboard is time-multiplexed, has nineteen digits, thirty seven lamps, 30 keys, and an audio buzzer (piezo-electric device).

The display is time-multiplexed at an interval of 2.5 ms (400 Hz), with six time slots: five used for continuous digit scanning, and the sixth used for highlighting a selected digit. The digits and lamps are displayed and the key-pad scanned in a similar method. This produces a complete display scan once every 15 ms (66.7 Hz).

To further enhance the tactile feedback a key-pad assertion, the audio beeper is excited. This has a dedicated signal line (not via the SPI) that is edge sensitive and fires the buzzer for a fixed duration of 2 ms.

The pin out for the display connector is shown in Table 33.

Table 33: Display Connector

Pin	Function
1	+5V
2	Audio Buzzer
3	Serial Data Input
4	Serial Clock
5	Serial Chip Select
6	Serial Data Output
7	Ground

Main Pulse Output PCB – J6

The main output PCB supports five output drivers that may be programmed for offset and step. The external trigger discriminator and edge selection is also implemented on this PCB.

Communication is implemented using the SPI. However, in order to minimize noise in the outputs, it is buffered and gated through the FPGA.

The five pulse outputs are replicated from LVDS signals (T0/AB/CD/EF/GH).

Additionally, the external discriminator is located on the PCB and is brought in through the LVDS signals Ext_Trig.

The pin-out for the main pulse output is shown in Table 34.

Table 34: J6 Main Pulse Output PCB

Pin	Function			Pin
1	Serial Chip Select	SPI	Serial Clock	2
3	Serial Data Output		Serial Data Input	4
5	4.096VREF		Level Monitor	6
7		GND		8
9	Ext Trig +	LVDS Input	Ext Trig -	10
11		GND		12
13	T0 +	LVDS Output	T0 -	14
15		GND		16
17	AB +	LVDS Output	AB -	18
19		GND		20
21	CD +	LVDS Output	CD -	22
23		GND		24
25	EF +	LVDS Output	EF -	26
27		GND		28
29	GH +	LVDS Output	GH -	30
31		GND		32
33		+15		34
35				36
37	+5V		-5V	38
39		-15		40

Power Supply – J11

Table 35 summarizes the power supply interface which delivers the power rails +/-HV, +/-15, +/-5, and +3.3V. Additional signals support line trigger, synchronizing the supply's switching frequency to our timebase, and power enable (from the front-panel switch).

Table 35: J11 Power Supply Connector

Pin	Function
1	Ground (Analog)
2	LINE_TRIG
3	SYNC
4	POWER_EN
5	-15VA
6	-5VA
7	+3.3VD
8	+5VA
9	+15VA
10	+24V
11	-HV
12	+HV
13	Ground (Digital)

Optional Oscillator Connector – J7

This connector provides a unified interface to either of the optional oscillators (ovenized crystal or rubidium). Separate detection is implemented for the two options. The rubidium also has a serial interface for determining its status.

Power is provided by the +24_US, which is present even during times that the front-panel power switch is OFF. This allows the oscillators to remain "warm" even during times when the unit is in the "OFF" state.

The pin out for the optional oscillator is shown in Table 36.

Table 36: J7 Optional Oscillator Connector

Pin	Function
1	TXD
2	CAL_Voltage
3	RXD
4	OCXO_Detect
5	Rubidium_Detect
6	10MHz_Out
7	Ground (Analog)
8	Ground (Power)
9	+24V
10	Ground (Power)

Optional Rear-Panel Pulse Output – J8

This connector provides power, SPI, and the nine LVDS edges to allow generation of pulses on one of the rear-panel output option boards. The pin out for the rear-panel pulse output connector is shown in Table 37.

Table 37: J8 Optional Rear Panel Pulse Output Connector

Pin	Function				Pin
1	T0 +	LVDS	Power	+HV	2
3	T0 -			-HV	4
5		GND	LVDS	A +	6
7				A -	8
9	B +	LVDS	Power	+15V	10
11	B -			-15V	12
13		GND	LVDS	C +	14
15				C -	16
17	D +	LVDS		+5V	18
19	D -			Level Monitor	20
21		GND	LVDS	E +	22
23				E -	24
25	F +	LVDS	SPI	Chip Select	26
27	F -			Data Output	28
29		GND	LVDS	G +	30
31				G -	32
33	H +	LVDS	SPI	Clock	34
35	H -			Data Input	36

Ethernet – J10

This RJ45 connector includes the necessary magnetics and illuminators (link and activity) to support a 10/100-Base-T interface.

RS232 – J2

The rear-panel RS-232 (DCE) utilizes a D-sub 9 female connector. The microcontroller's UART signals are converted between 3.3VCMOS and RS-232 levels by U1 (ADM3202AN). U1 also provides the high levels for the CD and DSR (carrier-detect and data-set-ready) lines on the D-sub-9 connector.

GPIB – J3

This is a standard female IEEE-488 connector.

10 MHz Reference Input – J9

This BNC is where an external 10 MHz 100 to 1000 mV signal may be applied. The input provides a 1 kΩ load.

10 MHz Reference Output – J5

This BNC is the 10 MHz reference output. The output is approximately 1 V_{rms} from 50 Ω.

Trigger Inhibit – J1

This (high true) input is used by the inhibit modes. A signal level greater than 1 V will assert the inhibit function. This provides a 2 kΩ load.

Analog µP Interface

Analog-to-Digital Convertor (ADC)

The ADC (12-bit, 100 kS/s) is provided in the microcontroller and has two 4-channel ports. The first port is assigned to three direct signals and an analog multiplexer. The second port is dedicated to the V_JITTER signal to allow for automatic sampling during a timing cycle. The signal assignments for the ADC are shown in Table 38 and Table 39.

Table 38: ADC Channels

ADC	Channel	Function
A	1	Multiplexed (see table XX)
A	2	Rear Output Pulse Option Detect
A	3	External 10MHz Monitor
A	4	Internal 10MHz Monitor
B	1	V_JITTER
B	2 – 4	Un-assigned

Table 39: ADC Multiplexer Channels

Pin	Function
1	Vernier T0 T1 Calibration
2	Vernier A & B Calibration
3	Vernier C & D Calibration
4	Vernier E & F Calibration
5	Vernier G & H Calibration
6	Front Output Level Monitor
7	100MHz Control Voltage Monitor
8	Un-assigned

Digital-to-Analog Convertor (DAC)

There are three LTC2620 8-channel, 12-bit voltage output DACs (U4, U5, U7). Table 40 summarizes the channel assignments.

Table 40: DAC Channels Assignment

DAC	Channel	Function
U4	A	T0 Vernier Setting
U4	B	T0 Vernier Calibration
U4	C	T1 Vernier Setting
U4	D	T1 Vernier Calibration
U4	E	Insertion Delay
U4	F	Vjitter_3ms_Calibration
U4	G	Oscillator Calibration
U4	H	Vjitter_10us_Calibration
U5	A	A Vernier Setting
U5	B	A Vernier Calibration
U5	C	B Vernier Setting
U5	D	B Vernier Calibration
U5	E	C Vernier Setting
U5	F	C Vernier Calibration
U5	G	D Vernier Setting
U5	H	D Vernier Calibration
U7	A	E Vernier Setting
U7	B	E Vernier Calibration
U7	C	F Vernier Setting
U7	D	F Vernier Calibration
U7	E	G Vernier Setting
U7	F	G Vernier Calibration
U7	G	H Vernier Setting
U7	H	H Vernier Calibration

Microcontroller

Schematic sheet “DG_MB_CPU”

The microcontroller is a 32-bit MCF52235 Coldfire (U50), with reduced instruction set based on the MC68020. The important features used in this design include: (A) 32-bit CPU, (B) 256k bytes of flash ROM for program storage, (C) 32k bytes of RAM for volatile storage, (D) triple serial communication (UARTs), (E) serial peripheral interface (SPI) used for communicating with system components (DAC, NVROM, FPGA…), (F) 16-bit pulse width modulator for extending the resolution of the DDS via its FSK input, (G) two 4-channel 12-bit A/D convertors (ADC) for test and calibration, (H) integrated fast Ethernet controller and on-chip transceiver (Phy) for 10/100 BaseT interface, (I) interrupt controllers and periodic interrupt timer (PIT), (J) software watchdog timer, (K) a myriad of general purpose I/O bits for system control, (L) and an integrated background debug mode (BDM) for in-system programming and chip debugging.

Interface

Power and Control

BDM_xxxx: These are the interface for the background debug mode port (BDM).

RESET_IN_N: Input from the reset switch (SW1). It also is used by the BDM for initialization during debug and flash ROM programming.

RESET_N: This is the system reset output which is derived from RESET_IN_N or the internal watchdog timer.

CLK_25MHZ_CPU: This input is the master clock for the microcontroller. The internal PLL uses this as a reference for the Ethernet as well as generating the internal 60 MHz frequency that the CPU operates at.

Ethernet

RXP, RXN, TXP, TXN: These are the Ethernet transceiver Phy's I/Os on J10.

ACT, LNK: These output signals drive the activity and link LEDs on J10.

GPIB Interface

GPIB_A[4:0]: Outputs for the GPIB controller address (general purpose output).

GPIB_DATA[7:0]: Bidirectional for the GPIB data (general purpose bidirectional).

GPIB_CS_N, GPIB_RE_N, GPIB_WE_N: These general purpose outputs control the exchange of data with the GPIB interface chip (U900).

Interrupts (inputs)

GPIB_IRQ: Interrupt from GPIB.

VCO_LOCK: Input from the PLL (U724) indicating that it has successfully phase-locked the 100 MHz timebase to the selected 10 MHz reference.

IRQ_FPGA_N: Interrupt from the FPGA (U80).

IRQ_P_OFF_N: Interrupt from power monitor (U13). This bit goes low to generate an interrupt when the unit is turned "off" or when the power is removed.

Serial Interfaces

SER0_xyz: These signals are for the rear-panel RS-232 I/O to J2 (via U1).

SER1_xXD: These signals are for serial communication with the optional rubidium oscillator.

ADC Interface

AN0_MUX: This input is multiplexed and allows the eight additional analog signals described in Table 39 to be monitored

10MHZ_EXT_DET: This input (>1.00 V) indicates that a signal has been applied to the rear-panel external reference input, and that the PLL should attempt to lock the 100 MHz timebase to the reference.

10MHZ_INT_DET: This input (>1.00 V) indicates that an optional oscillator is installed, and that PLL should attempt to lock the 100 MHz timebase to it (unless an external reference is applied).

ADC_R_LVL: This input from the optional rear-panel output PCB indicates the presence (< 3.0 V) and type (various) of optional output board.

V_JITTER_ADC: This input monitors the TAC output (level shifted and scaled) for calibration and during time intervals greater than 3 ms.

ANMUX[2:0]: These outputs select the channel routing for the AN0_MUX.

SYNCB_ADC: Input from the FPGA for triggering the ADC sampling of V_JITTER_ADC.

SPI Interface

SPI_MISO, SPI_MOSI, **SPI_SCK**, **SPI_CS [3:0]**: Master SPI interface (data in/out, clock, chip selects).

SPI_BQCS [7:0]: Outputs the decoded SPI chip select for the PLL and DDS chips.

FPGA Initialization

PROG_B: The microcontroller drives this output line low for 2 ms and then releases it to force a reconfiguration of the FPGA (U80).

FPGA_DONE: This input from the FPGA (U80) level indicates that the initial configuration has completed.

Timebase Interface

OCXO_OPT_DET_N: This input is pulled low when the optional oven controlled crystal oscillator (OCXO) timebase is installed. (The active pull-up for this port bit is enabled.)

RB_OPT_DET_N: This input is pulled low when the optional rubidium timebase is installed. (The active pull-up for this port bit is enabled.)

EXT_OPT_N: This output controls which high-precision source (external 10 MHz or internal OCXO or rubidium) is used as a frequency reference for the PLL. The EXT_OPT_N bit is set high to select the external 10 MHz reference or set low to select the optional OCXO or rubidium.

SEL_PLL: This output controls the operation of the 100 MHz timebase. A low level allows the frequency to be controlled by the DAC_CAL_OSC output. A high level will cause the 100 MHz timebase to be phase locked to either the external reference input or to the optional reference (rubidium or OCXO).

DDS Interface

DDS_UPD: This output strobes the DDS (U800) to transfer data from the SPI input registers to working registers.

DDS_FSK: This output is used to extend the resolution of the DDS (U800) from 48 to 64-bits. It is a pulse width modulation signal whose duty cycle is controlled with 16-bits of resolution.

DDS_DIS_CLK: This output disables the 100 MHz into the DDS (U800) for initialization.

RESET: This output is used to initialize DDS (U800).

Miscellaneous

CLICK: This output to the front-panel display excites the audio buzzer on the front panel.

PS_SYNC: This output is a pulse width modulator used to synchronize the switch mode power supply to a sub-harmonic of the master 100 MHz timebase.

TEST_POINT: This is a test point for debug purposes.

Subcircuits

SPI Address Decoding

The SPI chip select lines (SPI_CS [3:0]) are decoded by a 74LVC138 (U8) 3-8 decoder to allow additional devices to be accessed. Table 41 lists the address map.

Table 41: SPI Address Decoding

Address	Device
0	Front Panel Display
1	Front Panel Output
2	Rear Panel Output
3	Temp Sensor
5	Cal DAC 0
6	Cal DAC 1
7	Cal DAC 2
8	FPGA
9	DDS
10	PLL
11	SPI FLASH
15	INACTIVE

ADC Reference Generation

The microcontrollers ADC modules require a precision reference voltage of 3.3 V. To accomplish this, a LMC6035 (U667) translates the +4.096 VREF voltage down to +3.3 V and drives the VRH (Reference High) input of U80.

FPGA

Schematic sheet "DG_MB_FPGA"

The FPGA (U80) is a Xilinx Spartan 3E series device. The device has 250k system gates. It has the equivalent of 1200 flip-flops, multiple clock systems (delay lock loops), and supports 108 I/Os. The device is capable of operating at clock rates > 200 MHz.

The blocks implemented inside the FPGA include: (A) an SPI interface capable of 16-bit multi-word transfers with complete read/write of all registers, (B) a trigger state machine, (C) burst generator – period and count, (D) eleven 39-bit counters operating at 100 MHz for implementing the coarse delays, (E) pulse and trigger prescaling and blanking circuitry, (F) interrupt capture and gating, and more.

The FPGA is diagrammed in six sections: Power, MODE, and logic Banks 0-3. The power section contains all of the supply lines. The MODE section contains all pins associated with configuring the FPGA. The Banks correspond to architectural blocks within the FPGA.

Two voltage regulators are present (U70 and U78) for the 1.2 V core logic supply, and the 2.5 V to support banks that interface to 2.5 V logic.

Additional circuitry is present for generating the 25 MHz clock for the microcontroller, and re-synchronizing and level shifting the timing signals from the FPGA that are fed to the verniers.

The FPGA may be configured using either the JTAG port (via J70) or a 2 Mb SPI flash ROM (U72). The flash is also used as non-volatile storage by the microcontroller calibration coefficients and instrument settings.

Interface

Clock

CLK100MHZ_[7:6]: These LVDS inputs provides the master 100 MHz clock.

SPI Interfaces

SPI_MOSI, SPI_MISO, **SPI_SCK**, **SPI_CS [3:0]**: These signals (data in/out, and clock and chip selects inputs) comprise the SPI interface with the microcontroller.

SPROM_FMISO, SPROM_FMOSI, **SPROM_CCLK**, **SPROM_FCS_N**: These signals (data in/out, and clock and chip select outputs) interface into the SPI flash ROM (U72) and are used during configuration of the FPGA and by the microcontroller for non-volatile memory storage.

SPI_QMISO, SPI_QMOSI, **SPI_QSCK**: These signals (data in/out and clock output) comprise the buffered SPI interface. These are used for all system communications except the front panel.

SPI_BQCS9: This output is the SPI chip select for the DDS.

SPI_BQCS10: This output is the SPI chip select for the PLL.

TAC Interface

TRIG_EN: This output is the main "ARM" used to control whether the TAC should accept triggers.

STOP_RAMP: This output is the trigger (synchronized to the 100 MHz) that initiates counting in the FPGA.

VSH_[4:1]: These outputs sequence the track-and-hold circuit in the TAC as indicated.

VSH_1 closes U601B from PRETRIG TO 3ms

VSH_2 closes U601D from 50us TO END_OF_CYCLE

VSH_3 & VSH_4 closes U601A & C from 3ms TO END_OF_CYCLE

LAST_B_PULSE: This output prevents the clearing of the TAC during burst cycle.

CLEAR_CYCLE_N: This output forces the TAC to an OFF state.

INH_EN: This output enables the rear-panel inhibit signal to gate triggers into the TAC.

TRIG_INH_RT: This input is the rear-panel inhibit (synchronized to the 100 MHz) used by the FPGA to gate the pulses off.

TRIG_INH: This input is the un-synchronized rear-panel inhibit used to distinguish between inhibit and trigger over-range.

TRIG_SOURCE_1: This is a mirror of the TRIG_SOURCE signal.

Trigger and DDS Interface

DDS_RATE: This input is the main DDS synthesized frequency. This ranges from 12.5 to 25 MHz.

DDS_RATE_D_2N: This output is a scaled version of DDS_RATE equal to DDS_RATE/2^N where N is selected to obtain the desired trigger rate.

LINE_OUT: This input signal is from the power supply and is representative of the AC line rate (either 50 or 60 Hz), and is used during the line trigger mode.

LINE_SC: This output is the conjoined Single_Cycle and Line_Trigger signal.

TRIG_SEL[1:0]: These outputs select from the available trigger sources in accordance with Table 42.

Table 42: Trigger Selection

TRIG_SEL1	TRIG_SEL0	Source
1	X	EXT_TRG
0	0	DDS
0	1	LINE / SS

Vernier Interface

EOD_[19:0]: These outputs are the 10 (pairs) of LVDS end of delay signals. They represent the coarse (10 ns) portion of the delay.

Channel Logic Interface

OUT_EN[12:0]: These outputs are used to enable the channel logic to generate waveforms for the output amplifiers. These are cleared at power-on (or reset) to prevent spurious pulses from being generated during application of power. They may also be used to enable outputs on a channel by channel basis and during pulse inhibit.

POL[4:0]: These outputs determine the polarity of the five combinatory outputs (T0, AB, CD, EF, and GH) which drive the front-panel output amplifier interface.

FPGA Internal Subcircuits

SPI Interface

The U50 (microcontroller) uses the SPI as the interface to control the subcircuits in the FPGA. The FPGA's SPI interface can operate at up to 6Mb/s.

The FPGA resides at the SPI address 0x08.

For SPI traffic that is not directed toward the FPGA, the SPI is buffered and gated onto either the SPROM_xxx lines (for flash ROM access) or the SPI _Qxxx lines (for all other system component access).

For SPI traffic into the FPGA, the SPI data input (SPI_MOSI) is received in 2 (or more) 16-bit words. The first word (command word) is specifies the initial address and a conditional write command, with the subsequent data word(s) being destined for the address (and sequential addresses).

The command word has the following format:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	*W*	0	1	0	*X*	*X*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*A*	*X*

Where: W = 1 for write operation A = Address bits X = don't care

Data is output on the SPI_MISO. The data during the command word is undefined. Data for the subsequent word(s) corresponds to the register content at the specified address. If the 'W' bit is not set, no writes will take place.

The following diagrams a typical data transfer.

WORD 1 (command) 2 (data) … n (data)

SPI_MOSI <COM + address> <DATA(address)> … <DATA(address + n − 2)>

SPI_MISO < xxxxxxxx > < REG(address) > … <REG (address + n – 2)>

FPGA Memory Map

The following table lists the addresses of the various register (blocks) available:

Table 43: FPGA Memory Map

Address	Register Block
0x000	Burst Delay
0x004	T0 Delay
0x008	T1 Delay
0x00C	A Delay
0x010	B Delay
0x014	C Delay
0x018	D Delay
0x01C	E Delay
0x020	F Delay
0x024	G Delay
0x028	H Delay
0x040	Burst Period (10 ns)
0x042	Burst Count
0x080	Trigger
0x0C0	Config0
0x0C8	Pulse Enable
0x0D0	Interrupt Control
0x0D8	Interrupt Status
0x0F8	Dynamic
0x100	Status
0x140	Prescalers
0x180	Coincidence
0x1C0	Version

There are 11 **Delay** registers (Burst, T0, T1, A to H). Each is 3 words (39-bits) wide and represents the coarse (10 ns) portion of the delay, allowing for delays of 2000 s.

The **Burst** registers are comprised of a period and count value (each 32-bits). The burst period supports 100 ns to 25 s. The burst count can be set from 1 to 4.2 x 10^9.

The **Trigger** register is comprised of two fields (1) DDS Prescaler and (2) Trigger Select.

The DDS prescaler is a 6-bit value and determines the binary divider applied to the native DDS frequency (12.5-25 MHz). As the prescaler is 40-bits wide with an additional 1-bit implemented outside the FPGA, the lowest achievable frequency is ~6 µHz (12.5 MHz / 2^41).

The Trigger Select field is 3-bits. The two LSBs are output and used for trigger circuit selection multiplexers (U802, U803). The MSB is used internally to select between single cycle and line trigger. Overall trigger selection is summarized in Table 44.

Table 44: Trigger Selection

Trigger Select	Source
0b'X00	DDS
0b'001	SINGLE CYCLE
0b'101	LINE
0b'X1X	EXTERNAL TRIGGER

The **Config0** register is comprised of five polarity bits and three trigger enable bits.

There are 5 polarity bits and they determine the T10, AB, CD, EF, GH polarity. A zero corresponds to normal polarity, while a one is used for inverted polarity. Theses are routed to the DG_MB_CHANNEL_LOGIC_xx (via outputs POL[4:0]).

The TRIGGER bit is routed to the TAC (via EN_TRIG) and enables the TAC to receive triggers.

The BURST bit is used internally to enable the burst generator and condition the trigger state machine.

The INHIBIT bit is routed to the TAC (via INH_EN) and allows the rear-panel inhibit signal to gate trigger cycles.

The **Pulse Enable** register is a dual-function register. There is a global BLANK bit which turns off all pulses. There are also 13 bits which control the individual pulses (T0, A, B, AB, C, D, CD, E, F, EF, G, H, and GH).

The 13 individual bits are used in conjunction with the Config0.INHIBIT bit and the external iInhibit signal (TRIG_INH_RT). If all of the 13-bits are set, then the INH_EN signal is asserted (to the TAC) and triggers are gated by the external inhibit signal.

If any of the 13-bits is cleared, the inhibit signal blanks pulses who's bits are still set.

The **Interrupt** registers are comprised of two registers – control and status. The control register enables interrupts to be generated (either edge or level). The status register reports the present state of the event as well as any prior occurrence.

The events that may generate interrupts are triggers, end of delay, rate error, burst done, and external trigger Inhibit.

The **Status** register reports the state of various (trigger, burst cycle).

The **Dynamic** register contains bits that are asserted momentarily during the SPI data cycle. These include CLEAR CYCLE which asserts the CLEAR_CYCLE_N bit that connects to the TAC and terminates any cycle in progress.

The **Coincidence** register reflects the status of the 11-delay channels (a one corresponds to the given channel having timed out).

The **Version** register allows the microcontroller to determine the version of the FPGA firmware.

Synchronization and LVDS Translators

The FPGA's end of delay signals FEOD_[9:0] are CMOS levels with more timing dispersion than is permitted for desired accuracy. As such, a set of D-flops and resistor networks are used to reduce the timing dispersion and to translate the CMOS levels into LVDS levels with an impedance of 100 Ω.

NOTE: on our application, the LVDS signals are 400 mV and have an offset of 1 V.

The MAX9113 LVDS receiver (U82), translates the LVDS 100 MHz CLK100MHz_[7:6] into a pair of CMOS clocks CLK100MHz_B[1:0] that clock the synchronization D-Flops.

The D-Flops are also fed the FEOD_[9:0] signals and generate the complimentary CMOS outputs QEOD_[19:0]. These are then fed through resistor networks that both level shift and reverse terminate the resulting LVDS line for 'broadcast' to the verniers (where there is also a forward termination). This scheme guarantees good signal integrity and minimizes any cross coupling between adjacent channels.

100 MHz Timebase

Schematic sheet "DG_MB_TIMEBASE"

This circuit is comprised of a master oscillator X701, a distribution buffer U716, a phase lock loop (PLL) chip U724, discriminators U710/U739 and selector U725 for the two possible 10 MHz reference signals, and finally dividers and drivers U704/U707 for generating the 10 MHz Reference Output.

Interface

SPI_QMOSI, SPI_QSCK, SPI_BQCS10 (SPI Data, Clock, Chip Select): These are the buffered SPI interface from the FPGA. The microcontroller configures the PLL (U724)

using these signals. These signals are gated through the FPGA in order to minimize interference.

10MHZ_EXT_DET, 10MHZ_INT_DET: These outputs to the microcontroller indicate the presence of external and optional internal 10 MHz references. These will be zero volts for non-activity and 1.65 V when the signals are active.

ADC_VCO_CONT: This output to the microcontroller is used to monitor the control voltage of X701 (100 MHz Oscillator). The signal is band limited to 500 Hz and ranges between 0 and 3.3 V. By monitoring this signal when a high accuracy, External Reference is connected, we can determine what value the DAC_CAL_OSC signal must be set to order to achieve 1 ppm accuracy.

DAC_CAL_OSC: This input calibrates the internal 100 MHz. DAC_CAL_OSC is attenuated by R719/R720 and filtered by C714 to obtain the 3.3V full-scale range required by X701.

SEL_PLL: This input from the microcontroller enables U724 (PLL) and allows (via U725, analog multiplexer) the PLL to control X701. If no reference is detected, then U725 allows the DAC_CAL_OSC signal to control X701.

EXT_OPT_N: This input from the microcontroller controls U726 (digital multiplexer) to select between the internal or external 10 MHz for the PLL reference. In order to minimize any interference when an external reference is used, we disable the internal oscillator discriminator U739.

VCO_LOCK: This output to the microcontroller indicates if U724 (PLL) has been able lock X701 (100MHz oscillator) to the reference 10 MHz. The microcontroller will assert the front-panel LED “TIMEBASE – ERR” if the PLL is not able locked.

EXT_REF: This input is the rear-panel external 10 MHz timebase reference input.

CLK_10MHZ_OPT: This input is the optional internal 10 MHz timebase reference.

REF_OUT: This output for the rear-panel REF output is a scaled version (÷10) of the 100 MHz Oscillator.

CLK100MHZ_[xx]: These outputs are distributed to various other modules in the DG645.

Subcircuits

Reference Discriminators and Selector

The EXT_REF reference signal is AC coupled by L2 and presents a 1 kΩ load to the rear panel EXT REF input. The network L2/C44 form a resonant tank with f_r = 10 MHz. The diode pair D709 are used to improve the slew rate of the signal presented to U710, a TLV3501 (high speed comparator). U710’s inverting (‘-‘) input is set to +33 mV, and in the absence of a signal, U710’s output is 0 V. In the presence of a 10 MHz signal greater than 100 mV and assuming a 50 % duty factor, U710’s output (CLK_EXT_REF_DISC)

averages 1.65 V. This is filtered (by R704 and C725) to produce a DC voltage and monitored to detect the presence of an external reference.

The CLK_10MHZ_OPT reference signal (from and optional ovenized or rubidium oscillator) is terminated with pseudo 50Ω termination, comprised of a fixed 100 Ω and a diode pair 100 Ω. The diodes are used to improve the slew. The signal is then processed by U739.

The EXT_OPT_N determines (via multiplexer U726) which reference is used when the PLL is controlling the oscillator X701. Additionally, if an external reference is selected, the internal discriminator U739 is disabled by EXT_OPT_N (via the latch pin 1).

PLL and 100 MHz Oscillator

X701 is a voltage controlled oscillator with a nominal frequency of 100 MHz ± 1 kHz (10 ppm), a 20 ppm tuning range (±2 kHz), and PECL outputs (800 mV_{pp}).

U724 is a 400 MHz bandwidth integrated ADF4002 phase lock loop (PLL). U724 takes a single-ended reference input and differential inputs for the RF. The ADF4002 specifies a maximum 0 dBm (632 mV_{pp}) input signal at the RF inputs, thus X701s PECL output is both terminated and attenuated by RN708 before being AC-coupled into U724's RF inputs.

The SEL_PLL signal is used to enable the PLL to control X701 (via analog multiplexer U725). In the absence of a reference, SEL_PLL is driven low disabling the PLL and allowing the DAC_CAL_OSC to determine the setting of X701's output frequency.

U705 is a low noise, low dropout regulator that provides a local supply to maintain the power integrity for U724/U725/X701.

Clock Distribution

U716 (an MC100EP14 1:5 differential PECL clock driver) is used to distribute the timebase. X701's outputs (CLK100_OSC_P & CLK100_OSC_N) drive U716s CLK0 ports, and are replicated on U716's differential Qxx outputs.

CLK100MHz_[1:0] are used in the internal rate generator by U800 (AD9852 DDS) which takes native PECL levels using a 100Ω differential line.

The remaining PECL outputs are translated into LVDS using RN710 and RN712. This allows the distribution lines to be both forward and reverse terminated for optimal signal integrity.

CLK100MHz_[3:2] are used in the TAC and vernier sections. Due to the large load factor, these use a 50 Ω differential line.

CLK100MHz_[5:4] are used in the reference generator section and are distributed using a 100 Ω differential line.

CLK100MHz_[7:6] are used in the FPGA section and use a 100 Ω differential line.

10 MHz Reference Output Generator

A SN65LVDS2 (U708) translates the LVDS CLK100MHz_[5:4] into the CMOS signal CLK100M_REF. This clock is a presettable, binary counter (U704). U704 is configured to count between 4 and 8, and then reload 4. Thus, 4-5-6-7-8-4… produces a ÷5 prescaler with a 20 MHz output.

U707, a single D-flip-flop divides the 20 MHz down to 10 MHz and guarantees a symmetrical waveform, thus maximizing the energy content of the fundamental 10 MHz.

U707's 3.3 V levels and roughly 25 Ω outputs in conjunction with the 75 Ω series resistors R6/R7 provide a 3.3 V / 200 Ω drive to T3, a 4:1 transformer with a 0.2 to 300 MHz bandwidth.

The filter network L1 & C38 to C40 band pass the output to reduce the harmonic content providing a 10 MHz output of 0.5 V_{rms} into 50 Ω.

DDS & Trigger

Schematic sheet "DG_MB_TRIG"

This sheet provides the logic for the generation of the triggers that initiate timing cycles (either a single pulse or a burst of pulses). It is comprised of a DDS synthesizer (U800), a D-flop (U803) for re-synchronizing the scaled DDS output, a LVDS receiver (U804) for the external trigger signal (from the front panel output amplifier board), The pair of multiplexers (U801 & 802) are used for trigger selection, and a buffer (U2) replicates the final trigger signal for use by the FPGA.

Interface

SPI_QMOSI, SPI_QMISO, SPI_QSCK, SPI_BQCS10 (SPI data in/out, and clock and chip select inputs): These are used by the microcontroller to configure the DDS (U800).

DDS_UPD: This input from the microcontroller to update the latest SPI data in the DDS.

RESET: This input from the microcontroller resets the DDS.

DDS_DIS_CLK: This input from the microcontroller disables the 100 MHz into the DDS during initialization (the DDS requires no clock during initialization).

CLK100MHz_[1:0]: These inputs from the timebase (LVPECL) are the DDS synthesizer clock reference.

DDS_FSK: This input from the microcontroller is used to extend the DDS's native 48-bit frequency resolution by 16-bits, to 64-bits of resolution.

DDS_RATE: This output is the DDS frequency, which can range from between 12.5 and 25 MHz. This is then scaled by internal counters in the FPGA to achieve

2 times the requested frequency (DDS_RATE_D_2N), and then divided by two and resynchronized by the D-flop (U803).

DDS_RATE_D_2N: This input from the FPGA is the scaled version of the DDS.

EXT_TRG_S: These inputs are the LVDS output of the trigger discriminator on the front-panel output amplifier board, and are used during EXTRERNAL TRIGGER.

LINE_SC: This input from the FPGA is used both for single cycle and line triggering.

TRIG_SEL[1:0]: These inputs from the FPGA determine the multiplexer (U801 and 802) routing for the trigger.

TRIG_SOURCE, TRIG_SOURCE_1: These are the final outputs of the trigger and are sent to the TAC and FPGA.

Subcircuits

Internal Rate DDS Synthesizer

The internal rate generator utilizes a Direct Digital Synthesizer (DDS), FPGA, and D-flip flop to synthesize the requested frequency, which is applied to multiplexer U802.

The integrated 48-bit DDS, U800, is used to generate signals in a range between 12.5 MHz and 25.0 MHz (inclusive). The DDS provides complimentary 12-bit current source outputs at a sampling rate of 100 MHz. The buffered SPI interface of the microcontroller is used to read and write register data to the DDS.

The DDS output frequency is controlled by the 48-bit frequency tuning word (FTW) loaded in the DDS registers. The DDS has a frequency shift key (FSK) input which allows the DDS to shift between two different FTWs. This feature is used to extend the frequency resolution of the 48-bit DDS to 64-bits. Two 48-bit FTWs are loaded into the registers of U800: FTW and FTW+1. By applying a pulse width modulated (PWM) signal (with 16-bits of duty cycle resolution) to the FSK input, the frequency resolution of the DDS is extended by 16 bits. The frequency error associated with a ±1/2 LSB quantization error in the 16-bit duty cycle of the FSK will cause a clock output to time shift by 7 ps / year relative to an ideal source (which is considered to be negligible.

The DDS outputs a differential current mode digital to analog convertors (DACs) with a full scale output of 20 mA. This is then filtered by a 7^{th} order Chebyshev low pass filter with a corner frequency of 28 MHz to reduce the harmonic content.

The resulting differential voltage is applied to a high speed comparator in the DDS, which outputs as a CMOS signal (DDS_RATE) in the 12.5-25 MHz range.

The FPGA is then used to scale this signal by 2^N of the requested frequency and returned as DDS_RATE_D_2N.

Finally, in order reduce any dispersion or noise introduced by the FPGA, D-Flop U803 resynchronizes and divides the DDS_RATE_D_2N by 2 to achieve the requested frequency.

During the initialization of the DDS, the microcontroller disables the 100 MHz clock by pulling the DDS_CLK_DIS signal low. The transistor Q800 pulls the CLK100MHz_0 up to 3.3 V and guarantees that no clock is detected by the DDS.

External Trigger

The external trigger discriminator and edge polarity selection are implemented on the Main Pulse Output PCB. The resulting signals EXT_TRG_s (LVDS) are translated to CMOS levels by U804 and fed to the trigger select multiplexer U801.

Single Cycle and Line Trigger

The LINE_SC is the combined single cycle and line triggers. This is applied it to multiplexer U802.

The Line trigger originates on the POWER SUPPLY PCB. The native signal is then filtered in the FPGA to reduce timing dispersion. The single cycle signal is initiated by the microcontroller (during single cycle) and is also applied to this common signal.

A multiplexer internal to the FPGA determines if this signal carries the line or single cycle signal.

Trigger Selection

The multiplexers U801 and U802 are used to select from the three physical inputs (four virtual) selects from either the DDS rate, LINE_SC input, or external trigger, with the resulting signal TRIG_SOURCE being routed to the TAC. A replica of the final output, TRIG_SOURCE_1, is sent to the FPGA.

Time to Amplitude Convertor

Schematic sheet "DG_MB_TAC"

This sheet provides the analog voltage (V_JITTER) that is proportional to the phase between the trigger (TRIG_SOURCE) and the timebase clock (CLK100M)_. V_JITTER is also used by the verniers (amplitude to time converters) to eliminate jitter between randomly phased triggers and the outputs of the DG645.

The analog voltage V_JITTER is generated by a gated integrator. The gated integrator is turned on by TRIG_SOURCE (asynchronous to the timebase) and turned off by the next rising edge of CLK100M (plus delays for synchronization and settling). The integrator's current source is 10 mA with an integrating capacitor of 100 pF, which yields a charging rate of 100.0 mV / ns, and is calibrated by DAC_CAL_JIT to produce a voltage that varies by up to 1.000 V for trigger-to-clock phasing of 0° to 360°. V_JITTER is distributed using a single 70 Ω transmission line to all of the verniers.

The synchronized trigger (STOP_RAMP_P) is sent to the FPGA and initiates the 100 MHz coarse counters to begin their count down.

When the delays exceed 100 µs, the integration capacitor is augmented by an analog storage circuit VJSH_0, and for delays exceeding 3 ms, a digital replication of the V_JITTER - DAC_Jit_3ms - is used.

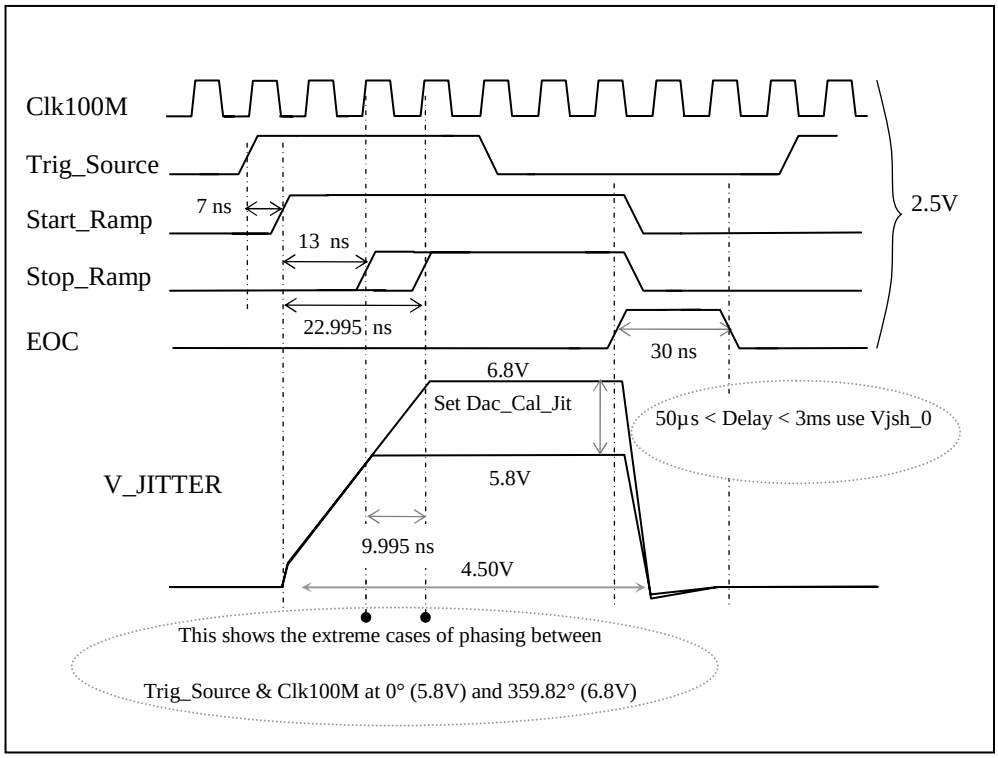

Figure 15: TAC Waveforms

Interface

CLK100MHz_[3:2]: These inputs from the timebase (LVDS) are the reference for conversions.

EN_TRIG: This input from the FPGA enables conversions.

TRIG_SOURCE: This input from the trigger section initiates a delay cycle.

CLEAR_CYCLE_N: This input from the FPGA clears any timing cycle in progress. It is used during initialization and data updates.

EOC: This input from the T01 waveform logic indicates that all delays have timed out. It also clears the TAC and prepares it for the next delay cycle.

LAST_B_PULSE: This input from the FPGA is used during burst mode to extend the TAC throughout the train of burst pulses.

INH_EN: This input from the FPGA enables the external TRIG_INHIBIT signal to gate the TRIG_SOURCE.

TRIG_INHIBIT: This input from the rear-panel connector J1 is used for the inhibit modes to gate the triggering of the TAC or blank individual pulses.

TRIG_INH_RT: This output to FPGA is a synchronized version the TRIG_INHIBIT signal used for pulse blanking.

TRIG_INH: This output to the FPGA is a non-synchronized version the TRIG_INHIBIT used for rate error detection.

STOP_RAMP_P: This output to the FPGA indicates that a delay cycle is in progress and initiates a coarse countdown.

VSH_[4:1]: These inputs from the FPGA control when the two V_JITTER storage augmentations are switched in.

V_JITTER: This is the main TAC output and is used by the verniers for the jitter reduction.

V_JITTER_ADC: This output is a scaled and level shifted version of the V_JIITER signal. This is used for capturing the value of V_JITTER and digital replication on the DAC_JIT_3MS input.

DAC_CAL_JIT: This input calibrates the gated integrator for 100.0 mV/ns.

DAC_JIT_3MS: This input is digital replica of V_JITTER and is used to maintain V_JITTER for delays exceeding 3 ms.

Subcircuits

Synchronization and Arming

The ARM signal at AND gate U627 determines if the TAC can accept triggers (feeds the D-input of U644) and is determined by the EN_TRIG, INH_EN, and TRIG_INHIBIT signals.

The TRIG_INHIBIT is processed by a comparator (U623) and must be greater than 1 V as set by the comparator bias and attenuation via RN605 and R610.

Table 45 indicates the ARM state based on EN_TRIG, INH_EN, and TRIG_INHIBIT signals:

Table 45: J6 Main Pulse Output PCB

Input			Output	Comments
EN_TRIG	INH_EN	TRIG_INHIBIT	ARM	
0	X	X	0 (Disarmed)	Disarmed
1	0	X	1 (Armed)	Normal Trigger
1	1	< 1V or no signal	1 (Armed)	Normal Trigger
1	1	> 1V	0 (Disarmed)	Trigger Inhibit

The TRIG_INH is also synchronized by a D-Flop (U645) and sent to the FPGA for controlling the channel inhibit functionality.

The LVDS timebase CLK100MHz_xx are translated via U664 to produce the CMOS signal CLK100M.

The D-Flops U641 and U644 and delay element U641 and U642 are used to process the incoming trigger and avoid metastability.

U644 is clocked by the TRIG_SOURCE and enabled by the ARM signal (via OR gate U628). The PRE_START output 'holds' U644 for the duration of the timing cycle and enables the subsequent D-Flops U641, U663, and U665.

The pair of LVDS translators (U642 and 643 set back-to-back) implement a 4 ns delay for the TRIG_SOURCE signal and allow the output of U644 to settle before being clocked into U641, generating the START_RAMP signal. The START_RAMP signal is asynchronous with respect to the 100 MHz timebase CLK100M and starts the gated integrator.

D-Flops U663 and U665 synchronize the START_RAMP signal with the timebase CLK100M and produce the STOP_RAMP_xx signals. As the two D-Flops are clocked by the same source, the first D-Flop (U665) signal has 10 ns to settle before the final D-Flop (U663) is clocked, eliminating any metastability. The STOP_RAMP is asserted between 14 and 23 ns after the START_RAMP signal. The STOP_RAMP signal is synchronous with the 100 MHz timebase and stops the integrator. It is also used by the FPGA to begin the coarse counting cycle.

Gated Integrator

The CAL_DAC_JIT is used to calibrate the current source (U602, Q619) and surrounding Rs and Cs for approximately 10 mA. This is eventually used to charge the integrating capacitor (C651) with a precise rate of 100.0 mV/ns. This current is fed into the transistor switching pair Q612A and B.

The U663's complimentary Q outputs (STOP_RAMP_s) drive the cascode pair Q611 and Q614 at between 11 mA and 0.25 mA. Q611's and Q614's collectors drive 75 Ω resistors (R664 and R665) and generate levels of 8.5 and 9.3 V to drive the switching pair Q612A and B that steer the current source toward C651.

When untriggered, Q612A sources current toward C651 (via R639). The high speed amplifier LM7171 (U622), in conjunction with the switch diode MMDB1701A (D605), form a voltage clamp (via R638) which holds C651 at 4.5 V. U622 is biased by a 5 V source fed through a pair of switch diodes (D606 & D607) which compensate for the temperature dependent drop across D605, and a similar diode used on the verniers.

The integrating capacitor C651 connects to Q612's collector (via R639), the switching diode D605 (via R638), and the output buffer U626.

When a trigger is received, START_RAMP is asserted and U622's output (the voltage clamp) is driven to 8.3 V. This allows Q612A's current to begin charging C651. After between 13 and 22.999 ns, the synchronizing D-Flop U663 is asserted (STOP_RAMP) and steers the integrating current away from Q612A to Q612B, stopping the charging of C651.

The net result is a voltage (VINT) on C651 that is proportional to the time between the incoming trigger and the phase of the internal 100 MHz timebase at 100 mV / ns. The minimum charging time of 13 ns corresponds to the time necessary to allow the voltage switch to settle to within 0.1 % of the current source. This corresponds to 0.1 % (1^{st} order) non-linearity in the ramp and translates into 10 ps error in the time to amplitude conversion.

Buffer and Storage Augmentation (Sample and Hold)

The wideband FET-input amplifier THS4631 (U626) buffers VINT and drives the 70 Ω transmission line used for distributing V_JITTER to the verniers. U626 is also used to "hold" the voltage on C651 via R633 and R634 for a short period (tens of microseconds).

Various parasitic sources will, over time, degrade the VINT signal. Two of the major sources for drift will be collector leakage through Q612A (I_{ces} = 10 nA) and the input offset voltage of U626 (V_{io} = 2 mV) that forces a current into the C651 via R633. The effect is that VINT continues to ramp at a (worst case) rate of 200 µV / µs. This would lead to an error of 2 ns for a 1 ms delay.

To compensate for this the integrating capacitor C651 is augmented by a dual stage sample and hold.

The VSH_[4:1] signals from the FPGA control the sequencing of the sample and hold switches as follows:

VSH_1 closes U601A/B from PRETRIG to 50 µs (initial sampling)

VSH_2 closes U601D from 50 µs to END_OF_CYCLE (initial hold)

VSH_3 & VSH_4 close U601C for delays longer than 3 ms.

Before triggering, VINT is clamped by U622 & D605 at 4.5 V.

After receiving a trigger, VINT is sustained by U626 via R633 and R634 feeding back the buffer V_JITTER. The switches 601A & B are closed and 601A, C, & D are open, with buffer U610A driving C628 to V_JITTER.

At 50 µs into the delay, switches U601A and B open and switch U601D closes, allowing the U609B to drive VINT (via R633) with the analog sampled version of V_JITTER. This prevents any further degradation due to the leakage and offset components of Q612 and U626 respectively. However, leakage from the switches U601B, C (≤ 0.1 nA) and op amp TLC072 (≤ 0.1 nA), and parasitic resistance from contamination (≥ 10 M Ω) will eventually degrade this voltage and lead to errors of 10 ns (and greater) for delays exceeding one second.

To avoid this error, the ADC samples V_JITTER_ADC (× 8) and the microcontroller replicates a scaled version on DAC_JIT_3MS. U601B and associated resistors translate the 0 to 4V DAC signal into an appropriate range of 5.3 to 7.1 V.

At 3 ms, switches U601A & B are opened, and switch U601C is closed allowing DAC_JIT_3MS to maintain VINT indefinitely.

When the delay terminates, VSH_[4:1] return the switches to their initial condition – with U601A/B closed, and U601C/D open.

Level Translator for the ADC & DAC

The V_JITTER_ADC is monitored by the ADC for calibration and during normal operation. U609A and its associated Rs & Cs translate the active range of V_JITTER (5.8 to 6.8 V) down to a range acceptable by the ADC (0.7 to 2.6 V). This range allows for 2300 bits of resolution (1.9 V / 3.3 V × 4096) or 4.3 ps / bit (10 ns / 2300). The ADC is also limited to a 10-bit ENOB (effective number of bits). In order to compensate for this and re-acquire an additional 1.5 bits, the signal must be sampled by × 8. This will allow for an effective resolution of 5.8 ps.

The control voltage DAC_JIT_3ms has a range of 0 to 4.096 V. U610B and its associated resistors translate this into a range of 5.3 to 7.1 V. This allows for a 1.8 V tuning range, of which only 1V is active. This provides 2276 bits (1/1.8 x4096) of tuning and a settability of 4.4 ps (10 ns / 2276).

Verniers

Schematic sheet “DG_MB_VERNIER_xy”

The verniers are on five sheets, with two channels per sheet, for a total of ten verniers. The sheets pair the channels in accordance with the font panel outputs (T0/T1, A/B, C/D, E/F, G/H). This description will cover the T0 channel of the T0/T1 sheet, but is applicable to all of the channels.

The verniers act as voltage-to-time converters, complimenting the TAC to eliminate any indeterminacy between the trigger and the DG645 outputs and allowing fine adjustment of the delay (5 ps).

Each channel is comprised of LVDS to CMOS translators, a resynchronization D-Flop (jitter reduction), a precision pulse amplifier (for controlling the initial level of the ramp), a gated integrator, and discriminators with LVDS outputs that are sent on to the waveform logic circuitry.

Figure 16 depicts the critical signals and levels:

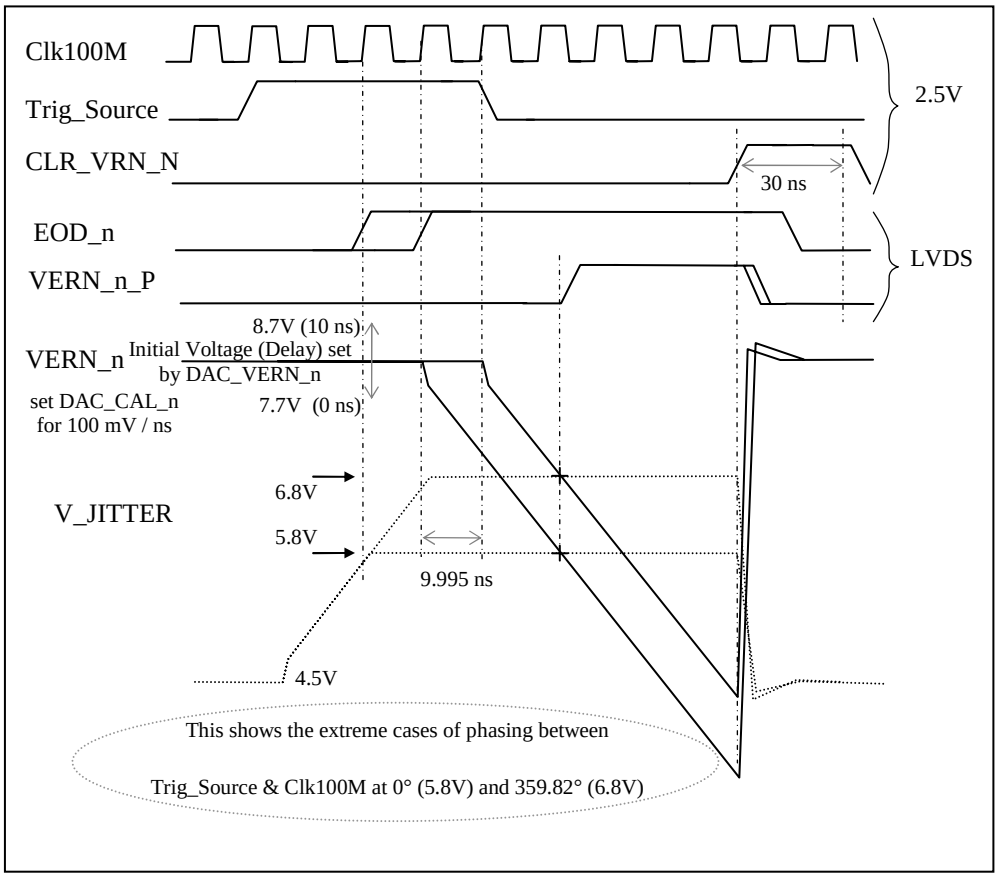

Figure 16: Vernier Waveforms

Interface

CLK100MHz_[3:2]: These inputs from the timebase (LVDS) are used to resynchronize the end of delay signals.

EOD_0_s: These inputs from the FPGA (LVDS) represent the coarse (10 ns) end of delay.

CLR_VRN_N: This input from the T0T1 waveform logic is used to clear the verniers.

VERN_0_s: These are the outputs of the verniers (LVDS) and are sent on to the waveform for conditioning module (before being routed to the output amplifier interfaces).

DAC_CAL_0: This input sets the vernier ramp to 100.0 mV / ns.

DAC_INS_DLY: This input sets the initial delay of all vernier channels.

DAC_VERN_n: This input determines the vernier's fine analog delay (0 to 9.995 ns).

Subcircuits

End of Delay Resynchronization

A pair of SN65LVDS2 LVDS translators (U102, U104) process the EOD_0_x (end of delay signals from the FPGA) and the timebase CLK100MHz_x. These are used by an SN74AUC74 D-Flop (U103) to resynchronized EOD_0, and minimize any timing dispersion or interference from adjacent channels. U103 is cleared by the CLR_VRN_N (from T1 vernier) after all channels have timed out.

Current Source and Integrator

An LT1396 precision high speed current mode amplifier (U101B) and an MMBT5179 NPN RF transistor (Q105) form a current source, which is used to charge capacitor C105. The DAC_CAL_0 is used to adjust the current source (approximately 10 mA) in conjunction with C105, to achieve a ramp rate of 100.0 mV/ns.

Fine Delay Setting and Ramp Gating

An LT1396 (U101A) is used both for setting the initial starting point and gating of the integrator. In the quiescent state, U101A holds the charging capacitor through R117 and D102 at an initial starting voltage that determines the analog delay. The initial starting voltage determines the resulting delay. This is controlled by U101A and RN101 (A= 4k, B = 1k), which forms a precision gain of ¼. The DAC_VERN_0 is used to program the starting voltage. The network resistors are matched to 0.1% and track to better than 25 ppm/ºC. This guarantees that the 0 to 4.000 V DAC_VERN_0 range translates to an initial starting voltage with a 0 to 1.000 V range with 1mV accuracy. This insures an error (non-monotinicity) of no greater than 10 ps. Since the networks are used in all vernier channels, channel to channel errors will be less than 20 ps. The initial starting voltage will range from 7.700 to 8.700 volts for corresponding delays of 0 to 9.995 ns.

The DACs are settable with 1 mV resolution (0.25 mV setting on the integrator). Delays may be set with 2.5 ps resolution. However this resolution is used only for calibration and allows achievable resolutions of 5ps.

The D-Flop (U103) drives a 499 Ω resistor (R107), which in conjunction with RN101B, forms a 2× gain. When U103 is triggered, U101A's output transitions from its initial starting point (of 8.5 to 9.5 volts) by 5 volts (to 3.5 to 4.5 Volts). This back biases D102 and allows Q110 to charge C114 at the rate of –100.0 mV / ns.

Voltage Comparator with LVDS outputs

The transistors Q101 and Q103 form a comparator with an LVDS output. Q101, R103, R106, and R102 form a current mirror that generates 8 mA for the differential comparator (Q103) and sets the output levels to either 1V or 1.4V.

The TAC conversion voltage V_JITTER is buffered by an additional LT1396, and sets the reference voltage at the base of Q103B, with Q103A monitoring the VERN_0 signal. When the VERN_0 drops below V_JITTER, VERN_0_P (VERN_0_N) switches high (low). These signals are passed onto the channel logic page before being routed to the various output amplifiers.

T0 & T1 Logic

Schematic sheet "DG_MB_CHANNEL_LOGIC_T01"

This sheet contains the channel logic for the signals from the verniers for the T0 front- and rear-panel PCB interface. It also contains circuitry for generating a blanking pulse for the remaining logic/waveform sheets and clearing the verniers at the end of a delay cycle. Finally, circuitry is implemented to allow for the measurement and calibration of the T0/T1 verniers and the TAC V_jitter ramp timing.

Interface

VERN_Tn_s: These inputs from verniers represent the main timing markers.

EOC_x: These outputs indicate the end of delay cycle.

CLR_VRN_N: This output clears all verniers at the end of a delay cycle.

OUT_EN0: This input from the FPGA blanks the output waveforms.

POL_T0: This input from the FPGA controls the polarity of front panel waveform.

FRONT_n_s: These outputs are sent to the front panel output PCB.

REAR_n_s: These outputs are sent to the rear panel output PCB.

ADC_DUTY_nm: This analog output is used for calibration of verniers and TAC.

Subcircuits

Both LVDS signals from the verniers VERN_T0_s and VERN_T1_s are translated to CMOS levels by SN65LVDS2 (U151 and U163).

T1 End Of delay

The T1 signal clocks a D-Flop (U162), which in turn drives the select input of an analog multiplexer (U160) switching its output from ground to +3.3 V through R155. R155 and C159 form a 25 ns time constant, after which U161 clears the D-Flop. This produces a low jitter 30 ns pulse. This is distributed (EOC_x and CLR_VRN_N) to clear all activity for the current timing cycle and blank outputs while the verniers and TAC are in transition.

T0 Logic

The T0 signal is fed through logic that (1) extends the pulse by 30 ns (U152), (2) allows blanking (U153), and (3) allows for polarity control (U155). Finally, the processed signals are sent to the front- and rear-panel output PCBs as LVDS (U156 and U154).

Vernier and TAC Calibration using Duty Factor

This circuit is used to calibrate the full scale delay of the verniers and TAC. It generates a DC voltage (ADC_DUTY_T01) from a pulse's duty factor at 500 mV/ 0.1%. This will produce an output of 2.5 V DC for a 0.5 % duty factor (10 ns width / 2 us period). As the ADC can resolve 0.8 mV, this translates into a time resolution of 3.2 ps. The ADC is also limited to a 10-bit ENOB (effective number of bits). In order to compensate for this and re-acquire the additional two bits, the signal must be oversampled by × 16.

The D-Flop U165 and NOR gate U12 allow the generation of a 10 ns pulse when the venier signals are set 10 ns apart. With a 2 us period, amplifier U152 and associated components, will produce a 2.5V DC signal. The ADC can resolve 0.8 mV out of 2.5V, or 1 part in 3125 of 10 ns, and thus 3.2 ps.

All delays are comprised of coarse (n x10 ns) and fine (0-9.995 ns) components (or n , f). For two delays that differ by 5 ps and alternate between zero and full scale vernier delays, we can determine the full scale vernier timing by measuring ADC_DUTY_T01. The DAC_CAL_VERN_0 is then adjusted (the vernier's current source) to realize a 0.8 mV difference between the two delays, and achieve a full scale error (and non-monotonicity) of less than of 5 ps.

For the TAC calibration we synchronously trigger the unit by setting the DDS frequency to 2.000 MHz (trigger to timebase phase will be fixed – and thus V_JITTER). We program the T1 to 1.7 µs, thus only allowing a 2 µs trigger period. Finally, we program T0 to realize a 2.5 V output on ADC_DUTY_T01 (approx. 1.5 µs – $T_{insertion}$ – 10 ns). This produces a condition where the D-Flop is clocked by T0 10 ns before one of the "blocked" DDS triggers, producing a 10 ns pulse, a 2 µs period and 2.5 V on ADC_DUTY_T01.

We then vary the phase of the DDS to find where the 100 MHz phase crossover occurs (by monitoring V_JITTER_ADC). By adjusting the DAC_CAL_JIT to minimize the change in ADC_DUTY_T01 at the phase cross over, we can set the full scale range of V_JITTER to within 3.2 ps of its nominal value of 1.00 V / 10 ns.

A - D (E - H) Logic

Schematic sheet "DG_MB_CHANNEL_LOGIC_z"

The waveform conditioning circuits are distributed over two pages. Each page contains two duplicate circuits, each circuit processes two vernier channels and generates the LVDS signals for the front and rear output amplifier interfaces. Additionally, each circuit has a duty factor circuit (similar to that used in the T0T1 circuit) used during calibrating the full scale vernier range.

Interface

VERN_n_s: These inputs are from the verniers (n = 0 to 3, s = P &N).

EOC_s: These inputs blank and extend the AB and A & B waveforms.

OUT_EN_n: This ouput from the FPGA enables the pulse waveform.

POL_n: This input from the FPGA determines the front-panel polarity.

FRONT_nm_s: These outputs drive the front-panel amplifier interface.

REAR_n_s: These outputs drive the rear-panel amplifier interface.

ADC_DUTY_nm: This analog output is for calibration of the verniers.

Subcircuits

There are four identical circuits on two sheets, only the 01 (AB) processing circuits will be described.

Front Panel Waveform Logic

Both of inputs from the verniers (VERN_n_s) are received as LVDS and translated by SN65LVDS2 (U251 and U220), to produce the CMOS P_0 and P_1 signals.

These signals are combined in the XOR U259 to generate a signal (W_01) that is proportional to their difference, and is the basis for the front panel AB output. The two AND gates (U267, U261) are used to enable the signal, before passing the signal to the XOR gate (U263) which implements polarity control. The signal is then translated back to LVDS by an SN65LVDS1 (U264) and sent to the front panel output interface.

Rear Panel Waveform Logic

The P_0 and P_1 signals are OR'd (U253, U272) with the 30 ns wide end of cycle signal (EOC_P) to extend the pulses and blank any transients caused by the resetting of the verniers and TAC at the end of cycle from being seen on the final pulse. The AND gates (U255, U274) are used to blank the signals during initialization and for the pulse inhibit function. The signals are then translated back to LVDS by SN65LVDS1s (U256, U275) and sent to the rear panel output interface.

Vernier Calibration using Duty Factor

This is used to calibrate the full scale delay of the verniers. This circuit generates a DC voltage (ADC_DUTY_01) from a pulse's duty factor at 500 mV/ 0.1 %. This will produce an output of 2.5 V DC for a 0.5 % duty factor (5 ns width / 1 µs period). As the ADC can resolve 0.8 mV, this translates into a time resolution of 3.2 ps.

All delays are comprised of coarse (n x 10 ns) and fine (0 to 9.995 ns) components (or n, f). For two delays that differ by 5 ps and alternate between zero and full scale vernier delays, we can determine the full-scale vernier timing by measuring ADC_DUTY_T01. The DAC_CAL_VERN_0 is then adjusted (the vernier's current source) to realize a 0.8 mV difference between the two delays, and achieve a full scale error (and non-monotonicity) of less than of 5 ps.

GPIB

Schematic sheet "DG_MB_GPIB"

The GPIB interface uses a TNT4882 (U900), which connects directly to the rear-panel GPIB connector (J3). Data is read and written to U900 via the bi-directional buffer U901, which translates U900's 5 V levels to 3.3 V levels necessary for the microcontroller (U50). Other control lines for U900 come directly from U50. U900 indicates a need for service by asserting GPIB_IRQ (a maskable interrupt request) to the microcontroller, which is level shifted by RN900B.

Power Supply IO

Schematic sheet "DG_MB_PSIO"

The power supply (+12VA, +3.3VA, +2.5VA, and the +4.096VREF) and grounding are implemented here.

Front-Panel Display

Schematic sheet "DG_FP1C"

The front panel uses time-multiplexed seven-segment LED displays, LED lamps, and a conductive rubber keypad to change and display the instrument settings. The PCB also has an audio transducer to generate key "clicks" and alarm sounds.

The display operates from +5 V and is controlled by a 3.3 V SPI interface. Data from the motherboard is clocked to the display, and data from the keypad is returned to the motherboard via the SPI interface. Level shifting between 3.3 V and 5 V is done by U30, a quad or-gate. Data from the mother board is shifted into six shift registers (U20 to U25) whose parallel outputs control displays and lamps. Data from the keypad is latched into a parallel in/serial out shift register (U26) whose data is clocked back to the motherboard.

The display cycle is divided into six intervals. Each interval activates one of five different strobe lines (STB0–STB4) by pulling that line high via an emitter follower, (Q1–Q5). One of the strobe intervals will be repeated to allow the highlighting of the cursor digit during the sixth interval. The strobe line pulls the common anode of four display digits, eight lamps, and the input to a column of six switches "high".

The cathodes of corresponding displays and lamps will be pulled low by "zeroes" in the shift registers U21–U24 for the displays, or in U25 via the emitter followers Q7–Q14 for the lamps. The LED currents are limited by the resistor networks N1–N8 for the displays, and N9 & N10 for the lamps. In order to protect the displays and lamps, the cathode driving shift registers will be disabled by U27A, a 74HC4538 10ms one-shot, if the SPI −CS becomes inactive.

Key click sounds and alarms are generated by the sounder SP1 which is driven by a 1 ms pulse from U27B via an emitter follower, Q6. A single pulse is used to generate a key click sound. A long series of pulses generate an alarm beep to warn that an improper command was attempted at the front panel.

Power Supply

Schematic sheet "DG_PS1B"

The power supply for the unit is contained in a separate shielded enclosure. The unit accommodates universal input voltages (90–264 VAC, 47–63 Hz) and provides a variety of DC voltages to the motherboard: +24 V, +15 V, +5 V, +3.3 V, −5 V, and −15 V. The unit will lock its DC–DC converter to a 200 kHz sync signal provided by the motherboard and will source a square wave at the AC line frequency, typically 50 Hz or 60 Hz. The unit also has a thermostatically controlled fan whose speed increases with increasing temperature.

An OEM power supply, Phihong PSA60-124, provides up to 3.3 A at +24 V from the line voltage input. This power supply is "on" whenever the line voltage is present, supplying +24 V to the motherboard to power optional timebases: either an ovenized crystal or rubidium oscillator. The +24 V supplied to the motherboard is filtered by L1 and C8 to remove ripples from the OEM power supply. The OEM supply also provides +24 V for a DC–DC converter to generate the other regulated voltages used in the system. The DC–DC converter and fan are "on" only when the front-panel power button is pressed "in."

The DC–D converter is disabled when the −DISABLE, pin 10 on the motherboard interface, is held low. When −DISABLE is released, the switching power supply controller (U5), generates complimentary square waves at about 100 kHz to drive the MOSFETs Q3 and Q4 into conduction during alternate half-cycles. The MOSFETs drive the primary of a transformer. The secondary voltages are rectified, filtered, and regulated to provide the +15 V, +5 V, +3.3 V, −5 V, and −15 V system voltages. One of the secondaries is not regulated but provides a floating 40 VDC source for the high-voltage rear-panel output option.

The regulated outputs have Schottky diodes on their outputs which prevent the power supplies from being pulled to the wrong polarity by loads which are connected to other supplies with opposite polarities. This is most important during start-up and to avoid SCR action in CMOS ICs in the case that one of the supplies should fail.

The DG645 has a LINE trigger mode. The line trigger is generated in the power supply by "sniffing" the AC line voltage input before it is applied to the OEM power supply. The circuit to do this is located on a small vertical PCB. Both the line and neutral leads (just in case the facility has swapped them) are held in close proximity to a large metal area on the PCB. The line voltage is capacitively coupled through the wires' insulation to this metal area. The coupled voltage is filtered by C1, R7 and C2 before being applied to the gate of an n-channel, small signal FET (Q2) which buffers the high impedance source. The FET is buffered by a unity follower op amp (U3B) which drives a gain of 100× amplifier, U3B. The output of the U3B is a square wave at the line frequency with about 20 µs transition times.

The thermostatic fan speed control is also located on the small vertical PCB. This circuit uses an LM35 (10 mV/deg C) as a temperature sensor. The output from the temperature sensor is offset, multiplied by 150×, and limited to a 0 to 15V range. This voltage is attenuated by 2× and offset (to assure a minimum fan speed) before driving a 12 V medium speed fan via the emitter follower, Q1.

Trigger Input and Front-Panel Outputs

Output Driver Control, Schematic sheet "DG_DR1C"

Circuitry for the external trigger input and front-panel output drivers is located on a 4.5" × 6.0" PCB which attaches directly to the inside of the instrument's front panel. The sub-assembly operates from ±5 V and ±15 V and is programmed via an SPI interface.

One connector, J101, transfers power supplies, the SPI interface, and fast LVDS signals between this sub-assembly and the motherboard. The ±5 V and ±15 V supplies from the motherboard are regulated to provide +3.3 V (U110) and +10 V (U108). A source to sink current at +6.7 V is provided by U109.

The SPI digital data is clocked into an 8-bit shift register, U102, to provide control of the Ext Trig polarity and of an analog multiplexer, U103, to allow the motherboard to measure the voltage at any output. The serial data is also clocked into two octal 12-bit DACs, which control the front-panel output amplitudes and offsets.

Ext Trig Input

The Ext Trig input threshold range is ±3.5 VDC. A high speed CMOS comparator is used to discriminate a trigger event. The Ext Trig input is scaled to the 0–4 VDC input range of the CMOS converter by N100, which offsets the input by 2.048 V and attenuates it by 2× while presenting a 1 MΩ Thevenin resistance to the input BNC. C100 and C101 attenuate high frequency components of the Ext Trig input by 2× while presenting about 18 pF to the Ext Trig input.

The comparator, U100, has a 4 ns propagation delay. The output of U100 will be inverted by the XOR gate, U111, if the polarity control bit, Q3 of U102, is set high. This is used to control the Ext Trig input polarity. The output of the XOR gate is converted to LVDS by U101. The differential output signal from U101 is sent to the motherboard via the main connector, J101.

Front-Panel Output Drivers

Output Drivers, Schematic sheet "DG_DR2C"

There are five front-panel output drivers, To, AB, CD, EF, and GH which provide outputs between −2 V and +5 V on the corresponding front-panel outputs. All of the outputs have 50 Ω source impedances and are intended to drive 50 Ω loads. Output amplitudes and offsets will double when not terminated and there will be some pulse distortion if the output exceeds 6.5 V. This can occur when an output is programmed to deliver a 0 to 5 V output pulse but is not terminated into 50 Ω.

The outputs are fast, high current pulse drivers capable of providing up to 200 mA into a 25 Ω load, (50 Ω internal load and 50 Ω external load) with a 1 ns rise time. The 50 Ω source impedance assures that the outputs will have a good "return loss" so that they will only reflect a small portion of a backward pulse that might, for example, have been reflected from a poorly matched user load.

All five output drivers are the same. The circuit description given here refers to the To output on sheet 2 of the 6 schematic pages which detail this subassembly.

The output is controlled by the LVDS signals +To and −To, which swing by 350 mV. The LVDS signal has a common mode voltage of 1.25 V, which must be translated up to about 8 V in order to be received by U201, an LVDS to CMOS receiver operating between 6.7 V and 10 V. To translate the LVDS signal, it is terminated by R200 and R201, ac coupled by C204 and C205, and DC restored by U200, resistor networks, N200 and N201, and resistors R202–R205. With this configuration, there is virtually no propagation delay to the high speed LVDS signal.

The output of the LVDS receiver has 20 Ω output impedance and swings between its power supply rails (6.7 V and 10 V) in about 600 ps. The two outputs drive the bases of two NPN emitter followers, Q200 and Q201, via 49.9 Ω base resistors. The emitters of these resistors are connected to the emitters of two PNP cascode transistors, Q202 and Q203, via 25 Ω of resistance. The collectors of the cascode transistor are connected to the outputs. The base voltage applied to the cascode transistors controls the output amplitude; if the base voltage is lowered, then more current is injected into the emitters of the cascode transistors thereby increasing the current provided to the output.

To accurately control the output amplitude the circuit will need to establish the correct bias at the bases of Q202 and Q203 under the control of a 12-bit DAC, T0_AMPL. A "mimic" circuit, with currents scaled down by a factor of 20× with respect to the actual output driver, is used to compensate for the V_{be} of emitter followers and the cascode outputs. The base of the mimic emitter follower, Q204, is pulled high via R216, as if it were an asserted output. The base bias of the mimic cascode transistor, as supplied by the output of the high speed op amp, U202, is at nearly the same potential as the bases of the actual cascode transistors. U202 is controlling the base bias so that the current from the mimic circuit is proportional to the voltage from the 12-bit DAC, and so the current from all of the cascode transistors will be proportional to the DAC voltage.

The output source resistance is 50 Ω, which consists of the parallel combination of four 200 Ω resistors: R214, R215, R229 and R230. Two of these resistors are connected to ground and the other two are connected to a voltage source which is used to provide the offset voltage for the output. The output offset source is controlled by a 12-bit DAC, T0_OFFS, which has been offset and scaled to the range ±1.00 VDC. The design of the voltage offset source is complicated by the requirement that the source should show very little transient (a few mV) when struck by a 50 mA current pulse (5 V/100 Ω) with a sub-nanosecond rise time.

To achieve a small transient, the offset voltage source is bypassed by two 0.1 µF capacitors, C216 and C217, which provide very low impedance to the current transient caused by the output pulse. Now the problem becomes controlling the voltage on these capacitors with the 12-bit DAC without introducing any feedback instabilities. It is notoriously difficult to drive a capacitive load with any op amp, as voltage feedback

from the capacitors is phase shifted by the op amp's output resistance and the load capacitance, virtually guaranteeing a circuit that will oscillate.

To overcome this difficulty, the output of an op amp is usually isolated from the capacitive load by a series resistor. In this circuit, that series resistor is R228, a 10 Ω resistor. But now there is a new problem; the voltage drop across the series resistor is significant and will degrade the output accuracy. To circumvent this new problem, the voltage drop across the series resistor can be corrected by "looking" at the output voltage and adjusting the output of the op amp to correct for the anticipated voltage drop across the 10 Ω series resistor. For example, if the output driver steps the output up by 5 V, we expect 5 V/100 Ω = 50 mA of current to flow via R229 and R230 on to the capacitors C216 and C217, which will need to be sourced from the op amp via the 10 Ω series resistor, R228. For this to happen without delay, the output of the op amp should jump down by V= I×R = 50mA × 10 Ω = 500 mV, or by 1/10 of the output pulse. This is arranged by providing a gain of −0.10× from the output BNC to the output of the offset op amp, which is accomplished by R223 and R224.

The offset current source will have to provide a lot of current in certain situations. For example, if the output offset is programmed for −2 V, then voltage on the capacitors, C216 and C217, will be −8 V. When the output steps up by 5 V during an output pulse, the output will be at +3 V, and so a current of I = V / R = (3+8) V / 100 Ω = 110 mA will need to be sunk by the offset source. This is more than the output amplifier, U203, can provide. To help out, a current boost circuit, Q206 and R225, starts to sink current when the op amp output current exceeds about 45 mA (sinking).

The output offset source is controlled by a 12-bit DAC that has been offset and scaled to the range of ±1.00 VDC. The op amp circuit (U203, etc.) has a gain, measured between the non-inverting input and the emitter of Q206, of about 8.5×. A resistor network, N202, is used to offset and scale the output voltage so that it can be measured by the CPU's 0–3.3 V ADC (on the motherboard) via the analog multiplexer, U103. This is used to verify the operation of the outputs and to provide an initial calibration of the output offset and amplitude.

Rear-Panel Outputs

Option 1: 8-Channel, 5 V

Internally, the DG645 generates 8 user-defined time events: A, B, C, D, E, F, G, and H. These timing events have a range of 2000 s and precision of 5 ps. The front-panel outputs pair these timing events to produce four output pulses: AB, CD, EF, and GH. In addition, a T_0 output is asserted at t=0 and remains asserted until 30 ns after the longest delay. The rear-panel Option 1 allows users to use each of the 8 timing events, independently, by producing an output at T_0 and at each of the 8 user-defined time events: A, B, C, D, E, F, G and H. All of these outputs use positive, 5 V logic (2.5 V into 50 Ω), going high at their programmed delay and going low about 30 ns after the longest programmed delay. There is no duty cycle limitation for these outputs.

This rear-panel option consists of four small PCBs; a vertical PCB that connects three small horizontal PCBs to the motherboard. Each of the three horizontal PCBs holds three output drivers.

Rear Panel 8-Channel, Schematic sheet "DG_RP1C"

The vertical PCB connects to the motherboard via a 36 pin connector, JP100. The connector provides power supplies, an SPI interface, and nine, fast, LVDS signals for T_0, A, B, C, D, E, F, G, and H. This option only uses the +5 V supply. The SPI interface is used to latch a bit which is set to enable the outputs and reset to disable the outputs. This bit is set once the unit has settled from its power-up sequence and reset as the unit powers-down in order to prevent spurious triggers.

The +5 V supply is regulated to +3.3 V by U100 to provide power to the nine LVDS line receivers. Each of the LVDS signals, T_0, A, B, C, D, E, F, G, and H, are converted to 3.3 V CMOS levels and passed to the output driver PCBs.

Rear Panel 8-Channel, Schematic sheet "DG_RP2C"

Each of the horizontal PCBs are identical and may be interchanged during assembly. Each channel consists of an AND gate (U200, for example) which ANDs the SPI enable bit with the CMOS level from one of the LVDS line receivers. The AND gate's input is compliant with 3.3 V logic levels but its output is a 5 V logic signal that drives the triple buffer that is used to drive the output BNC via a 45.3 Ω resistor. Each of the buffer channels has about 15 Ω of output resistance. Three in parallel is about 5 Ω, which in series with the 45.3 Ω resistor produces and output source resistance near 50 Ω. The 4.7 Ω resistor is used in series with the 0.1 µF Vcc bypass capacitor of the output driver to damp ringing which would otherwise occur after the rising edge of the output pulse.

Option 2: 8-Channel, High Voltage

Internally, the DG645 generates 8 user-defined time events: A, B, C, D, E, F, G, and H. These timing events have a range of 2000 s and precision of 5 ps. The front-panel outputs pair these timing events to produce four output pulses, AB, CD, EF, and GH. In addition, a T_0 output is asserted at t=0 and remains asserted until 30 ns after the longest delay. The rear-panel Option 2 allows users to use each of the 8 timing events independently by producing an output at T_0 and at each of the 8 user-defined time events: A, B, C, D, E, F, G, and H. All of these outputs use positive, 30 V logic (15 V into 50 Ω), going high at their programmed delay for a period of about 100 ns.

Each of the nine outputs can drive a 50 Ω load to +15 V, requiring a total current of 9×15/50 = 2.7 A from a 40 V internal supply. The peak power of 108 W cannot be maintained, and so the output amplitude is reduced as the duty cycle is increased. The output pulse amplitude is reduced by less than 1 % per kHz of trigger rate. Details will follow.

This rear-panel option consists of four small PCBs; a vertical PCB that connects three small horizontal PCBs to the motherboard. Each of the three horizontal PCBs holds three output drivers.

HV Rear-Panel Outputs, Schematic sheet "DG_HV1B"

The vertical PCB connects to the motherboard via a 36 pin connector, JP100. The connector provides power supplies, an SPI interface, and nine fast LVDS signals for T_0, A, B, C, D, E, F, G, and H. This option uses the +5 V and floating 40 VDC supplies.

The +5 V supply is regulated to +3.3 V by U100 to provide power to the nine LVDS line receivers. Each of the LVDS signals (T_0, A, B, C, D, E, F, G, and H) are converted to 3.3 V CMOS levels and used to trigger a 100 ns one-shot. The output of the one-shot, a 100 ns +5 V pulse, is passed to the horizontal output driver board.

HV Rear-Panel Outputs, Schematic sheet "DG_HV2B"

Each of the horizontal PCBs are identical and may be interchanged during assembly. Each channel has two parallel drivers for increased current capability consisting of a triple CMOS buffer driving the base of a PNP emitter follower. The 5 V swing of the CMOS buffer, less the V_{be} of the PNP emitter follower, together with the 14.0 Ω emitter resistor sets the magnitude of the collector current to be about 300 mA. Both collector currents sum to 600 mA to provide a 30 V pulse (with about 3 ns rise time) into the 50 Ω load that consists of the parallel combination of R15 and R16.

The total power from the HV outputs is limited by reducing the pulse current with increasing duty cycle. The charge reservoir for the output pulse is C11, a 4.7 µF capacitor. That capacitor is charged via R10, a 499 Ω resistor. The average current through R10 increases as the duty cycle of the pulse output increases; the increasing voltage drop across R10 reduces the voltage on C11 thereby reducing the pulse amplitude. It can be shown that the output pulse current is given by:

$$I_{PULSE} = 2 \cdot (5V - V_{BE}) / (R_{11} + 2 \cdot R_{10} \cdot f \cdot T)$$

Where $V_{be} \approx 0.7$ V, $R_{11} = 14$ Ω, $R_{10} = 499$ Ω, f = trigger rate, and T = pulse width (100 ns). The voltage pulse is given by $V_{PULSE} = I_{PULSE} \times 25$ Ω when the user load is 50 Ω or $V_{PULSE} = I_{PULSE} \times 50$ Ω when the user load is a high impedance.

Table 46 shows the output pulse amplitude vs. trigger rate (in kHz).

Table 46: Option 3 Pulse Amplitude vs Trigger Rate

f(kHz)	I_{PULSE} (A)	Percentage	V_{PULSE} (50 Ω)	V_{PULSE}(high Z)
0	0.614	100.0%	15.4	30.7
1	0.609	99.3%	15.2	30.5
2	0.605	98.6%	15.1	30.3
5	0.593	96.6%	14.8	29.7
10	0.573	93.3%	14.3	28.7
20	0.537	87.5%	13.4	26.9
50	0.452	73.7%	11.3	22.6
100	0.358	58.4%	9.0	17.9
200	0.253	41.2%	6.3	12.7
500	0.134	21.9%	3.4	6.7
1000	0.075	12.3%	1.9	3.8

Note that the HV pulse amplitude drops by less than 1 % per kHz of trigger rate. Also, the table shows the pulse amplitude for continuous operation; it is important to note that the first pulses will be at full amplitude: 15 V into 50 Ω or 30 V into a high impedance load.

Option 3: Combinatorial Logic Outputs

Internally, the DG645 generates 8 user-defined time events: A, B, C, D, E, F, G and H. These timing events have a range of 2000 s and precision of 5 ps. The front-panel outputs pair these timing events to produce four output pulses, AB, CD, EF, and GH. In addition, a T_0 output is asserted at t=0 and remains asserted until 30 ns after the longest delay. The rear-panel Option 3 provides copies of the front-panel outputs on the rear panel. In addition, the logical OR of AB + CD, EF + GH, AB + CD + EF and AB + CD + EF + GH are also provided to give 1, 2, 3, or 4 precisely defined pulses on separate BNC outputs. All of these outputs use positive, 5 V logic (2.5 V into 50 Ω), going high for the time between their programmed delays. There is no duty cycle limitation for these outputs.

This rear-panel option consists of four small PCBs; a vertical PCB that connects three small horizontal PCBs to the motherboard. Each of the three horizontal PCBs holds three output drivers.

Combo Rear-Panel Outputs, Schematic sheet "DG_CB1B"

The vertical PCB connects to the motherboard via a 36 pin connector, JP100. The connector provides power supplies, an SPI interface, and nine fast LVDS signals for T_0, A, B, C, D, E, F, G, and H. This option only uses the +5 V supply.

The +5 V supply is regulated to +3.3 V by U100 to provide power to the nine LVDS line receivers. Each of the LVDS signals, T_0, A, B, C, D, E, F, G, and H, are converted to 3.3 V CMOS levels. High speed logic gates are used to generate the required outputs; applying A and B to the input of an XOR gate generates a pulse that is high for the interval between A and B. OR gates are used to generate pulse combinations, and other OR gates are used to maintain equal propagation delays for outputs with 1, 2, 3 or 4 terms. The final results are passed to the horizontal output driver PCBs.

A 10 ns VETO signal is generated on the trailing edge of the T_0 output to veto glitches that might be generated by the XOR gates when both inputs transition simultaneously from high to low. This veto is generated on the vertical PCB and applied to the AND gate on the output driver PBC.

Combo Rear-Panel Outputs, Schematic sheet "DG_CB2B"

Each of the horizontal PCBs are identical and may be interchanged during assembly. Each channel consists of an AND gate, U200, for example, which ANDs the −VETO with each of the output terms. The AND gate's input is compliant with 3.3 V logic levels but its output is a 5 V logic signal that drives the triple buffer that is used to drive the output BNC via a 45.3 Ω resistor. Each of the buffer channels has about 15 Ω of output resistance. Three in parallel is about 5 Ω, which in series with the 45.3 Ω resistor produces an output source resistance near 50 Ω. The 4.7 Ω resistor is used in series with

the 0.1 µF Vcc bypass capacitor of the output driver to damp ringing which would otherwise occur after the rising edge of the output pulse.

Parts List

Motherboard Assembly

BD2	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD3	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD4	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD5	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD8	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD51	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD52	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD53	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD71	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD72	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD81	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD101	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD102	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD103	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD104	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD151	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD152	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD201	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD202	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD203	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD204	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD251	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD252	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD253	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD254	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD255	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD256	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD301	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD302	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD303	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD304	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD401	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD402	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD403	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD404	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD451	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD452	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD453	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD454	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD455	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD456	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD501	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD502	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD503	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD504	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD602	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD606	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD621	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD701	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD709	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD710	6-00759-631	2506031517Y0	Ferrite bead, SMT

BD800	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD801	6-00759-631	2506031517Y0	Ferrite bead, SMT
BD803	6-00759-631	2506031517Y0	Ferrite bead, SMT
BL1	6-00236-631	FR47	Ferrite bead, SMT
BL2	6-00236-631	FR47	Ferrite bead, SMT
BL3	6-00236-631	FR47	Ferrite bead, SMT
BL4	6-00236-631	FR47	Ferrite bead, SMT
BL7	6-00236-631	FR47	Ferrite bead, SMT
C 1	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 2	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 3	5-00591-568	1.0U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 4	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 5	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 6	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 7	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 8	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 9	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 10	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 11	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 12	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 13	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 14	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 15	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 16	5-00591-568	1.0U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 17	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 18	5-00657-578	22UF 10V /1206	SMT Ceramic Cap, all sizes
C 19	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 20	5-00657-578	22UF 10V /1206	SMT Ceramic Cap, all sizes
C 21	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 22	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 23	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 24	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 25	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 26	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 27	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 28	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 29	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 30	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 31	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 32	5-00318-569	2.2U/T35	Cap, Tantalum, SMT (all case sizes)
C 33	5-00527-568	.47U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 34	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 35	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 38	5-00728-580	330P	Cap. Mono. (0603), 50v,5%, NPO
C 39	5-00706-580	39P	Cap. Mono. (0603), 50v,5%, NPO
C 40	5-00728-580	330P	Cap. Mono. (0603), 50v,5%, NPO
C 41	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 42	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 43	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 44	5-00713-580	75P	Cap. Mono. (0603), 50v,5%, NPO
C 45	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 46	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 47	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 48	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 49	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 50	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 51	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 52	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 53	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 54	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 55	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 56	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R

C 57	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 58	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 59	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 60	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 61	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 62	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 70	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 72	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 73	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 75	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 76	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 77	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 78	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 79	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 80	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 81	5-00657-578	22UF 10V /1206	SMT Ceramic Cap, all sizes
C 82	5-00657-578	22UF 10V /1206	SMT Ceramic Cap, all sizes
C 83	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 84	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 85	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 86	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 87	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 88	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 89	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 91	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 92	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 93	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 94	5-00657-578	22UF 10V /1206	SMT Ceramic Cap, all sizes
C 95	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 96	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 97	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 98	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 99	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 101	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 102	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 103	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 104	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 105	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 106	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 107	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 108	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 109	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 110	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 111	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 112	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 113	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 114	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 115	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 116	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 117	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 151	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 152	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 153	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 156	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 157	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 158	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 159	5-00714-580	82P	Cap. Mono. (0603), 50v,5%, NPO
C 166	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 201	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 202	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 203	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 204	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R

C 205	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 206	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 207	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 208	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 209	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 210	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 211	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 212	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 213	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 214	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 215	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 216	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 217	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 224	5-00657-578	22UF 10V /1206	SMT Ceramic Cap, all sizes
C 225	5-00527-568	.47U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 251	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 252	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 253	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 254	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 255	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 256	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 257	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 258	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 259	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 260	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 261	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 262	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 263	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 264	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 265	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 266	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 301	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 302	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 303	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 304	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 305	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 306	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 307	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 308	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 309	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 310	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 311	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 312	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 313	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 314	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 315	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 316	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 317	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 401	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 402	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 403	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 404	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 405	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 406	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 407	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 408	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 409	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 410	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 411	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 412	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 413	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 414	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO

C 415	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 416	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 417	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 451	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 452	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 453	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 454	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 455	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 456	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 457	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 458	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 459	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 460	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 461	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 462	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 463	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 464	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 465	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 466	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 501	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 502	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 503	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 504	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 505	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 506	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 507	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 508	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 509	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 510	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 511	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 512	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 513	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 514	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 515	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 516	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 517	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 604	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 605	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 607	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 616	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 628	5-00545-554	3.3N	Capacitor, Polypropylene, Radial
C 629	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 641	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 644	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 650	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 651	5-00375-552	100P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 652	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 656	5-00675-580	2.2P	Cap. Mono. (0603), 50v,5%, NPO
C 657	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 662	5-00668-580	1P	Cap. Mono. (0603), 50v,5%, NPO
C 663	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 671	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 672	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 673	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 686	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 687	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 690	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 691	5-00724-580	220P	Cap. Mono. (0603), 50v,5%, NPO
C 692	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 708	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 714	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 717	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R

C 718	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 721	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 724	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 725	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 726	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 730	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 731	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 736	5-00740-580	1000P	Cap. Mono. (0603), 50v,5%, NPO
C 737	5-00720-580	150P	Cap. Mono. (0603), 50v,5%, NPO
C 738	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 742	5-00758-581	33000P	Cap. Mono, (0603), 50v, 10%, X7R
C 744	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 745	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 746	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 747	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 748	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 749	5-00716-580	100P	Cap. Mono. (0603), 50v,5%, NPO
C 800	5-00752-581	10000P	Cap. Mono, (0603), 50v, 10%, X7R
C 801	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 802	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 803	5-00708-580	47P	Cap. Mono. (0603), 50v,5%, NPO
C 804	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 805	5-00714-580	82P	Cap. Mono. (0603), 50v,5%, NPO
C 806	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 807	5-00714-580	82P	Cap. Mono. (0603), 50v,5%, NPO
C 809	5-00708-580	47P	Cap. Mono. (0603), 50v,5%, NPO
C 810	5-00714-580	82P	Cap. Mono. (0603), 50v,5%, NPO
C 811	5-00714-580	82P	Cap. Mono. (0603), 50v,5%, NPO
C 812	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 813	5-00708-580	47P	Cap. Mono. (0603), 50v,5%, NPO
C 814	5-00708-580	47P	Cap. Mono. (0603), 50v,5%, NPO
C 815	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 816	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 817	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 818	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 819	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 820	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 821	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 822	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 900	5-00661-578	1UF 16V /0603	SMT Ceramic Cap, all sizes
C 901	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 902	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 903	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 904	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 905	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
C 2001	5-00764-581	100000P	Cap. Mono, (0603), 50v, 10%, X7R
D 1	3-01752-311	598-8010-107F	LED, Subminiature
D 101	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 102	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 201	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 202	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 301	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 302	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 401	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 402	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 501	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 502	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 605	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 606	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 607	3-01753-360	MMBD1701A	Integrated Circuit (Surface Mount Pkg)
D 708	3-00538-360	MMBD352L-ROHS	Integrated Circuit (Surface Mount Pkg)
D 709	3-00538-360	MMBD352L-ROHS	Integrated Circuit (Surface Mount Pkg)

DG1	7-01871-701	DG645 M/B	Printed Circuit Board
J 1	1-00579-120	227677-1	Connector, BNC
J 2	1-01031-160	DEKL-9SAT-E	Connector, D-Sub, Right Angle PC, Female
J 3	1-00160-162	IEEE488/STAND.	Connector, IEEE488, Standard, R/A, Femal
J 4	1-00065-114	7 PIN; WHITE	Header, Amp, MTA-100
J 5	1-00579-120	227677-1	Connector, BNC
J 6	1-01144-132	HTSW-120-08-S-D	Header, DIP
J 7	1-01057-130	26-48-1101	Connector, Male
J 8	1-01215-132	SLW-118-01-G-D	Header, DIP
J 9	1-00579-120	227677-1	Connector, BNC
J 10	1-01089-100	J0011D21B	Connector, Misc.
J 11	1-01143-132	FWJ-13-04-T-S	Header, DIP
J 50	1-00083-130	26 PIN DIL	Connector, Male
J 70	1-01146-132	TSW-106-08-G-S	Header, DIP
J 1002	1-00488-130	2 PIN	Connector, Male
L 1	6-00686-609	0.68U	Inductor, Fixed, SMT
L 2	6-00669-609	3.3UH - S1210	Inductor, Fixed, SMT
L 600	6-00650-609	.47UH - SMT	Inductor, Fixed, SMT
L 701	6-00676-609	1.2UH / 5%	Inductor, Fixed, SMT
L 800	6-00597-609	1.5UH	Inductor, Fixed, SMT
L 801	6-00597-609	1.5UH	Inductor, Fixed, SMT
L 802	6-00597-609	1.5UH	Inductor, Fixed, SMT
L 803	6-00597-609	1.5UH	Inductor, Fixed, SMT
L 804	6-00597-609	1.5UH	Inductor, Fixed, SMT
L 805	6-00597-609	1.5UH	Inductor, Fixed, SMT
Q 101	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 103	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 105	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 106	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 108	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 110	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 201	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 203	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 205	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 206	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 208	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 210	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 301	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 303	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 305	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 306	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 308	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 310	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 401	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 403	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 405	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 406	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 408	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 410	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 501	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 503	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 505	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 506	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 508	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 510	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 611	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 612	3-01419-360	MBT3906DW1	Integrated Circuit (Surface Mount Pkg)
Q 614	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 619	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 800	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
R 1	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 2	4-02191-466	2.26K	Thin Film, 1%, 50ppm, 0603 Chip Resistor

R 3	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 4	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 5	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 6	4-02049-466	75.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 7	4-02049-466	75.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 8	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 9	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 10	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 11	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 12	4-02207-466	3.32K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 13	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 14	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 15	4-01974-466	12.4	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 16	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 17	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 18	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 30	4-02278-466	18.2K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 31	4-02215-466	4.02K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 32	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 50	4-02261-466	12.1K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 51	4-02262-466	12.4K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 55	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 70	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 71	4-02207-466	3.32K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 72	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 73	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 75	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 76	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 77	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 101	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 102	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 103	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 104	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 105	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 106	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 107	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 108	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 109	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 110	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 111	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 112	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 113	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 114	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 115	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 116	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 117	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 118	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 119	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 120	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 121	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 122	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 123	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 124	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 125	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 126	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 130	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 131	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 133	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 134	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 135	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 136	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 137	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor

R 138	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 139	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 140	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 145	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 146	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 151	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 152	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 153	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 154	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 155	4-02099-466	249	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 156	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 157	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 201	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 202	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 203	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 204	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 205	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 206	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 207	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 208	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 209	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 210	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 211	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 212	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 213	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 214	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 215	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 216	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 217	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 218	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 219	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 220	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 221	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 222	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 223	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 224	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 225	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 226	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 230	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 231	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 233	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 234	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 235	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 236	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 237	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 238	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 239	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 240	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 251	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 252	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 253	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 254	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 255	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 256	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 301	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 302	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 303	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 304	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 305	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 306	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 307	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 308	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor

R 309	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 310	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 311	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 312	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 313	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 314	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 315	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 316	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 317	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 318	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 319	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 320	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 321	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 322	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 323	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 324	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 325	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 326	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 330	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 331	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 333	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 334	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 335	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 336	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 337	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 338	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 339	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 340	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 401	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 402	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 403	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 404	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 405	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 406	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 407	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 408	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 409	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 410	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 411	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 412	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 413	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 414	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 415	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 416	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 417	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 418	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 419	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 420	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 421	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 422	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 423	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 424	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 425	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 426	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 430	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 431	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 433	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 434	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 435	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 436	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 437	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 438	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor

R 439	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 440	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 451	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 452	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 453	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 454	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 455	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 456	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 501	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 502	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 503	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 504	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 505	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 506	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 507	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 508	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 509	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 510	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 511	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 512	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 513	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 514	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 515	4-02078-466	150	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 516	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 517	4-01994-466	20.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 518	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 519	4-02241-466	7.50K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 520	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 521	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 522	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 523	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 524	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 525	4-02111-466	332	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 526	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 530	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 531	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 533	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 534	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 535	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 536	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 537	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 538	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 539	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 540	4-02070-466	124	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 602	4-02215-466	4.02K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 603	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 610	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 633	4-02379-466	205K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 634	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 635	4-01409-461	1.2	Thick Film, 5%, 200 ppm, Chip Resistor
R 638	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 639	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 640	4-02189-466	2.15K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 645	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 652	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 661	4-02128-466	499	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 662	4-02061-466	100	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 664	4-02049-466	75.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 665	4-02049-466	75.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 666	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 667	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 668	4-02099-466	249	Thin Film, 1%, 50ppm, 0603 Chip Resistor

R 669	4-01965-466	10.0	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 670	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 671	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 672	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 673	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 674	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 675	4-02258-466	11.3K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 676	4-02320-466	49.9K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 677	4-02121-466	422	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 678	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 679	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 680	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 681	4-02077-466	147	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 682	4-02195-466	2.49K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 685	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 686	4-02207-466	3.32K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 687	4-02191-466	2.26K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 690	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 691	4-02157-466	1.00K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 693	4-02189-466	2.15K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 704	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 705	4-02270-466	15.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 706	4-02349-466	100K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 707	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 708	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 709	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 710	4-02003-466	24.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 711	4-02061-466	100	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 712	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 713	4-02061-466	100	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 714	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 715	4-02224-466	4.99K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 716	4-02032-466	49.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 719	4-02195-466	2.49K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 720	4-02253-466	10.0K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 800	4-02169-466	1.33K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 801	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 802	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 803	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 804	4-02090-466	200	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 805	4-02215-466	4.02K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 1000	4-02217-466	4.22K	Thin Film, 1%, 50ppm, 0603 Chip Resistor
R 2001	4-02043-466	64.9	Thin Film, 1%, 50ppm, 0603 Chip Resistor
RN1	4-00906-463	100X4D	Resistor network, SMT, Leadless
RN3	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN30	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN38	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN50	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless
RN70	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN72	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN74	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN75	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN76	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN77	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN78	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN79	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN80	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN81	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN83	4-02454-463	742C083151J	Resistor network, SMT, Leadless
RN84	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless
RN85	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless
RN86	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless

RN88	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless
RN101	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN105	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN106	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN201	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN205	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN206	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN301	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN305	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN306	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN401	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN405	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN406	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN501	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN505	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
RN506	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN605	4-00910-463	1.0KX4D	Resistor network, SMT, Leadless
RN622	4-00911-463	4.7KX4D	Resistor network, SMT, Leadless
RN708	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN709	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN710	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN712	4-00916-463	47X4D	Resistor network, SMT, Leadless
RN900	4-01794-400	RA=4K,RB=1K	Resistor, Misc.
SW1	2-00053-208	B3F-1052	Switch, Momentary Push Button, NO
SW2	2-00023-218	DPDT	Switch, Panel Mount, Power, Rocker
T 3	6-00767-610	TC4-1T	Transformer
TP1	1-00143-101	TEST JACK	Vertical Test Jack
TP2	1-00143-101	TEST JACK	Vertical Test Jack
TP600	1-00143-101	TEST JACK	Vertical Test Jack
U 1	3-01757-360	ADM3202ARUZ	Integrated Circuit (Surface Mount Pkg)
U 2	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 3	3-01758-360	REF198GRU	Integrated Circuit (Surface Mount Pkg)
U 4	3-01185-360	LTC2620CGN	Integrated Circuit (Surface Mount Pkg)
U 5	3-01185-360	LTC2620CGN	Integrated Circuit (Surface Mount Pkg)
U 6	3-01386-360	DG408DY	Integrated Circuit (Surface Mount Pkg)
U 7	3-01185-360	LTC2620CGN	Integrated Circuit (Surface Mount Pkg)
U 8	3-01779-360	74LVC138APWT	Integrated Circuit (Surface Mount Pkg)
U 9	3-01764-360	LP3878SD-ADJ	Integrated Circuit (Surface Mount Pkg)
U 10	3-01764-360	LP3878SD-ADJ	Integrated Circuit (Surface Mount Pkg)
U 12	3-01864-360	74AUC1G02DCKR	Integrated Circuit (Surface Mount Pkg)
U 13	3-00728-360	LM393	Integrated Circuit (Surface Mount Pkg)
U 42	3-01778-360	74LVC74APWT	Integrated Circuit (Surface Mount Pkg)
U 50	3-01676-360	MCF52235CAL60	Integrated Circuit (Surface Mount Pkg)
U 70	3-01764-360	LP3878SD-ADJ	Integrated Circuit (Surface Mount Pkg)
U 71	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 72	3-01768-360	M25PE20-VMN6TP	Integrated Circuit (Surface Mount Pkg)
U 73	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 74	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 75	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 76	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 77	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 78	3-01765-360	LP3879SD-1.2	Integrated Circuit (Surface Mount Pkg)
U 80	3-01783-360	XC3S250E-4TQ144	Integrated Circuit (Surface Mount Pkg)
U 81	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 82	3-01761-360	MAX9113EKA	Integrated Circuit (Surface Mount Pkg)
U 83	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 84	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 85	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 98	3-01857-360	LM95071CIMFX	Integrated Circuit (Surface Mount Pkg)
U 101	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 102	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 103	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)

U 104	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 105	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 106	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 107	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 108	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 127	3-01762-360	LM340SX-12	Integrated Circuit (Surface Mount Pkg)
U 151	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 152	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 153	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 154	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 155	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 156	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 159	3-01763-360	LMC6035IMM	Integrated Circuit (Surface Mount Pkg)
U 160	3-01776-360	74AUC2G53DCUR	Integrated Circuit (Surface Mount Pkg)
U 161	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 162	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 163	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 165	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 166	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 201	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 202	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 203	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 204	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 205	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 206	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 207	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 208	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 212	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 220	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 223	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 251	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 252	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 253	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 254	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 255	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 256	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 257	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 258	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 259	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 260	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 261	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 263	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 264	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 265	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 266	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 267	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 268	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 271	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 272	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 274	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 275	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 276	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 277	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 278	3-01763-360	LMC6035IMM	Integrated Circuit (Surface Mount Pkg)
U 301	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 302	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 303	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 304	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 305	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 306	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 307	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 308	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)

U 401	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 402	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 403	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 404	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 405	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 406	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 407	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 408	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 412	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 420	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 423	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 451	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 452	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 453	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 454	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 455	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 456	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 457	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 458	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 459	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 460	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 461	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 463	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 464	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 465	3-01775-360	74AUC1G86DCKR	Integrated Circuit (Surface Mount Pkg)
U 466	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 467	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 468	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 471	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 472	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 474	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 475	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 476	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 477	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 478	3-01763-360	LMC6035IMM	Integrated Circuit (Surface Mount Pkg)
U 501	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 502	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 503	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 504	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 505	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 506	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 507	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 508	3-01759-360	LT1396CMS8	Integrated Circuit (Surface Mount Pkg)
U 601	3-01756-360	ADG1211YRUZ	Integrated Circuit (Surface Mount Pkg)
U 602	3-01763-360	LMC6035IMM	Integrated Circuit (Surface Mount Pkg)
U 609	3-01781-360	TLC072CDGNR	Integrated Circuit (Surface Mount Pkg)
U 610	3-01781-360	TLC072CDGNR	Integrated Circuit (Surface Mount Pkg)
U 615	3-01782-360	TLV3501AIDBVT	Integrated Circuit (Surface Mount Pkg)
U 622	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 623	3-01771-360	74AUC1G00DCKR	Integrated Circuit (Surface Mount Pkg)
U 626	3-01780-360	THS4631DGN	Integrated Circuit (Surface Mount Pkg)
U 627	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 628	3-01773-360	74AUC1G32DCKR	Integrated Circuit (Surface Mount Pkg)
U 629	3-01771-360	74AUC1G00DCKR	Integrated Circuit (Surface Mount Pkg)
U 630	3-01772-360	74AUC1G08DCKR	Integrated Circuit (Surface Mount Pkg)
U 638	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 641	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 642	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 643	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 644	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 645	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 663	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)

U 664	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 665	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 667	3-01763-360	LMC6035IMM	Integrated Circuit (Surface Mount Pkg)
U 702	3-01763-360	LMC6035IMM	Integrated Circuit (Surface Mount Pkg)
U 704	3-01863-360	74LVC163	Integrated Circuit (Surface Mount Pkg)
U 705	3-01784-360	LP5900SD-3.3	Integrated Circuit (Surface Mount Pkg)
U 706	3-01784-360	LP5900SD-3.3	Integrated Circuit (Surface Mount Pkg)
U 707	3-01867-360	74LVC2G74DCTR	Integrated Circuit (Surface Mount Pkg)
U 708	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 710	3-01782-360	TLV3501AIDBVT	Integrated Circuit (Surface Mount Pkg)
U 711	3-01204-360	SN74LVC1G32DBVR	Integrated Circuit (Surface Mount Pkg)
U 712	3-01204-360	SN74LVC1G32DBVR	Integrated Circuit (Surface Mount Pkg)
U 716	3-01193-360	MC100EP14DT	Integrated Circuit (Surface Mount Pkg)
U 724	3-01755-360	ADF4002BRUZ	Integrated Circuit (Surface Mount Pkg)
U 725	3-01776-360	74AUC2G53DCUR	Integrated Circuit (Surface Mount Pkg)
U 726	3-01766-360	74LVC1G157GW	Integrated Circuit (Surface Mount Pkg)
U 739	3-01782-360	TLV3501AIDBVT	Integrated Circuit (Surface Mount Pkg)
U 800	3-01122-360	AD9852AST	Integrated Circuit (Surface Mount Pkg)
U 801	3-01776-360	74AUC2G53DCUR	Integrated Circuit (Surface Mount Pkg)
U 802	3-01776-360	74AUC2G53DCUR	Integrated Circuit (Surface Mount Pkg)
U 803	3-01774-360	74AUC1G74DCUR	Integrated Circuit (Surface Mount Pkg)
U 804	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 900	3-01019-360	TNT4882-BQ	Integrated Circuit (Surface Mount Pkg)
U 901	3-01777-360	74LVC245APWR	Integrated Circuit (Surface Mount Pkg)
X 701	6-00760-625	100.000MHZ	Voltage Controlled Crystal Oscillator

Output Driver Assembly

C 100	5-00369-552	33P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 101	5-00368-552	27P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 103	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 104	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 105	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 106	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 107	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 108	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 109	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 110	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 111	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 112	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 114	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 115	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 116	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 117	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 118	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 119	5-00472-569	4.7U/T35	Cap, Tantalum, SMT (all case sizes)
C 120	5-00472-569	4.7U/T35	Cap, Tantalum, SMT (all case sizes)
C 121	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 122	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 123	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 200	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 201	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 202	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 203	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 204	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 205	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 206	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 207	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 208	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 209	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 210	5-00357-552	3.3P	Capacitor, Chip (SMT1206), 50V, 5%, NPO

C 211	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 212	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 213	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 214	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 216	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 217	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 218	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 300	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 301	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 302	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 303	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 304	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 305	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 306	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 307	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 308	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 309	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 310	5-00357-552	3.3P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 311	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 312	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 313	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 314	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 316	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 317	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 318	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 400	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 401	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 402	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 403	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 404	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 405	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 406	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 407	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 408	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 409	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 410	5-00357-552	3.3P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 411	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 412	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 413	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 414	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 416	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 417	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 418	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 500	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 501	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 502	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 503	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 504	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 505	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 506	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 507	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 508	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 509	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 510	5-00357-552	3.3P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 511	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 512	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 513	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 514	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 516	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 517	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 518	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 600	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes

C 601	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 602	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 603	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 604	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 605	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 606	5-00387-552	1000P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 607	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 608	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 609	5-00313-552	1P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 610	5-00357-552	3.3P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 611	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 612	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 613	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 614	5-00794-578	4.7UF / 25V X7R	SMT Ceramic Cap, all sizes
C 616	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 617	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 618	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
J 100	1-01158-120	73100-0195	Connector, BNC
J 101	1-01150-150	SSQ-120-03-S-D-	Socket, THRU-HOLE
J 200	1-01158-120	73100-0195	Connector, BNC
J 300	1-01158-120	73100-0195	Connector, BNC
J 400	1-01158-120	73100-0195	Connector, BNC
J 500	1-01158-120	73100-0195	Connector, BNC
J 600	1-01158-120	73100-0195	Connector, BNC
L 100	6-00236-631	FR47	Ferrite bead, SMT
L 101	6-00236-631	FR47	Ferrite bead, SMT
L 102	6-00236-631	FR47	Ferrite bead, SMT
L 103	6-00236-631	FR47	Ferrite bead, SMT
L 200	6-00236-631	FR47	Ferrite bead, SMT
L 201	6-00236-631	FR47	Ferrite bead, SMT
L 202	6-00236-631	FR47	Ferrite bead, SMT
L 203	6-00236-631	FR47	Ferrite bead, SMT
L 204	6-00236-631	FR47	Ferrite bead, SMT
L 205	6-00530-609	.027UH - SMT	Inductor, Fixed, SMT
L 300	6-00236-631	FR47	Ferrite bead, SMT
L 301	6-00236-631	FR47	Ferrite bead, SMT
L 302	6-00236-631	FR47	Ferrite bead, SMT
L 303	6-00236-631	FR47	Ferrite bead, SMT
L 304	6-00236-631	FR47	Ferrite bead, SMT
L 305	6-00530-609	.027UH - SMT	Inductor, Fixed, SMT
L 400	6-00236-631	FR47	Ferrite bead, SMT
L 401	6-00236-631	FR47	Ferrite bead, SMT
L 402	6-00236-631	FR47	Ferrite bead, SMT
L 403	6-00236-631	FR47	Ferrite bead, SMT
L 404	6-00236-631	FR47	Ferrite bead, SMT
L 405	6-00530-609	.027UH - SMT	Inductor, Fixed, SMT
L 500	6-00236-631	FR47	Ferrite bead, SMT
L 501	6-00236-631	FR47	Ferrite bead, SMT
L 502	6-00236-631	FR47	Ferrite bead, SMT
L 503	6-00236-631	FR47	Ferrite bead, SMT
L 504	6-00236-631	FR47	Ferrite bead, SMT
L 505	6-00530-609	.027UH - SMT	Inductor, Fixed, SMT
L 600	6-00236-631	FR47	Ferrite bead, SMT
L 601	6-00236-631	FR47	Ferrite bead, SMT
L 602	6-00236-631	FR47	Ferrite bead, SMT
L 603	6-00236-631	FR47	Ferrite bead, SMT
L 604	6-00236-631	FR47	Ferrite bead, SMT
L 605	6-00530-609	.027UH - SMT	Inductor, Fixed, SMT
N 100	4-01791-463	4X1.0M	Resistor network, SMT, Leadless
N 101	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 102	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 103	4-00912-463	10KX4D	Resistor network, SMT, Leadless

N 200	4-02460-463	3.3KX4	Resistor network, SMT, Leadless
N 201	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 202	4-01792-463	R4X33K	Resistor network, SMT, Leadless
N 300	4-02460-463	3.3KX4	Resistor network, SMT, Leadless
N 301	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 302	4-01792-463	R4X33K	Resistor network, SMT, Leadless
N 400	4-02460-463	3.3KX4	Resistor network, SMT, Leadless
N 401	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 402	4-01792-463	R4X33K	Resistor network, SMT, Leadless
N 500	4-02460-463	3.3KX4	Resistor network, SMT, Leadless
N 501	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 502	4-01792-463	R4X33K	Resistor network, SMT, Leadless
N 600	4-02460-463	3.3KX4	Resistor network, SMT, Leadless
N 601	4-00912-463	10KX4D	Resistor network, SMT, Leadless
N 602	4-01792-463	R4X33K	Resistor network, SMT, Leadless
PC1	7-01873-701	DG645 PCB	Printed Circuit Board
Q 200	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 201	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 202	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 203	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 204	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 205	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 206	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 300	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 301	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 302	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 303	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 304	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 305	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 306	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 400	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 401	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 402	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 403	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 404	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 405	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 406	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 500	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 501	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 502	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 503	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 504	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 505	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 506	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
Q 600	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 601	3-01212-360	BFG541	Integrated Circuit (Surface Mount Pkg)
Q 602	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 603	3-01211-360	BFG31	Integrated Circuit (Surface Mount Pkg)
Q 604	3-00808-360	MMBT5179	Integrated Circuit (Surface Mount Pkg)
Q 605	3-01214-360	BFT92	Integrated Circuit (Surface Mount Pkg)
Q 606	3-00580-360	MMBT3906LT1	Integrated Circuit (Surface Mount Pkg)
R 100	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 101	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 103	4-01108-462	806	Thin Film, 1%, 50 ppm, MELF Resistor
R 104	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 105	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 106	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 107	4-01030-462	124	Thin Film, 1%, 50 ppm, MELF Resistor
R 108	4-01111-462	866	Thin Film, 1%, 50 ppm, MELF Resistor
R 109	4-01050-462	200	Thin Film, 1%, 50 ppm, MELF Resistor
R 110	4-01030-462	124	Thin Film, 1%, 50 ppm, MELF Resistor

R 200	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 201	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 202	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 203	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 204	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 205	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 206	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 207	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 208	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 209	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 210	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 211	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 212	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 213	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 214	4-01793-400	200/1W	Resistor, Misc.
R 215	4-01793-400	200/1W	Resistor, Misc.
R 216	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 217	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 218	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 219	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 220	4-01158-462	2.67K	Thin Film, 1%, 50 ppm, MELF Resistor
R 221	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 222	4-01000-462	60.4	Thin Film, 1%, 50 ppm, MELF Resistor
R 223	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 224	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 225	4-00942-462	15.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 226	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 227	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 228	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 229	4-01793-400	200/1W	Resistor, Misc.
R 230	4-01793-400	200/1W	Resistor, Misc.
R 231	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 232	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 233	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 234	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 300	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 301	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 302	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 303	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 304	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 305	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 306	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 307	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 308	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 309	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 310	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 311	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 312	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 313	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 314	4-01793-400	200/1W	Resistor, Misc.
R 315	4-01793-400	200/1W	Resistor, Misc.
R 316	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 317	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 318	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 319	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 320	4-01158-462	2.67K	Thin Film, 1%, 50 ppm, MELF Resistor
R 321	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 322	4-01000-462	60.4	Thin Film, 1%, 50 ppm, MELF Resistor
R 323	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 324	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 325	4-00942-462	15.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 326	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor

R 327	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 328	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 329	4-01793-400	200/1W	Resistor, Misc.
R 330	4-01793-400	200/1W	Resistor, Misc.
R 331	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 332	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 333	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 334	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 400	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 401	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 402	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 403	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 404	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 405	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 406	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 407	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 408	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 409	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 410	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 411	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 412	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 413	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 414	4-01793-400	200/1W	Resistor, Misc.
R 415	4-01793-400	200/1W	Resistor, Misc.
R 416	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 417	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 418	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 419	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 420	4-01158-462	2.67K	Thin Film, 1%, 50 ppm, MELF Resistor
R 421	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 422	4-01000-462	60.4	Thin Film, 1%, 50 ppm, MELF Resistor
R 423	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 424	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 425	4-00942-462	15.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 426	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 427	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 428	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 429	4-01793-400	200/1W	Resistor, Misc.
R 430	4-01793-400	200/1W	Resistor, Misc.
R 431	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 432	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 433	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 434	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 500	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 501	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 502	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 503	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 504	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 505	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 506	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 507	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 508	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 509	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 510	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 511	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 512	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 513	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 514	4-01793-400	200/1W	Resistor, Misc.
R 515	4-01793-400	200/1W	Resistor, Misc.
R 516	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 517	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 518	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor

R 519	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 520	4-01158-462	2.67K	Thin Film, 1%, 50 ppm, MELF Resistor
R 521	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 522	4-01000-462	60.4	Thin Film, 1%, 50 ppm, MELF Resistor
R 523	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 524	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 525	4-00942-462	15.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 526	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 527	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 528	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 529	4-01793-400	200/1W	Resistor, Misc.
R 530	4-01793-400	200/1W	Resistor, Misc.
R 531	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 532	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 533	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 534	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 600	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 601	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 602	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 603	4-01146-462	2.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 604	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 605	4-01204-462	8.06K	Thin Film, 1%, 50 ppm, MELF Resistor
R 606	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 607	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 608	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 609	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 610	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 611	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 612	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 613	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 614	4-01793-400	200/1W	Resistor, Misc.
R 615	4-01793-400	200/1W	Resistor, Misc.
R 616	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 617	4-01059-462	249	Thin Film, 1%, 50 ppm, MELF Resistor
R 618	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 619	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 620	4-01158-462	2.67K	Thin Film, 1%, 50 ppm, MELF Resistor
R 621	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 622	4-01000-462	60.4	Thin Film, 1%, 50 ppm, MELF Resistor
R 623	4-01184-462	4.99K	Thin Film, 1%, 50 ppm, MELF Resistor
R 624	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 625	4-00942-462	15.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 626	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 627	4-00963-462	24.9	Thin Film, 1%, 50 ppm, MELF Resistor
R 628	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 629	4-01793-400	200/1W	Resistor, Misc.
R 630	4-01793-400	200/1W	Resistor, Misc.
R 631	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 632	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 633	4-00954-462	20.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 634	4-00992-462	49.9	Thin Film, 1%, 50 ppm, MELF Resistor
U 100	3-01791-360	TLV3501AID	Integrated Circuit (Surface Mount Pkg)
U 101	3-01769-360	65LVDS1DBV	Integrated Circuit (Surface Mount Pkg)
U 102	3-01866-360	74HCT595D	Integrated Circuit (Surface Mount Pkg)
U 103	3-00661-360	74HC4051	Integrated Circuit (Surface Mount Pkg)
U 104	3-01865-360	LMC6492BEM	Integrated Circuit (Surface Mount Pkg)
U 105	3-01865-360	LMC6492BEM	Integrated Circuit (Surface Mount Pkg)
U 106	3-01185-360	LTC2620CGN	Integrated Circuit (Surface Mount Pkg)
U 107	3-01185-360	LTC2620CGN	Integrated Circuit (Surface Mount Pkg)
U 108	3-01281-360	LM317MDT	Integrated Circuit (Surface Mount Pkg)
U 109	3-01282-360	LM337KTP	Integrated Circuit (Surface Mount Pkg)
U 110	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)

U 111	3-01854-360	74LVC1G86DBVR	Integrated Circuit (Surface Mount Pkg)
U 112	3-01886-360	74LVC1G125DBV	Integrated Circuit (Surface Mount Pkg)
U 200	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 201	3-01188-360	MAX9113ESA	Integrated Circuit (Surface Mount Pkg)
U 202	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 203	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 300	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 301	3-01188-360	MAX9113ESA	Integrated Circuit (Surface Mount Pkg)
U 302	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 303	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 400	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 401	3-01188-360	MAX9113ESA	Integrated Circuit (Surface Mount Pkg)
U 402	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 403	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 500	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 501	3-01188-360	MAX9113ESA	Integrated Circuit (Surface Mount Pkg)
U 502	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 503	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 600	3-00774-360	LMC662C	Integrated Circuit (Surface Mount Pkg)
U 601	3-01188-360	MAX9113ESA	Integrated Circuit (Surface Mount Pkg)
U 602	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
U 603	3-00819-360	LM7171AIM	Integrated Circuit (Surface Mount Pkg)
Z 0	0-01259-040	1/2" CUSTOM	Washer, Flat
Z 0	7-02021-721	BNC TOOL	Machined Part
Z 0	9-01570-917	SIM-PCB S/N	Product Labels
Z 1	7-01881-720	DG645 BRACKET	Fabricated Part
Z 2	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 3	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 4	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 5	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 6	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips

Power Supply Assembly

C 1	5-00285-562	100P	Cap., NPO Monolitic Ceramic, 50v, 5% Ra
C 2	5-00200-532	470P	Capacitor, Ceramic Disc, 50V, 10% NPO
C 3	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 4	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 5	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 6	5-00288-528	.01U	Cap, Mono. Ceramic, 50V, 10%, X7R RAD
C 7	5-00612-509	1000U	Capacitor, Electrolytic, 50V, 20%, Rad
C 8	5-00612-509	1000U	Capacitor, Electrolytic, 50V, 20%, Rad
C 9	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 10	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 11	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 12	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 13	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 14	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
C 15	5-00665-509	220U-100V	Capacitor, Electrolytic, 50V, 20%, Rad
C 16	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 17	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 18	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 19	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 20	5-00516-526	330U HIGH RIPPL	Capacitor, Electrolytic, 35V, 20%, Rad
C 21	5-00098-517	10U	Capacitor, Tantalum, 35V, 20%, Rad
C 22	5-00098-517	10U	Capacitor, Tantalum, 35V, 20%, Rad
C 23	5-00098-517	10U	Capacitor, Tantalum, 35V, 20%, Rad
C 24	5-00098-517	10U	Capacitor, Tantalum, 35V, 20%, Rad
C 25	5-00098-517	10U	Capacitor, Tantalum, 35V, 20%, Rad
C 26	5-00098-517	10U	Capacitor, Tantalum, 35V, 20%, Rad
C 27	5-00049-566	.001U	Cap, Polyester Film 50V 5% -40/+85c Rad

C 28	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 29	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
C 30	5-00143-536	1200P	Capacitor, Ceramic, 1000 VDCW
D 1	3-00011-303	RED	LED, T1 Package
D 2	3-01208-301	MUR220	Diode
D 3	3-01208-301	MUR220	Diode
D 4	3-01208-301	MUR220	Diode
D 5	3-01208-301	MUR220	Diode
D 6	3-01208-301	MUR220	Diode
D 7	3-01208-301	MUR220	Diode
D 8	3-01208-301	MUR220	Diode
D 9	3-01208-301	MUR220	Diode
D 10	3-01208-301	MUR220	Diode
D 11	3-01208-301	MUR220	Diode
D 12	3-01208-301	MUR220	Diode
D 13	3-01208-301	MUR220	Diode
D 14	3-01208-301	MUR220	Diode
D 15	3-01208-301	MUR220	Diode
D 16	3-00516-301	1N5819	Diode
D 17	3-00516-301	1N5819	Diode
D 18	3-00516-301	1N5819	Diode
D 19	3-00516-301	1N5819	Diode
D 20	3-00516-301	1N5819	Diode
J 1A	1-00250-116	2 PIN, WHITE	Header, Amp, MTA-156
J 1B	1-00275-131	2 PIN DIF #18GA	Connector, Female
J 2	1-01151-132	SSW-105-01-S-S	Header, DIP
J 3	1-01152-132	HTSW105-08SS-RA	Header, DIP
J 4	1-01153-132	FHP-13-01-T-S	Header, DIP
L 1	6-00646-601	10UH	Inductor
L 2	6-00646-601	10UH	Inductor
L 3	6-00647-601	47UH	Inductor
L 4	6-00646-601	10UH	Inductor
L 5	6-00647-601	47UH	Inductor
L 6	6-00647-601	47UH	Inductor
L 7	6-00647-601	47UH	Inductor
L 8	6-00647-601	47UH	Inductor
L 9	6-00647-601	47UH	Inductor
PC1	7-01874-701	DG645 P/S PCB	Printed Circuit Board
Q 1	3-00021-325	2N3904	Transistor, TO-92 Package
Q 2	3-00635-325	PN4117A	Transistor, TO-92 Package
Q 3	3-00283-340	IRF530/IRF532	Integrated Circuit (Thru-hole Pkg)
Q 4	3-00283-340	IRF530/IRF532	Integrated Circuit (Thru-hole Pkg)
R 1	4-00192-407	49.9K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 2	4-00130-407	1.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 3	4-00192-407	49.9K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 4	4-00142-407	100K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 5	4-00142-407	100K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 6	4-00131-407	1.00M	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 7	4-00131-407	1.00M	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 8	4-00139-407	10.0M	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 9	4-00138-407	10.0K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 10	4-00130-407	1.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 11	4-00142-407	100K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 12	4-00131-407	1.00M	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 13	4-00138-407	10.0K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 14	4-00130-407	1.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 15	4-00030-401	10	Resistor, Carbon Film, 1/4W, 5%
R 16	4-00080-401	47	Resistor, Carbon Film, 1/4W, 5%
R 17	4-00080-401	47	Resistor, Carbon Film, 1/4W, 5%
R 18	4-00347-407	7.50K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 19	4-00685-408	100.0	Resistor, Metal Film, 1/8W, 0.1%, 25ppm
R 20	4-01790-458	.22/2W	Resistor, Metal Oxide

R 21	4-00149-407	121	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 22	4-00439-407	1.33K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 23	4-00080-401	47	Resistor, Carbon Film, 1/4W, 5%
R 24	4-00080-401	47	Resistor, Carbon Film, 1/4W, 5%
R 25	4-00180-407	301	Resistor, Metal Film, 1/8W, 1%, 50PPM
T 1	6-00765-615	DG645	Power Supply
U 1	3-01785-360	LM35DZ	Integrated Circuit (Surface Mount Pkg)
U 2	3-00889-340	LMC662	Integrated Circuit (Thru-hole Pkg)
U 3	3-00889-340	LMC662	Integrated Circuit (Thru-hole Pkg)
U 4	3-00346-329	7812	Voltage Reg., TO-220 (TAB) Package
U 5	3-00634-340	3525A	Integrated Circuit (Thru-hole Pkg)
U 6	3-01786-340	LM1086CT-ADJ	Integrated Circuit (Thru-hole Pkg)
U 7	3-01787-360	LM2990T-15	Integrated Circuit (Surface Mount Pkg)
U 8	3-01788-340	LM1086CT-5.0	Integrated Circuit (Thru-hole Pkg)
U 9	3-01789-360	LM2990T-5	Integrated Circuit (Surface Mount Pkg)
U 10	3-01790-340	LM1086CT-3.3	Integrated Circuit (Thru-hole Pkg)
Z 0	0-00043-011	4-40 KEP	Nut, Kep
Z 0	0-00048-011	6-32 KEP	Nut, Kep
Z 0	0-00084-032	36154	Termination
Z 0	0-00089-033	4"	Tie
Z 0	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 0	0-00177-002	6ESRM-3	Power Entry Hardware
Z 0	0-00185-021	6-32X3/8PP	Screw, Panhead Phillips
Z 0	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 0	0-00222-021	6-32X1/4PP	Screw, Panhead Phillips
Z 0	0-00231-043	1-32, #4 SHOULD	Washer, nylon
Z 0	0-00243-003	TO-220	Insulators
Z 0	0-00456-021	6-32X3/4PP	Screw, Panhead Phillips
Z 0	0-00634-032	2-520184-2	Termination
Z 0	0-01014-050	4"GREEN W/YELL	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01181-070	KDE1205PHV2	Fans, & Hardware
Z 0	0-01189-050	12" BLACK	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01190-050	12" WHITE	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01191-050	3" BLACK	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	0-01192-050	3" RED	Wire #18 UL1007 Stripped 3/8x3/8 No Tin
Z 0	1-00120-113	3 PIN, 18AWG/OR	Connector, Amp, MTA-156
Z 0	1-00472-112	2 PIN, 24AWG/WH	Connector, Amp, MTA-100
Z 0	1-00473-114	2 PIN, WHITE	Header, Amp, MTA-100
Z 0	1-00496-113	6 POS 18GA ORNG	Connector, Amp, MTA-156
Z 0	6-00655-615	24V - 60W	Power Supply
Z 0	7-01884-720	DG645 P/S CHASS	Fabricated Part
Z 0	7-01885-720	DG645 MYLAR	Fabricated Part
Z 0	7-01887-720	DG645 COVER	Fabricated Part

Front-Panel Display Assembly

C 1	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 2	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 3	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 4	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 5	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 6	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 7	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 8	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
D 1	3-00424-307	GREEN	LED, T-3/4
D 2	3-00424-307	GREEN	LED, T-3/4
D 3	3-00424-307	GREEN	LED, T-3/4
D 4	3-00424-307	GREEN	LED, T-3/4
D 5	3-00424-307	GREEN	LED, T-3/4
D 6	3-00424-307	GREEN	LED, T-3/4
D 7	3-00424-307	GREEN	LED, T-3/4

D 8	3-00424-307	GREEN	LED, T-3/4
D 9	3-00424-307	GREEN	LED, T-3/4
D 10	3-00424-307	GREEN	LED, T-3/4
D 11	3-00424-307	GREEN	LED, T-3/4
D 12	3-00424-307	GREEN	LED, T-3/4
D 13	3-00424-307	GREEN	LED, T-3/4
D 14	3-00424-307	GREEN	LED, T-3/4
D 15	3-00424-307	GREEN	LED, T-3/4
D 16	3-00425-307	RED	LED, T-3/4
D 17	3-00424-307	GREEN	LED, T-3/4
D 18	3-00424-307	GREEN	LED, T-3/4
D 19	3-00424-307	GREEN	LED, T-3/4
D 20	3-00424-307	GREEN	LED, T-3/4
D 21	3-00424-307	GREEN	LED, T-3/4
D 22	3-00424-307	GREEN	LED, T-3/4
D 23	3-00424-307	GREEN	LED, T-3/4
D 24	3-00424-307	GREEN	LED, T-3/4
D 25	3-00424-307	GREEN	LED, T-3/4
D 26	3-00424-307	GREEN	LED, T-3/4
D 27	3-00424-307	GREEN	LED, T-3/4
D 28	3-00424-307	GREEN	LED, T-3/4
D 29	3-00424-307	GREEN	LED, T-3/4
D 30	3-00424-307	GREEN	LED, T-3/4
D 31	3-00424-307	GREEN	LED, T-3/4
D 32	3-00424-307	GREEN	LED, T-3/4
D 33	3-00424-307	GREEN	LED, T-3/4
D 34	3-00425-307	RED	LED, T-3/4
D 35	3-00424-307	GREEN	LED, T-3/4
D 36	3-00424-307	GREEN	LED, T-3/4
D 37	3-00425-307	RED	LED, T-3/4
D 41	3-01084-360	BAL99LT1	Integrated Circuit (Surface Mount Pkg)
D 42	3-01084-360	BAL99LT1	Integrated Circuit (Surface Mount Pkg)
D 43	3-01084-360	BAL99LT1	Integrated Circuit (Surface Mount Pkg)
D 44	3-01084-360	BAL99LT1	Integrated Circuit (Surface Mount Pkg)
D 45	3-01084-360	BAL99LT1	Integrated Circuit (Surface Mount Pkg)
JP1	1-00065-114	7 PIN; WHITE	Header, Amp, MTA-100
L 1	6-00236-631	FR47	Ferrite bead, SMT
L 2	6-00236-631	FR47	Ferrite bead, SMT
N 1	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 2	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 3	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 4	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 5	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 6	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 7	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 8	4-02461-463	680 OHMS X 4	Resistor network, SMT, Leadless
N 9	4-01715-463	15X4	Resistor network, SMT, Leadless
N 10	4-01715-463	15X4	Resistor network, SMT, Leadless
N 11	4-01789-463	10KX4	Resistor network, SMT, Leadless
N 12	4-01789-463	10KX4	Resistor network, SMT, Leadless
PC1	7-01872-701	DG645 F/P PCB	Printed Circuit Board
Q 1	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 2	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 3	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 4	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 5	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 6	3-01210-360	BC817	Integrated Circuit (Surface Mount Pkg)
Q 7	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 8	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 9	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 10	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 11	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)

Q 12	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 13	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
Q 14	3-01209-360	BC807	Integrated Circuit (Surface Mount Pkg)
R 1	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 2	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 3	4-01309-462	100K	Thin Film, 1%, 50 ppm, MELF Resistor
R 4	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
SP1	6-00096-600	MINI	Misc. Components
SW1	7-01877-740	DG645 KEYPAD	Keypad, Conductive Rubber
U 1	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 2	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 3	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 4	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 5	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 6	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 7	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 8	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 9	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 10	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 11	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 12	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 13	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 14	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 15	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 16	3-01424-340	HDSP-A107	Integrated Circuit (Thru-hole Pkg)
U 17	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 18	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 19	3-00290-340	HDSP-A101	Integrated Circuit (Thru-hole Pkg)
U 20	3-00787-360	74HC595	Integrated Circuit (Surface Mount Pkg)
U 21	3-00787-360	74HC595	Integrated Circuit (Surface Mount Pkg)
U 22	3-00787-360	74HC595	Integrated Circuit (Surface Mount Pkg)
U 23	3-00787-360	74HC595	Integrated Circuit (Surface Mount Pkg)
U 24	3-00787-360	74HC595	Integrated Circuit (Surface Mount Pkg)
U 25	3-00787-360	74HC595	Integrated Circuit (Surface Mount Pkg)
U 26	3-01157-360	74HC165	Integrated Circuit (Surface Mount Pkg)
U 27	3-01467-360	74HC4538	Integrated Circuit (Surface Mount Pkg)
U 29	3-01252-360	74LVC1G00DBVR	Integrated Circuit (Surface Mount Pkg)
U 30	3-01850-360	74HCT32D-T	Integrated Circuit (Surface Mount Pkg)
U 31	3-01886-360	74LVC1G125DBV	Integrated Circuit (Surface Mount Pkg)
Z 0	9-01570-917	SIM-PCB S/N	Product Labels

Chassis Assembly

Z 0	1-01222-174	7 PIN CABLE	Cable, Misc.
Z 1	0-00079-031	4-40X3/16 M/F	Standoff
Z 2	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 3	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 4	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 5	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 6	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 7	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 8	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 9	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 10	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 11	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 12	0-00150-026	4-40X1/4PF	Screw, Black, All Types
Z 13	0-00179-000	RIGHT FOOT	Hardware, Misc.
Z 14	0-00180-000	LEFT FOOT	Hardware, Misc.
Z 15	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 16	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 17	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips

Z 18	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 19	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 20	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 21	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 22	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 23	0-00204-000	REAR FOOT	Hardware, Misc.
Z 24	0-00204-000	REAR FOOT	Hardware, Misc.
Z 25	0-00237-016	F1404	Power Button
Z 26	0-00238-026	6-32X1/4PF	Screw, Black, All Types
Z 27	0-00238-026	6-32X1/4PF	Screw, Black, All Types
Z 28	0-00238-026	6-32X1/4PF	Screw, Black, All Types
Z 29	0-00238-026	6-32X1/4PF	Screw, Black, All Types
Z 30	0-00242-026	8-32X1/4PF	Screw, Black, All Types
Z 31	0-00242-026	8-32X1/4PF	Screw, Black, All Types
Z 32	0-00248-026	10-32X3/8TRUSSP	Screw, Black, All Types
Z 33	0-00248-026	10-32X3/8TRUSSP	Screw, Black, All Types
Z 34	0-00248-026	10-32X3/8TRUSSP	Screw, Black, All Types
Z 35	0-00248-026	10-32X3/8TRUSSP	Screw, Black, All Types
Z 36	0-00271-000	BUMPER	Hardware, Misc.
Z 37	0-00326-026	8-32X1/4PP	Screw, Black, All Types
Z 38	0-00326-026	8-32X1/4PP	Screw, Black, All Types
Z 39	0-00326-026	8-32X1/4PP	Screw, Black, All Types
Z 40	0-00326-026	8-32X1/4PP	Screw, Black, All Types
Z 41	0-00500-000	554043-1	Hardware, Misc.
Z 42	0-00500-000	554043-1	Hardware, Misc.
Z 43	0-00517-000	BINDING POST	Hardware, Misc.
Z 44	0-00589-026	4-40X5/16"PF	Screw, Black, All Types
Z 45	0-00589-026	4-40X5/16"PF	Screw, Black, All Types
Z 46	0-00589-026	4-40X5/16"PF	Screw, Black, All Types
Z 47	0-00589-026	4-40X5/16"PF	Screw, Black, All Types
Z 48	0-00671-026	6-32 X 3/8"PF	Screw, Black, All Types
Z 49	0-00671-026	6-32 X 3/8"PF	Screw, Black, All Types
Z 50	0-00671-026	6-32 X 3/8"PF	Screw, Black, All Types
Z 51	7-00122-720	DG535-36	Fabricated Part
Z 52	7-00217-735	PS300-40	Injection Molded Plastic
Z 53	7-00259-720	SR560-28	Fabricated Part
Z 54	7-00260-720	SR560-27	Fabricated Part
Z 55	7-01878-709	DG645 LEXAN	Lexan Overlay
Z 56	7-01879-720	DG645 CHASSIS	Fabricated Part
Z 57	7-01880-720	DG645 CHASSIS	Fabricated Part
Z 58	7-01883-720	DG645 BRACKET	Fabricated Part
Z 59	7-01886-720	DG645 COVER PLT	Fabricated Part

Option 1 Assembly

C 100	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 101	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 102	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 103	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 104	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 105	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 106	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 107	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 108	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 109	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 200	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 201	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 202	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 300	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 301	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 302	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

C 400	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 401	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 402	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
J 200	1-01158-120	73100-0195	Connector, BNC
J 201	1-01158-120	73100-0195	Connector, BNC
J 202	1-01158-120	73100-0195	Connector, BNC
J 300	1-01158-120	73100-0195	Connector, BNC
J 301	1-01158-120	73100-0195	Connector, BNC
J 302	1-01158-120	73100-0195	Connector, BNC
J 400	1-01158-120	73100-0195	Connector, BNC
J 401	1-01158-120	73100-0195	Connector, BNC
J 402	1-01158-120	73100-0195	Connector, BNC
JP100	1-01147-132	TLW-118-06-G-D	Header, DIP
JP101	1-01200-130	6 POS.	Connector, Male
JP102	1-01200-130	6 POS.	Connector, Male
JP103	1-01200-130	6 POS.	Connector, Male
JP200	1-01199-131	6 POS.	Connector, Female
JP300	1-01199-131	6 POS.	Connector, Female
JP400	1-01199-131	6 POS.	Connector, Female
L 100	6-00236-631	FR47	Ferrite bead, SMT
L 200	6-00236-631	FR47	Ferrite bead, SMT
L 201	6-00236-631	FR47	Ferrite bead, SMT
L 202	6-00236-631	FR47	Ferrite bead, SMT
L 300	6-00236-631	FR47	Ferrite bead, SMT
L 301	6-00236-631	FR47	Ferrite bead, SMT
L 302	6-00236-631	FR47	Ferrite bead, SMT
L 400	6-00236-631	FR47	Ferrite bead, SMT
L 401	6-00236-631	FR47	Ferrite bead, SMT
L 402	6-00236-631	FR47	Ferrite bead, SMT
R 101	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 103	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 104	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 105	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 106	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 107	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 108	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 109	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 110	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 111	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 112	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 200	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 201	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 202	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 203	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 204	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 205	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 300	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 301	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 302	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 303	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 304	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 305	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 400	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 401	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 402	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 403	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 404	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 405	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
U 100	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 101	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 102	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)

U 103	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 104	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 105	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 106	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 107	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 108	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 109	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 110	3-01252-360	74LVC1G00DBVR	Integrated Circuit (Surface Mount Pkg)
U 111	3-01203-360	SN74LVC1G08DBVR	Integrated Circuit (Surface Mount Pkg)
U 112	3-01867-360	74LVC2G74DCTR	Integrated Circuit (Surface Mount Pkg)
U 113	3-01881-360	DS1810R-5+T&R	Integrated Circuit (Surface Mount Pkg)
U 200	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 201	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 202	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 203	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 204	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 205	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 300	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 301	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 302	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 303	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 304	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 305	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 400	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 401	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 402	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 403	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 404	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 405	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
Z 0	0-01259-040	1/2" CUSTOM	Washer, Flat
Z 0	7-02021-721	BNC TOOL	Machined Part
Z 0	9-01570-917	SIM-PCB S/N	Product Labels
Z 1	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 2	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 3	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 4	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 5	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 6	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
Z 7	7-01882-720	DG645 BRACKET	Fabricated Part
Z 8	7-01882-720	DG645 BRACKET	Fabricated Part
Z 9	7-01882-720	DG645 BRACKET	Fabricated Part
Z 10	7-01875-701	DG645 OPTION	Printed Circuit Board

Option 2 Assembly

C 1	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 2	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 3	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 10	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 11	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 12	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 20	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 21	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 22	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 30	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 31	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 32	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 40	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 41	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 42	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 50	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R

C 51	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 52	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 60	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 61	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 62	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 70	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 71	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 72	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 80	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 81	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 82	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 90	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 91	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 92	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 100	5-00792-578	4.7UF - 100V	SMT Ceramic Cap, all sizes
C 101	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 102	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 103	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 110	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 111	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 120	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 121	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 130	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 131	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 140	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 141	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 150	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 151	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 160	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 161	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 170	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 171	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 180	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 181	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
C 190	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 191	5-00370-552	39P	Capacitor, Chip (SMT1206), 50V, 5%, NPO
J 10	1-01158-120	73100-0195	Connector, BNC
J 20	1-01158-120	73100-0195	Connector, BNC
J 30	1-01158-120	73100-0195	Connector, BNC
J 31	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
J 32	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
J 40	1-01158-120	73100-0195	Connector, BNC
J 50	1-01158-120	73100-0195	Connector, BNC
J 60	1-01158-120	73100-0195	Connector, BNC
J 61	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
J 62	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
J 70	1-01158-120	73100-0195	Connector, BNC
J 80	1-01158-120	73100-0195	Connector, BNC
J 90	1-01158-120	73100-0195	Connector, BNC
J 91	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
J 92	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
JP1	1-01199-131	6 POS.	Connector, Female
JP2	1-01199-131	6 POS.	Connector, Female
JP3	1-01199-131	6 POS.	Connector, Female
JP100	1-01147-132	TLW-118-06-G-D	Header, DIP
JP101	1-01200-130	6 POS.	Connector, Male
JP102	1-01200-130	6 POS.	Connector, Male
JP103	1-01200-130	6 POS.	Connector, Male
L 100	6-00236-631	FR47	Ferrite bead, SMT
L 101	6-00236-631	FR47	Ferrite bead, SMT
L 102	6-00236-631	FR47	Ferrite bead, SMT
L 103	6-00236-631	FR47	Ferrite bead, SMT

L 104	6-00236-631	FR47	Ferrite bead, SMT
PC1	7-01982-701	DG645 H/V RR	Printed Circuit Board
Q 10	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 11	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 20	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 21	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 30	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 31	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 40	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 41	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 50	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 51	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 60	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 61	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 70	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 71	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 80	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 81	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 90	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
Q 91	3-01663-360	PZT2907	Integrated Circuit (Surface Mount Pkg)
R 10	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 11	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 12	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 13	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 14	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 15	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 16	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 20	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 21	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 22	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 23	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 24	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 25	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 26	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 30	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 31	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 32	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 33	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 34	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 35	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 36	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 40	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 41	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 42	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 43	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 44	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 45	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 46	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 50	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 51	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 52	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 53	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 54	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 55	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 56	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 60	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 61	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 62	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 63	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 64	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 65	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 66	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor

R 70	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 71	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 72	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 73	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 74	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 75	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 76	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 80	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 81	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 82	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 83	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 84	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 85	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 86	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 90	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 91	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 92	4-00939-462	14.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 93	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 94	4-00925-462	10.0	Thin Film, 1%, 50 ppm, MELF Resistor
R 95	4-01088-462	499	Thin Film, 1%, 50 ppm, MELF Resistor
R 96	4-00997-462	56.2	Thin Film, 1%, 50 ppm, MELF Resistor
R 100	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 101	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01213-462	10.0K	Thin Film, 1%, 50 ppm, MELF Resistor
R 110	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 111	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 120	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 121	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 130	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 131	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 140	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 141	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 150	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 151	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 160	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 161	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 170	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 171	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 180	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 181	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 190	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 191	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
U 10	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 11	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 20	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 21	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 30	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 31	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 40	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 41	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 50	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 51	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 60	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 61	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 70	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 71	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 80	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 81	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 90	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 91	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 100	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 101	3-01252-360	74LVC1G00DBVR	Integrated Circuit (Surface Mount Pkg)

U 102	3-01203-360	SN74LVC1G08DBVR	Integrated Circuit (Surface Mount Pkg)
U 103	3-01867-360	74LVC2G74DCTR	Integrated Circuit (Surface Mount Pkg)
U 104	3-01881-360	DS1810R-5+T&R	Integrated Circuit (Surface Mount Pkg)
U 110	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 111	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 120	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 121	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 130	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 131	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 140	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 141	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 150	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 151	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 160	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 161	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 170	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 171	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 180	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 181	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
U 190	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 191	3-01853-360	74AHCT123APWR	Integrated Circuit (Surface Mount Pkg)
Z 0	0-01259-040	1/2" CUSTOM	Washer, Flat
Z 0	7-01882-720	DG645 BRACKET	Fabricated Part
Z 0	7-02021-721	BNC TOOL	Machined Part
Z 0	9-01570-917	SIM-PCB S/N	Product Labels

Option 3 Assembly

C 100	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 101	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 102	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 103	5-00611-578	4.7U - 16V X5R	SMT Ceramic Cap, all sizes
C 104	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 105	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 106	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 107	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 108	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 109	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 200	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 201	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 202	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 300	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 301	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 302	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 400	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 401	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
C 402	5-00299-568	.1U	Cap, Ceramic 50V SMT (1206) +/-10% X7R
J 200	1-01158-120	73100-0195	Connector, BNC
J 201	1-01158-120	73100-0195	Connector, BNC
J 202	1-01158-120	73100-0195	Connector, BNC
J 300	1-01158-120	73100-0195	Connector, BNC
J 301	1-01158-120	73100-0195	Connector, BNC
J 302	1-01158-120	73100-0195	Connector, BNC
J 400	1-01158-120	73100-0195	Connector, BNC
J 401	1-01158-120	73100-0195	Connector, BNC
J 402	1-01158-120	73100-0195	Connector, BNC
JP100	1-01147-132	TLW-118-06-G-D	Header, DIP
JP101	1-01200-130	6 POS.	Connector, Male
JP102	1-01200-130	6 POS.	Connector, Male
JP103	1-01200-130	6 POS.	Connector, Male
JP200	1-01199-131	6 POS.	Connector, Female

JP300	1-01199-131	6 POS.	Connector, Female
JP400	1-01199-131	6 POS.	Connector, Female
L 100	6-00236-631	FR47	Ferrite bead, SMT
L 200	6-00236-631	FR47	Ferrite bead, SMT
L 201	6-00236-631	FR47	Ferrite bead, SMT
L 202	6-00236-631	FR47	Ferrite bead, SMT
L 300	6-00236-631	FR47	Ferrite bead, SMT
L 301	6-00236-631	FR47	Ferrite bead, SMT
L 302	6-00236-631	FR47	Ferrite bead, SMT
L 400	6-00236-631	FR47	Ferrite bead, SMT
L 401	6-00236-631	FR47	Ferrite bead, SMT
L 402	6-00236-631	FR47	Ferrite bead, SMT
M 200	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
M 201	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
M 300	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
M 301	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
M 400	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
M 401	0-00241-021	4-40X3/16PP	Screw, Panhead Phillips
R 101	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 102	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 103	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 104	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 105	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 106	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 107	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 108	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 109	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 110	4-01117-462	1.00K	Thin Film, 1%, 50 ppm, MELF Resistor
R 111	4-01021-462	100	Thin Film, 1%, 50 ppm, MELF Resistor
R 200	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 201	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 202	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 203	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 204	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 205	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 300	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 301	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 302	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 303	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 304	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 305	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 400	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 401	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 402	4-00988-462	45.3	Thin Film, 1%, 50 ppm, MELF Resistor
R 403	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 404	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
R 405	4-01423-461	4.7	Thick Film, 5%, 200 ppm, Chip Resistor
U 100	3-01184-360	LP2985AIM5-3.3	Integrated Circuit (Surface Mount Pkg)
U 101	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 102	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 103	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 104	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 105	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 106	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 107	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 108	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 109	3-01770-360	65LVDS2DBV	Integrated Circuit (Surface Mount Pkg)
U 110	3-01854-360	74LVC1G86DBVR	Integrated Circuit (Surface Mount Pkg)
U 111	3-01854-360	74LVC1G86DBVR	Integrated Circuit (Surface Mount Pkg)
U 112	3-01854-360	74LVC1G86DBVR	Integrated Circuit (Surface Mount Pkg)
U 113	3-01854-360	74LVC1G86DBVR	Integrated Circuit (Surface Mount Pkg)
U 114	3-01854-360	74LVC1G86DBVR	Integrated Circuit (Surface Mount Pkg)

U 115	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 116	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 117	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 118	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 119	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 120	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 121	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 122	3-01798-360	74LVC2G32DCTR	Integrated Circuit (Surface Mount Pkg)
U 125	3-01252-360	74LVC1G00DBVR	Integrated Circuit (Surface Mount Pkg)
U 126	3-01203-360	SN74LVC1G08DBVR	Integrated Circuit (Surface Mount Pkg)
U 127	3-01867-360	74LVC2G74DCTR	Integrated Circuit (Surface Mount Pkg)
U 128	3-01203-360	SN74LVC1G08DBVR	Integrated Circuit (Surface Mount Pkg)
U 129	3-01203-360	SN74LVC1G08DBVR	Integrated Circuit (Surface Mount Pkg)
U 130	3-01203-360	SN74LVC1G08DBVR	Integrated Circuit (Surface Mount Pkg)
U 131	3-01881-360	DS1810R-5+T&R	Integrated Circuit (Surface Mount Pkg)
U 200	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 201	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 202	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 203	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 204	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 205	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 300	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 301	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 302	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 303	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 304	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 305	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 400	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 401	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 402	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 403	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
U 404	3-01855-360	TC7SET08F	Integrated Circuit (Surface Mount Pkg)
U 405	3-01852-360	74LVC3G34DCTR	Integrated Circuit (Surface Mount Pkg)
Z 0	0-01259-040	1/2" CUSTOM	Washer, Flat
Z 0	7-02021-721	BNC TOOL	Machined Part
Z 0	9-01570-917	SIM-PCB S/N	Product Labels
Z 1	7-01882-720	DG645 BRACKET	Fabricated Part
Z 2	7-01882-720	DG645 BRACKET	Fabricated Part
Z 3	7-01882-720	DG645 BRACKET	Fabricated Part
Z 4	7-01994-701	DG645 OPTION	Printed Circuit Board

Option 4 Assembly

J 1	1-01078-150	SSW-107-01-S-S	Socket, THRU-HOLE
J 3	1-01058-131	09-52-3101	Connector, Female
PC1	7-01586-701	CG635 TIMEBASE	Printed Circuit Board
R 1	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 2	4-00158-407	2.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 3	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 4	4-00148-407	12.1K	Resistor, Metal Film, 1/8W, 1%, 50PPM
U 1	3-00508-340	LM358	Integrated Circuit (Thru-hole Pkg)
Z 0	0-00048-011	6-32 KEP	Nut, Kep
Z 0	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 0	0-01090-031	3403	Standoff
Z 0	1-01057-130	26-48-1101	Connector, Male
Z 0	6-00079-624	SC10-24V - CG	Oscillator, Misc.
Z 0	7-01614-720	CG635	Fabricated Part

Option 5 Assembly

C 1	5-00023-529	.1U	Cap, Monolythic Ceramic, 50V, 20%, Z5U
J 2	1-00342-165	10 PIN STRAIGHT	Connector, D-Sub, Female
J 2A	1-00343-100	COAX CONTACT	Connector, Misc.
J 3	1-01058-131	09-52-3101	Connector, Female
PC1	7-01586-701	CG635 TIMEBASE	Printed Circuit Board
R 1	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 2	4-00158-407	2.00K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 3	4-00176-407	3.01K	Resistor, Metal Film, 1/8W, 1%, 50PPM
R 4	4-00148-407	12.1K	Resistor, Metal Film, 1/8W, 1%, 50PPM
U 1	3-00508-340	LM358	Integrated Circuit (Thru-hole Pkg)
U 2	3-00155-340	74HC04	Integrated Circuit (Thru-hole Pkg)
U 3	3-00116-325	78L05	Transistor, TO-92 Package
Z 0	0-00043-011	4-40 KEP	Nut, Kep
Z 0	0-00187-021	4-40X1/4PP	Screw, Panhead Phillips
Z 0	0-00781-031	4-40X1/4 M/F	Standoff
Z 0	1-01057-130	26-48-1101	Connector, Male
Z 0	6-00159-624	SRS RB OSC.	Oscillator, Misc.
Z 0	7-01614-720	CG635	Fabricated Part

Schematics

DG645 Schematic Diagram List

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3	FPGA	DG_MB_FPGA
4	100 MHz Timebase	DG_MB_TIMEBASE
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6	Time to Amplitude Converter	DG_MB_TAC
7	T0-T1 Vernier Ramps	DG_MB_VERNIER_T01
8	AB Vernier Ramps	DG_MB_VERNIER_AB
9	CD Vernier Ramps	DG_MB_VERNIER_CD
10	EF Vernier Ramps	DG_MB_VERNIER_EF
11	GH Vernier Ramps	DG_MB_VERNIER_GH
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21	AB Output Driver	DG_DR3C
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23	EF Output Driver	DG_DR5C
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