Alpha Processor Byte and Bit Ordering
The alpha processor is a 64 bit machine which places the least significant byte of multi-byte quantities at the lowest numerical memory address. This mapping is shown below.

L1 Trigger Bit Order
To ensure correct and fast decoding of the L1 trigger bits, when received by the L2 global, the bits must be arranged such that bit 0 is the least significant bit of the byte in the lowest memory location and that bit 127 is the most significant bit of the final memory location. This is shown below.