Notes on connections from real setup to test stand:
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**Question:** How does "toy" L3 system get informed about next event coming
Is this done by software, or is some board required?

Prefer real *L1, L2 accept/reject information* to test stand:
3 SCL cables running to the 3 crates
  outbound: standard L1/L2 messages
    all such sent if no L2 running; else copy of what sent to L2 crates
    will get into some trouble if these don't match data transmission
    plug into normal Pilot MBT's
back path: busy from each as needed (for resynch if test stand behind)

  fallback:
  SFO fanout from one of the MBT's in the test stand crate, or even from L2 in MCH
  This would require special initialization of the MBT: turn off L1 accept channel
  Plug SFO copy of L1 accept channel in another MBT channel, and set it's destination ID
to the one usually used by channel 0

*L2 accept behavior in test stand:*
  L3 R/O of test stand MUST be controlled locally in the test stand
  Since a local L3 is there for data taking

*Preprocessor Standalone:*
Administrator of crate must decide
  Could use L1 qualifiers (eg Unbias Sample)
  Could prescale, or write all events, depending on rate

*Global Standalone*
All inputs captured
Crate will see real L2 decision, and its own decision
Based on these two can choose whether to do L3 R/O
  If Global worker failed event, Adm must do ALL R/O!! (tricky--fixed VME address)

*Global + preprocessor(s)*
Auxiliary circuitry connects crates
Hardware support required is TSI circuitry, and possibly driver/receiver
L2 accept to preprocessors from Global:
  J2 drive (2 pins)
  J2 receive (2 pins)
  16 deep fifo to simulate mbt l2 decision fifo ok (if pins available)
  put on pins not normally used (if pins avail)
purpose: control of L3 readout for preprocessors
  probably CAN'T write to L3 at 10 KHz
Vertical interconnect is a fallback to this
  Requires VME poll--more different from usual software