Agenda

- SLIC 20 Fortner
- MBT 15 Baden
- Alpha 15 Martin
- Test 20 Linnemann
- Monitoring 15 Adams/Yasuda
- Milestones 15 Moore
  - slack 20

Michigan State University
4/14/99
L2 Trigger

L1: $E_T$ towers, tracks consistent with e, $\mu$, j

L2: Combines objects into e, $\mu$, j

(w/o STT)
Standard Crate

TCC  ←  MBus  ←  VME  ←  MPM  ←  VBD  ←  Worker  ←  Admin  ←  MBT  ←  MBus  ←  Inputs

L3  ←  7 VME slots minimum
up to 5 workers per crate
short (non-CDF) MBus

Dec Alpha
(Unix)

→  SCL
→  Outputs to Global
(preprocessors only)
→  L2 HWFW
(Global only)

→  L2 Answer
→  128

Michigan State University 4/14/99
JTL, MSU 12/18/97
Standard Crate with SLIC

10 VME slots minimum

Dec Alpha
(Unix)

Inputs
SCL
Outputs to Global

Inputs

MBus

TCC
L3
Standard Crate with FIC to MBT

9 VME slots minimum

Inputs

Dec Alpha
(Unix)

Outputs to Global

SCL

TCC
L3

VME

MPM

VBD

FIC

Worker

Admin

MBus

MBT
Standard Crate with FIC to SLIC

11 VME slots minimum

Dec Alpha
(Unix)

Inputs
SCL
Outputs to Global

JTL, MSU 12/18/97
Trigger Connections

Si Trker

Cu-Cypress 160 Mb/s
~150
Cu-AMCC 1.4 Gb/s
~280

L1 CFT
Broad
FE

L1 FPS
Broad
FE

MUON

Fi-Glink 1.3 Gb/s 20-bit

Fi-Glink 288
1.3 Gb/s, 20-bit

L2STT
(In Design)

Fi-Glink 1.3 Gb/s 20-bit

L2CTT
(FIC/MBT)

L2PS
(FIC/MBT)

L2G
(MBT)

Cu-AMCC
1.4 Gb/s

Cu-Cypress
160 Mb/s

MGR

L1 μ

L2μ
(SLIC/MBT)

CIC

L2CAL
(FIC/MBT)

Fi-Glink
1.3 Gb/s, 20-bit
Test Stand at FNAL

- **4 crates:**
  - Global simulator (Admin + Worker)
    - or CTT...
  - 2 preprocessor simulators (A+2W, A+W+Slic)
  - 1 data source (2alphas, MBT’s; own MBus)

- **Incomplete system--**
  - no L1, L2
  - not enough parts for full code of any/all crates
    - except maybe full playback for Global
    - could reconfigure if need be--painful!

- **Copy of some real-time inputs? (grounding!?)**
Test Stand: What can it do?

- (Pre-)Commissioning/debugging  (protoypes?)
  - alpha-alpha, alpha-MBT, SLIC-MBT-alpha issues

- Timing, verification of download (Alpha, SLIC)
  - run in real environment; count clock cycles
    - how good is offline simulator? (SLIC code differs…)

- Playback
  - drop data into memory (input only: cheap event dump?)
  - testing pre-release after running in simulator

- Debugging
  - event dump and restart (else debug = deadtime)
  - pretty tough to dump event unless Linux???
When do we want things?

- Crates on order, but 3 months
  - more spares from Marvin?
  - shuffle crates at Saclay, MSU, UIC, UMd, Nevis?

- Mbus backplane order ready to send to Myron
  - waiting on me! Hope not such a long leadtime...

- No power yet (may need design work...)
  - power requirements for cards not yet firm!
  - Need to sequence 5V vs 3V power???
  - Too much 3 V power for card pins?
    - Grab user bus?

- Bit3 617/618?
  - Order soon--618 problems traced to bad PCI crate
Fake Data Functionality
For each(?) L2 crate in MCH:

- Copy of Alpha’s or 1 SLIC’s inputs
  - outputs captured at Global if needed...
- extra transmitter in or near each real crate
  - redefine SFO to 1 in, 12 out, OR 6 in, 12 out
  - up to 3 slots per crate needed
  - extra cabling
    - sfo has extra input cables (female connector end??)
    - sfo has short output cables (copied input)
    - sfo has long output cables (to window in MCH)

- Recabling
  - how often can we afford to move it
  - moveable cabling vs lockable door, neat layout?
Cabling in sending crate: Logical (Alpha inputs)

Normal

Copied Data

Forward

Withdrawn
Moveable Counting House

L2 Test

Forward

Withdrawn
Alpha Inputs: Physical

- Move Cable Bundles from MBT to SFO?
  - 7 inputs MBT; 6 inputs SFO
- Input cables to SFO unbundled, with female connector dangling?
- Short output cables of SFO unbundled, with male connector dangling?
- Space may be tight if > 3 workers
  - 2 to 3 SFO’s needed per crate
Cabling in sending crate: Logical (SLIC inputs)

\[\text{CIC} \xrightarrow{2} \text{SLIC} \xrightarrow{\text{Normal}}\]

\[\text{CIC} \xrightarrow{2} \text{SFO} \rightarrow \text{SLIC} \xrightarrow{\text{Forward, Withdrawn}} \text{SLIC (SFO?)}\]

Copied Data
SLIC Inputs: Physical

- Cannot move Cable Bundles from SLIC to SFO
  - incompatible # inputs, 2 inputs per cable on SLIC
- Short input cables to SFO unbundled, with female connector dangling?
  - Connections to SFO split 1 cable to 2 inputs
- Short output cables of SFO unbundled, with male connector dangling?
  - Connection to SFO split 1 cable to 2 outputs
- SFO needs different cable bundles for copying SLIC vs copying MBT inputs (BOTH of possible interest!)
- No spare room in central muon crate for 2-3 SFO’s!
  - share with forward? SFO’s in CIC crate?
Fake data receiving:
Test Stand End

- Two sets of long input cables to each test stand crate
  - one for each wall window (positions of MCH)
  - SFO receiver and short cables needed too?
    - If SLIC can’t receive long-haul cables…
    - at least, SLIC needs another set of short cables:
      - pairs of 1-signal female to 2-single male
  - repeat this setup for 3 (4?) test stand crates

- Assuming NOT attempting an optical split:
  - copy FIC outputs, not inputs
Test Stand Concerns

- **Grounding**
  - transformer coupling from MBT inputs
    - SLIC capacitor coupled???
    - Had assumed only short-run inputs to SLIC
    - SLIC’s close to Calorimeter ADC’s (analog)
    - Use SFO receiver with transformer + short cable?

- **Cable Length: error rate**

- **Cable topology**
  - MBT inputs have one input per cable
  - SLIC inputs have two channels per cable
    - get around with special forked cables?
    - Patch panel?
    - *(dangerous)* redefine everybody else to be 2-input?
Added functionality to support test data import

- Return busy to L2 crates (Pilot MBT)
  - stop data to resynchronize after debugging
  - otherwise, keep up, or let data fall on floor

- a branch of L3 needed to record test data?
  - And matching control system!
  - fake TCC: script from Coor or online dbase?
    - Global, or if software qualifiers for preprocessors

- Is there anything else we’ve forgotten?
  - SCL info? L1HWFW data? Fake these?

- Software: special/unofficial releases...
L2 Test Stand Layout?
2nd floor, North Wall

- Cabinet
- Work Bench
- Rack 1
- Rack 2
- Desk
Needs coordination!

- Mario Vaz will coordinate engineering of test stand
## Test Stand Data Copy

### Cost Estimate (ROUGH)

#### TEST STAND SETUP

<table>
<thead>
<tr>
<th>1 crate:</th>
<th>number</th>
<th>length</th>
<th>cost</th>
<th>Total Crates</th>
<th>3</th>
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<td>SFO</td>
<td>3</td>
<td>1500</td>
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<td>4500 needed?</td>
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<td>cables</td>
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<tr>
<td>in to hole 1</td>
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<td>75</td>
<td>59</td>
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<tr>
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<td>75</td>
<td>59</td>
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<td>total</td>
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Counting house setup

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<th>number</th>
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<th>cost</th>
<th>Total Crates</th>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>total</td>
<td>2808</td>
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</table>

| SFO      | 24     | 12000  |
| cables   | 304    | 12972  |
| total    |        | 24972  |
## Data Source Count

### L2 Data Types and Source ID's

4/14/99 JTL  
DRAFT

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<tr>
<th>GS Crate/ID</th>
<th>Contents</th>
<th>Data Source</th>
<th>Contents</th>
<th>Data Source</th>
<th>Contents</th>
<th>Data Source</th>
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### Outputs:

- mu central
- mu forward
- em
- jet
- etmiss
- pt track
- impact track
- ps central
- ps north
- ps south
- zvtx

Michigan State University  4/14/99
## Crates/Test Stand Schedule

<table>
<thead>
<tr>
<th>Crate #</th>
<th>Date</th>
<th>Usage</th>
<th>Date</th>
<th>Usage</th>
<th>Date</th>
<th>Usage</th>
<th>Date</th>
<th>Usage</th>
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<td>1</td>
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<td>MSU Swe</td>
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<td>UIC Swe</td>
<td>Aug-99</td>
<td>UIC Alpha</td>
<td>Jan-00</td>
<td>Test/Pre2</td>
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<td>Jun-98</td>
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<td>Jan-00</td>
<td>CFT</td>
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<td>5</td>
<td>Jan-99</td>
<td>Nevis SLIC/STT</td>
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<td>Jul-00</td>
<td>Spare</td>
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<tr>
<td>6</td>
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<td>BU STT?</td>
<td></td>
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<td>Jul-00</td>
<td>Spare</td>
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<td>Mu Central</td>
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<td>Aug 99</td>
<td>NebraskaCIC/SFO?</td>
<td>Jan-00</td>
<td>PS</td>
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</tbody>
</table>

**Test Stand at FNAL:**

- **global-like**: admin+worker
- **Pre1**: admin+2 workers
- **Pre2**: admin+2 slic + worker + 2fic
- **data/testing**: alpha+2 MBT’s + various warm spares; useable for testing/repair with extenders

NOTE: Proposed Eventual configuration. Details may vary.
Common Controls

- **VME: 2 levels of reset for specific card**
  - 1) Initialize This Card (simulate power cycle)
    - after safety catch released?
  - 2) reset this card (only) don’t reload FPGA, but
    - go to state 0 and discontinue all activity
    - clear data buffers
    - need not clear control registers; let Alpha reprogram?

- **VME SYSRESET:**
  - would prefer this just cleared bus?? Or job of Bit3?
  - believe VBD does full reset on this, too

- **VME SYSFAIL**
  - prefer to do nothing (except Administrator…)
  - want to use as interrupt for SCL_INITIALIZE from MBT to Admin

- **MBReset**
  - drop Mbus cycle
More common stuff...

- Register to read current FPGA code version(s)?
  - Not clear how important…
  - but DO want version control, maybe with code put in CVS repository, and change dates to database…

- geo addressing to set base address

- NO POWER ORDER DEPENDENCE
  - take care of it on your card if you have to

- front panel button: simulate power cycle