The Standard L2 Crate

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Michigan State University
FNAL L2 Workshop
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7 VME slots minimum

Dec Alpha
(Unix)
Standard Crate
VME Slot Assignments

1: Bit3 (Crate Controller) no J3 (1 slot)
2: VBD (2 signals from J3 to Admin)
   – through hole in blank Mbus
3-6 J3 connector for VTM
   • up to 4 FIC’s, or any non-MBus cards (SLIC/SFO)
7-21 J3 Magic Bus:
   • 20-21 Administrator (all Alphas 2 slots)
   • 19 Pilot MBT (preproc. : 1MBT for 2 Workers)
   • 18 down [Assistant MBT as needed]
     • [need 1 MBT per 2 Workers for output]
   • 7-8 up up to 5 Workers (or non-MBus cards)
Bit3 MPM

- To PCI of a PC; VME master, crate controller
- Add Multiport Memory Module
- Perform general VME I/O, generate interrupts
- Download parameters for run
- Run begin/end commands
- Collect Monitoring information
  - preferably, already placed in MPM by Administrator Alpha
  - If necessary, can collect from other modules
VBD

- VME Master to read out to L3
- Not interruptable during Readout
- Probably 10-20 MB/s effective
- Must read from SAME set of VME addresses every event
  - some of wordcounts may be zero
  - faster if fewer addresses
  - intent is readout from Worker Alpha
Alphas

- Up to 1 GIP Alpha 21164 on VME card
  - small local disk for bootup
  - Enet to Dec Unix Alpha for user .EXE, debugging

- All Mbus I/O via MBT card
  - Mbus DMA input 80-100 MB/s
  - Mbus bidirectional programmed I/O 20 MB/s?

- 64-128b parallel I/O

- 2 per crate
  - Worker formatting, Output to Global
  - Administrator housekeeping, L3 R/O
MBT
Magic Bus Transceiver

- Vme slave; Mbus Master and slave
  - Administrator controls card(s)
- 7 Cypress Hotlink inputs
  - 160 or 320 MB/s in Copper Cables
  - broadcast to Alphas (Workers & Admin) on Mbus
  - normal data Input path
- 3 Cypress Outputs
  - 2 Preprocessor outputs to L2 Global input MBT’s
  - 1 Echo of L1 SCL info
Serial Command Link (SCL) Receiver
- broadcast L1 to Alphas on Mbus
  - synchronization check
  - L1 Qualifiers
  - echo’d on Cypress output for SLIC
- Queue L2 for Administrator Mbus reads

128 b Parallel I/O
- Global uses to send L2 decision to L2 HWFW
- Misc communication/control signals (VBD?)
Standard Crate Uses

- Global JUST Standard Crate described so far
- Cal: more workers
- Standard Crate can also be used with non-Alpha, non-MBus pre-preprocessor
  - Cypress inputs to Worker via MBT
    - format, massage data for Global
  - handle L2, L3 buffering & I/O, most of monitoring
  - *Completely standard data movement software*
    - *User code testable once data structure fixed*
  - Penalty: extra latency (lose a buffer)
    - “*pre-preprocessor*”
SLIC:
Serial Link Input Card

- 16 Cypress serial inputs
  - 1-slot VME slave card
  - 4 TI DSP’s, up to 2 GIPS each
- more inputs, CPU / slot than Alpha
- output via Hotlink to MBT
- Readout via Worker Alpha via MBT
  - Acts as pre-preprocessor
- test registers on all inputs (eg. SCL)
SFO: SCL Fanout

- Receives L1 SCL information
  - from MBT as Cypress Hotlink
- Fans out as Cypress output to 12 SLIC cards
  - event synchronization
  - L1 Qualifiers
- purely analog fanout
Standard Crate with SLIC

10 VME slots minimum

Inputs
SCL
Outputs to Global

Dec Alpha
(Unix)
Fiber Input Converter (FIC)

- Convert Fiber Input to Cu Cypress Hotlink
  - G-link input 16b data in 20b data frame (24b total)
    - input thru J3 by standard VTM transition module
  - Cypress 160 out
- Front end to *either* SLIC or MBT
  - avoids variants of complex card
- VME used for control, monitoring
- 4 independent channels per card
Standard Crate with FIC to SLIC

11 VME slots minimum

Dec Alpha
(Unix)
Standard Crate with FIC to MBT

9 VME slots minimum

Dec Alpha
(Unix)

Outputs to Global

SCL

VME

TCC
L3

MBus

FIC

Worker

Admin

VBD

MPCM
FIC: L2CFT from 
L1 CFT trigger (& L1 Cal)

- Presently, plan g-link 1.3Gb/s = 100MB/s
  - L1CFT: 100B (50 tracks)/fiber to STT in 1 μs
    - L1CFT plans to send fixed length, pad w/ trailing zeros
    - add physical trailer with parity and error indication

- 4 g-link inputs per card max
- 8 fibers = 2 cards for L2CFT
FIC: Raw Data Input

- Split of raw data fiber *requires* 1.3 Gb/s g-link
- not needed currently
  - no cable count yet
  - use as part of STT?
    - More likely, recycle part of VRB input
MBT Simplifications:

*are* all sources intelligent?

- Enforce padding to 16 B? No?
  - probably can’t if accepting raw data

- Enforce maximum event size? Try.
  - Input FIFOs hold 16 worst-case M+P events
    - need definition from EVERY know source
  - Truncate if overflow anyway (no marker added!)
    - In-band marker makes assumptions about data formats!
    - OK *if* processors can recognize w/o extra work
      - OK for L2-formatted inputs (trailers broken)
      - what about raw fiber data?

- SAME issues for SLIC inputs
MBT Testing Questions

- **VME OR MBus**
  - Control/Setup
  - Fake data for inputs, outputs
  - Loopback test of output(s) to inputs at full speed
    - VME readback of filled FIFO’s needed

- **MBus only: need MBus, Alphas**
  - Broadcast input test
  - Parallel I/O test
  - Mbus Control/Setup

- **SCL Test Jig?**
  - SCL L1 formatting + standard input
  - SCL L2: need Alpha?
  - Check with SCL designers: Walter Knopf in Barsotti group
Development System Questions

- Digital Unix Alpha required for debugging
  - compile, link at any Alpha; serve disk anywhere?

- Most user software needs only simulator with correct data format and buffer structure
  - should build into simulator

- Data movement software from Global & Cal
  - MINOR modifications
    - specific qualifiers needed
How long do which systems stay at home?

- Current estimate is 50K for a Standard Crate
- Attempt communication with Global before commissioning—requires extra development crate
- Timing may force production of Alpha cards early
  – lose potential for later speedup?
Test Stand at Fermi

- Global, Cal-like, Mu/Track-like, Data Source
- Incomplete system--
  - no HWFW
  - not enough parts for full code of any/all crates
    - except maybe full playback for Global
    - could reconfigure if need be--painful!
# L2 Parts Count

12/18/97 18:43

<table>
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<tr>
<th></th>
<th>PC</th>
<th>Alpha</th>
<th>MBT</th>
<th>SLIC</th>
<th>SCL Falt</th>
<th>Fiber</th>
<th>Bit3</th>
<th>MPM</th>
<th>VBD</th>
<th>Cables</th>
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## Count of Standard Parts

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<tr>
<th></th>
<th>Global</th>
<th>Cal</th>
<th>Mu/Tracking</th>
<th>Less Cal Development</th>
<th>Spares</th>
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<td>Fiber Bit3 MPM VBD Cables Crate Mbus Power Cooling Cost</td>
<td>1 2 2 0 0 0 1 1 16 1 1 1 0.5</td>
<td>49400</td>
<td>0 3 1 0 0 0 1 1 3 1 1 1 0.5</td>
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<td>1 4 3 0 0 0 2 1 21 2 2 2 1</td>
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<td>MSU</td>
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<td>0 4 2 0 0 0 1 0 3 1 1 1 0</td>
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<td>UMD</td>
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<tr>
<td>System</td>
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<td>1 4 4 4 2 2 2 2 2 100 2 2 2 2</td>
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<table>
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<tr>
<th></th>
<th>System</th>
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<th>Totals Parts (w/ STT)</th>
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<tbody>
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<td>1 4 3 0 0 0 2 1 21 2 2 2 1</td>
<td>89700</td>
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