L2 Status

James T. Linnemann
MSU
Trigger Meeting
February 1, 2001
L2 Status: Who

Hardware
- focus on component cards
- preprocessors assembled from shared components

Installation/Commissioning
- MCH
- Test Stand
- Vertical slices

Online Software
- Simulation:

STT
- After rollin (no more this talk)
(Baseline) L2 Cards & Names

build/ operate

- **FIC**  
  G-link to Hotlink  
  Renardy, Mur (Saclay)  
  Buehler, Kostas, Heinmiller (UIC) Kwarciany (FNAL)

- **MBT**  
  Hotlink, MBus, other I/O  
  Giganti, Bard, Baden (Maryland) +Toole/ Schwienhorst

- **Alpha**  
  main processor  
  (Campbell, Miller UM);  
  Buehler, Heinmiller, Kostas, Varelas (UIC)  
  Hirosky (UVa)  
  Kwarciany/Zmuda (FNAL)

- **SLIC**  
  Processor  
  Sippach, Evans (Nevis/Columbia)  
  Kothari, Christos (CU); Maciel, Fortner, Uzunyan (NIU)

- **CIC, SFO**  
  SMB to RJ45 Hotlink; Hotlink fanout  
  Lewis, Snow (Nebraska)  
  Tester: Johns (UAZ)  
  Hansen, Baldin, (Anderson) FNAL  
  Maciel, Kothari, Fortner

- **VBD; Bit3**  
  L3, TCC  
  Zeller, Cutts; Commercial  
  Mattingly (Brown); Schwienhorst (MSU)
Infrastructure
(and status)

🌿 Power, Cooling Baum (UMd)
- All except muon CIC crate done (end February)
- ORC’s in **February/March**?
  ? Documentation is mostly in place

🌿 Patch Panel Baum (UMd)
- MCH window done; Test Stand in **Feb/March**

🌿 Cabling Maciel/Sergei (NIU)
  - laying input cables in MCH for muon **Feb**
  - cabling intra-crate **February/March**
  - building muon pigtails
  - cables to test stand **February/March**
Cards Done

- in normal data mode and commissioning modes
- **BUT** BIST errors to SLIC
  - Replace mismatched signal path with UTP cable
  - 3 repaired at Saclay
  - verify OK, then rest at Fermi?
- Anomalies in VME interface?
  - ABEL to FPGA compiler problems, complicating corrections

Support from UIC
5 pre-production cards in hand, tested (2 at Fermi)

25 to be checked by end March

- New postdoc Terry Toole mid-Feb

VHDL “90% done”: estimate mid March

- SCL handling (including init) how complex?
- Programmed I/O cleanup
- Broadcast cleanup
- Monitoring
- Documentation: as-needed; estimate mid-June

Some manpower conflicts with “Beta” fallback plan
Alpha Status

-board count
- 2 preproduction (+ 1 CDF) worked within 1 week
- Production: Many problems to fix (3 months 2EE + 2PhD)
  - 2 of 24 production fully functional
  - 4 having VME BGA replaced (now understood)
  - Another 2-3 possible boards
  - CIA BGA not successfully replaced yet

Expect 6-11 on March 1
- Possibly more if CIA BGA problem understood, VME BGA yield high
  - Enough to start commissioning
  - Not enough for full 1st year L2: need 15 ( + 2 in test stand)

Build another 12 by May-June (start mid-Feb?)
## How Many Alphas?

15 + test stand in 2001

<table>
<thead>
<tr>
<th></th>
<th>baseline</th>
<th>1st year</th>
<th>&quot;minimum&quot;</th>
<th>min commission</th>
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<tbody>
<tr>
<td>Test Stand Crate 1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2 &quot;global&quot;</td>
</tr>
<tr>
<td>Test Stand Crate 2</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3 &quot;multiprocessor&quot;</td>
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<tr>
<td>Test Stand Crate 3</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td>0 2nd preprocessor test</td>
</tr>
<tr>
<td>Test Stand Crate 4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 data source uses prototypes</td>
</tr>
<tr>
<td>Global</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Cal</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>0 Oct</td>
</tr>
<tr>
<td>PS</td>
<td>3</td>
<td>3</td>
<td>2</td>
<td>0 Sept?</td>
</tr>
<tr>
<td>CTT</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>0 min is no stt; L1 in Sept?</td>
</tr>
<tr>
<td>Mu</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>2 one crate; L1 in June</td>
</tr>
<tr>
<td><strong>total</strong></td>
<td><strong>24</strong></td>
<td><strong>22</strong></td>
<td><strong>17</strong></td>
<td><strong>9 imaginable partial production</strong></td>
</tr>
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<tr>
<th></th>
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<tbody>
<tr>
<td>spare/extra power</td>
<td>14</td>
<td>16</td>
<td>21</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td>38</td>
<td>38</td>
<td>38</td>
<td>38</td>
</tr>
<tr>
<td>pre-production</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2 as good as final cards</td>
</tr>
<tr>
<td>spare parts</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10 but some needed by CDF too</td>
</tr>
<tr>
<td>old prototypes</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2 useable for testing</td>
</tr>
</tbody>
</table>

We don't have enough parts to build the system twice.
Could build all baseline workers twice

### Administrators:

<p>| | | | | |</p>
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<tr>
<th></th>
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<th></th>
</tr>
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<tbody>
<tr>
<td>test stand</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>real system</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>total admin</strong></td>
<td><strong>9</strong></td>
<td><strong>9</strong></td>
<td><strong>7</strong></td>
<td><strong>4</strong></td>
</tr>
<tr>
<td>workers</td>
<td>15</td>
<td>13</td>
<td><strong>10</strong></td>
<td>5</td>
</tr>
</tbody>
</table>

J. Linnemann, MSU

2/25/2001
Where do we put our Alphas?
Staging; rotating tests

Feb/March (6-11)
- 1 Maryland
- 2 Test Stand/UIC
- 2 Global
- 2 Mu/Cal (turns?)

April/May (6-23)
- 2 Test stand
- 2 Global
- 2-4 Mu
- 2-4 Cal
- 2-5 CTT,PS

- 3-4 in Cal, others
- 1-4 UIC/Test Stand
Alpha Risks

- Not long-term tested yet (fragile?)
- Some Mbus problems to repair yet (probably easier)
- Programmed I/O, Broadcast not shown at full speed
  - Need to be sure it’s FPGA, not board layout
- Have parts for 12 more boards (needed!)
  - Considering new raw board maker
    - Need touchup of Gerbers for BGA pads
    - Want I/O working, so sure no other changes!
  - Considering new assembler? Delay (proto at least)
    - Want to know why BGA’s died (VME, and worse, CIA)
      - Still diagnosing both kinds of failures
      - Warped PCB’s?
      - Assemble without them, than add later?
  - Real risks: will next assembly have better yield? Last shot
    - We have learned some reasons for bad yield
  - Schedule risks:
    - When will we know enough to build?
    - Take delay for new assembler?
    - How long to make new boards work?
Component recovery not very attractive
- Obsolete CIA’s may be dead
- Some other obsolete parts (sockets)
  - Recovery for sockets “harder”?
- Long lead time for other parts
  - Could just pay up and recover…

Hope not much longer to build beta?
- Commercial 6u VME CPU
  - More MIPS, but ½ raw PCI bandwidth
- CERN (based) PMC/PCI to Local Bus board
  - One DMA, one Programmed I/O
    - DMA near alpha’s… PIO latency?
- Beta “Motherboard” Custom
  - 9u, holds 6u CPU, PMC boards
  - Custom interfaces (Mbus etc) to Local Bus
    - U Mich work, but simpler bus interface than PCI
Betas?

- Rough plan (no holes)  January
- Document  March 1

  Conflict w/ Alpha I/O, build; MBT FPGA, driver; commissioning

- Pre-proto review?  March 15
  - Design, personnel, schedule, cost

- Prototype  “summer”

- Production  ?December?
  - Decide need, based on alpha experience
    - Run 2a, 1st year: enough alphas—if lucky
    - Run 2b, “extra power”, or replacement

Spare change, anyone?
Good news—all boards here!

- It’s a software problem now
- Basic Operating System done
- First algorithm tests (Mu Central) OK
  - Meet speed and efficiency requirements
- Deciding on monitoring scheme
CIC

- pre-production: 1 passes all tests, 1 not
  - $5 \times 10^{-12}$ BER with 3 channels, 2 boards
    - Possibly limited by Mu FE BER
  - Production/checkout: end March
    - Bare boards, components in hand
    - But assumes 2nd board's problems understood in 2 wk

- Now have 1 board to start commissioning

- Needed only by muon system

- Test Input Card (Johns): mid Feb
  - BIST ok and in use now
    - commissioning and CIC checkout
  - Need Programmable, multi-channel inputs to CIC
preproduction passes some tests
  - $5 \times 10^{-12}$ BER with 12 channels, 2 boards
  - Need to verify behavior with CIC as input
  - Components in hand; bare boards February(?)
  - Production/checkout by end April (CIC + 2-4 wk)
    ? Could interleave SFO checkout with CIC checkout

Needed by muon system, and for test stand

Now have 1-3 boards to start commissioning
Miscellaneous Interface Hardware

- 16 to 128 bit mux add-on to MBT (UMd)
  - Returns L2 trigger mask to L2HWFW  Feb
- L1HWFW to L2 Global (via FIC) (MSU)
  - Transmits L1 trigger mask  Feb/March
  - Piggyback on L1 VRB readout
- Monitoring of Alphas by L1 Scalers (MSU)
  - Passive cable formatting card  March/April
  - Card, cabling under design
Commissioning

Limiting factors:

- Manpower (trained)
  - Big conflict with
    - Prototype testing (MBT, CIC, SFO)
    - Production debugging (Alpha)
    - Beta (fallback plan for Alpha)
- Working alphas
  - Alpha firmware issues vs. Alpha board debugging
- ORC for Installed infrastructure (power, cabling…)
  - Hope relieved by end of month
- to lesser extent, MBT’s with full functionality
- Alpha software for commissioning
  - Limited, in turn, by above problems
- Inputs, CIC, SFO, FIC’s
Online Software ( & Risks)
Monitoring, Verification later!

Alpha:
- Much of structural software exists in simulation
  - Control/data flow for preprocessor and global
- Loader and modified Linux kernel
- Draft drivers/setup for MBT and event loop March/April
  - Some alpha firmware problems?
  - SCL_INIT, and DAQ interface
- VME driver, buffer allocation
  - VBD/L3 readout beginning Feb/March
- Error logging and beginnings of monitoring: End Feb
- Downloading, release to Worker Feb/April
- Admin/Worker control; data flow March/May

SLIC:
- Basic operating system in place
  - Code moving to CVS; testing download scheme
  - Monitoring interface to alpha: planning March/May


<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Dates in simulator</th>
</tr>
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<tbody>
<tr>
<td>Mu</td>
<td>L1 Fmt;; Central, Fwd segment merge tables, DSP Segment Finders:</td>
</tr>
<tr>
<td></td>
<td>Jan</td>
</tr>
<tr>
<td>CTT</td>
<td>not quite yet</td>
</tr>
<tr>
<td></td>
<td>Feb?</td>
</tr>
<tr>
<td></td>
<td>then tau (Mihalcea/Abbott) / slow movers(who?)</td>
</tr>
<tr>
<td></td>
<td>Jun? / ?</td>
</tr>
<tr>
<td>PS</td>
<td>more work needed</td>
</tr>
<tr>
<td></td>
<td>Jan</td>
</tr>
<tr>
<td></td>
<td>FPS</td>
</tr>
<tr>
<td></td>
<td>Mar/Apr?</td>
</tr>
<tr>
<td>Cal</td>
<td>= Run 1B L1.5 Iso under discussion</td>
</tr>
<tr>
<td></td>
<td>Jan</td>
</tr>
<tr>
<td></td>
<td>merge needs work</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MET = L1</td>
</tr>
<tr>
<td>Global</td>
<td>now limited by lack of CTT,mu</td>
</tr>
<tr>
<td></td>
<td>Jan</td>
</tr>
<tr>
<td></td>
<td>e(cal,cps), j(cal); deta, dphi (e: fps, ctt ready)</td>
</tr>
<tr>
<td></td>
<td>Feb(Mar)</td>
</tr>
<tr>
<td></td>
<td>Ht, MET (mass)</td>
</tr>
<tr>
<td></td>
<td>Apr/May?</td>
</tr>
<tr>
<td></td>
<td>Mu(with ctt); tau?</td>
</tr>
<tr>
<td>STT</td>
<td>(and new CTT)</td>
</tr>
<tr>
<td></td>
<td>Mar(Jul)?</td>
</tr>
</tbody>
</table>
Preprocessor Chains: Commissioning Scale

..20..40..60..80..100%

0% Connectivity not tested
20 Signal compatibility demonstrated
40 Correct data transfer once or usually; or physical layer (BIST?) full speed, error rate OK
60 Fake data, repeated transfers, error rate OK
80 Full speed fake data, error rate ok, >1 day
100% Real data full cards, in system, full speed, errors OK, > 1 week
Preprocessor Chains

0%..20%..40..60..80..100%

- L1DFE FIC SFO MBT Alpha L3 (test stand)
- L1Cal FIC SFO MBT Alpha VBD L3 (DAQ)
- Mu FE CIC SLIC SFO MBT Alpha L3
- Mutest CIC SFO SLIC SFO MBT Alpha L3
- Alpha MBT MBT Alpha (2 crates)
- Alpha Alpha
- L1SCL MBT Alpha
- MBT SFO patch panel MBT Alpha VBD L3 (test stand)
- L1SCL MBT SFO SLIC MBT Alpha
- L1FW FIC MBT Alpha
- Alpha MBT L2FW

....
Board Summary:

**Dates, Risks**

- **SLIC**
  - Monitoring software
  - January

- **Crates/Power/Cables**
  - ORC; CIC crates
  - Feb/March

- **FIC**
  - Communication; FPGA code; verify fixed
  - Feb/March?

- **MBT**
  - FPGA code; software driver
  - March/April

- **Alpha**
  - Understand CIA, Universe problems; verify full functionality
  - Feb; May; Fall/winter
  - Build 12 more when understood (production, yield)
  - Fallback: Beta—late this year (interferes w/ commissioning)

- **CIC**
  - March/April
  - Verify error rate (production)

- **SFO**
  - March/April
  - Verify error rate w/ CIC (production; can interleave checkout w/ CIC)
Time Line
ignoring input arrival

During February:
- Muon cabling; Restart slice tests, beginning with Muon

March
- Other intra-crate cabling, populating crates, ORC
- Fwd Muon, Cal, Global tests start
  - Few channels; CIC SFO SLIC; FIC MBT Alpha

April
- Muon, Cal, + Global (partial crates); L3 DAQ?
  - Try preprocessor to global?

May
- start PS and/or CTT
  - May have to time-share alphas
- 1 Muon crate fully functional (Cal + 2
nd Mu if enough alphas)

June: attempt triggering, monitoring/verification…
Personnel changes (past 6 mo)

- Saclay + Mur (FIC engineer)
- UIC - Hirosky, + Heinmiller, Kostas (alpha, Cal)
  - Nikos full time (replacing Hirosky)
- UVa + Hirosky + Steele
- Maryland – Toback + Toole
  - CTT: - Toback + Mihalcea, Abbott et. al. (UOk)
- MSU + Schweinhorst; Columbia + Christos
  - Commissioning and L2 Muon
- Muon: + Christiansen; Trefzger, Strohmer, Schaile (Munich)
- +3 grad students on-site (1 UIC, 2 MSU)
- Lack of project engineer has slowed progress.
  - Rich Kwarciany (CD) helped as on-call consultant
    - Alpha debugging with Zmuda
  - Anderson, Baldin, Hansen: CIC/SFO consultants
  - Johnny Green: alpha board help
Manpower Needs

- Engineer (+ tech) to assist L2 debugging & integration.
  - Escalation of valuable on-call arrangement?
  - Many cards w/o physicists on site
  - Trying to cross train (limits: experience, docs)

- Software:
  - Monitoring: online, comparisons, examines, releases
  - Physics studies of L2 algorithms