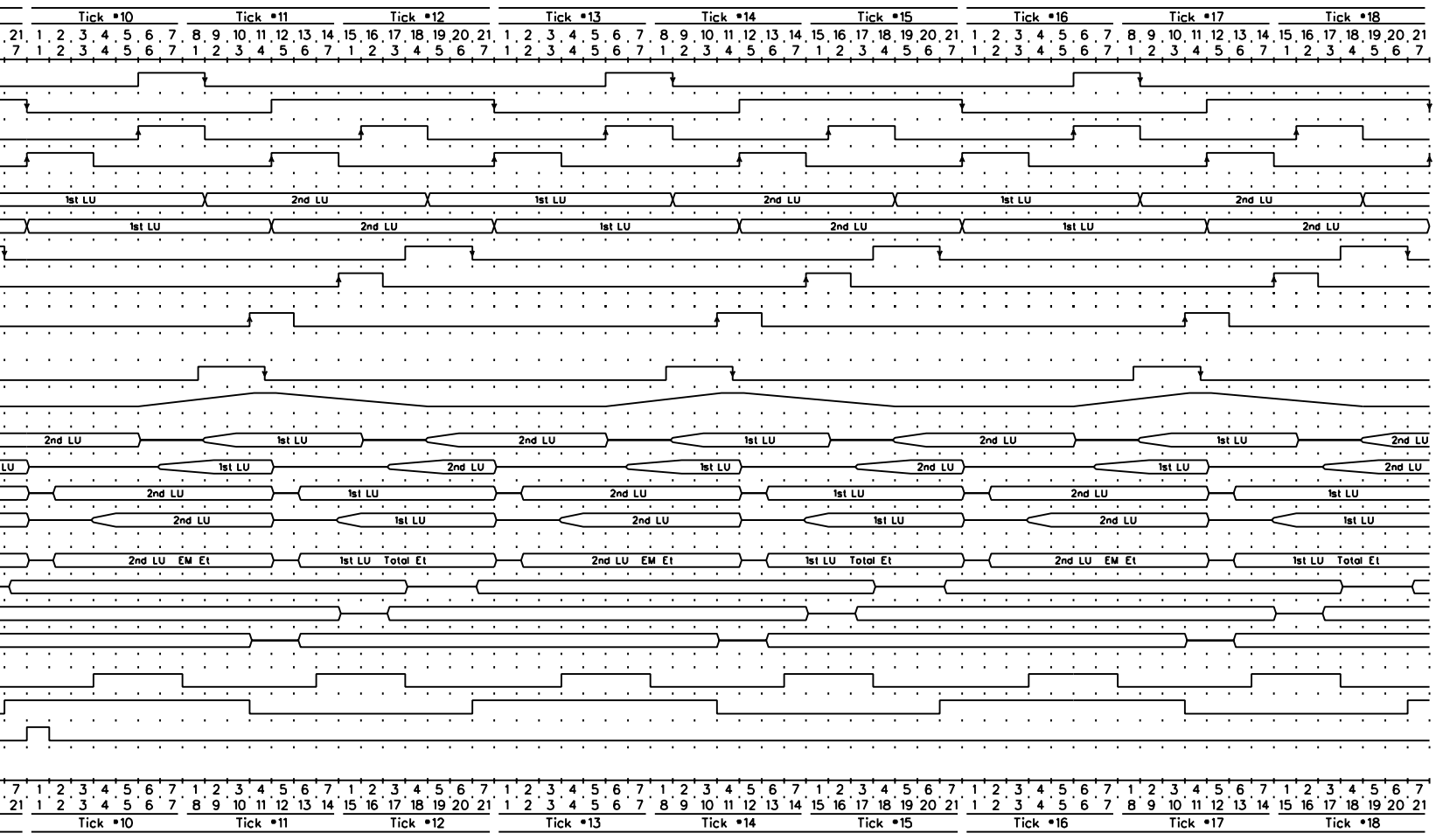
Calorimeter Trigger Tier 1 and ERPB Timing Diagram



TIME LINE	TIME LINE FUNCTION	
0	ADC Clock	CMC
1	Latch-Shift	CMC
2	2X Clock	CMC
3	X Clock	CMC
4	Energy LU Page Select	CMC
5	Momentum LU Page Select	CMC
6	CHTCR Clock	CMC
7	Energy Adder Tree Tier 1 CAT2 Clock	CMC
8	Momentum Adder Tree Tier 1 CAT2 Clock	CMC
9		
10	Typical Delayed ADC Clock	
11	Typical Trigger Pickoff	
12	Brd Total Energy Output	
13	Brd Total Momentum Output	
14	EM Et Comp Output	
15	Total Et Comp Outputs	
16	Trg Twr "Total Et" Output to the ERPB card.	
17	Measured CHTCR Output	
18	Tier 1 Energy Adder Tree CAT2 Output	
19	Tier 1 Momentum Adder Tree CAT2 Output	
20	ERPB Input_Clk	CMC
21	ERPB EM/Total	CMC
22	Mark the Latch-Shift that starts processing 1st Real BX	CMC
nc		

in the Cal_Trig_Readout_Helper FPGA, the ERPB_Input_Clk _Tot_Clk actually occur about 20 nsec later, with respect 2, and Tier 3 signals, than shown in this diagram.

Because of Cable, FanOut, and MBD Delays in the Timing & Control Signals to Tier 1, Tier 2 and Tier 3, the outputs from Tier 1, Tier 2, and Tier 3 are really about 50 nsec later, with respect to Sub System Strobe, than shown in this diagram.

CMC → Generated by Carmen Master Clock on the Indicated Time Line

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