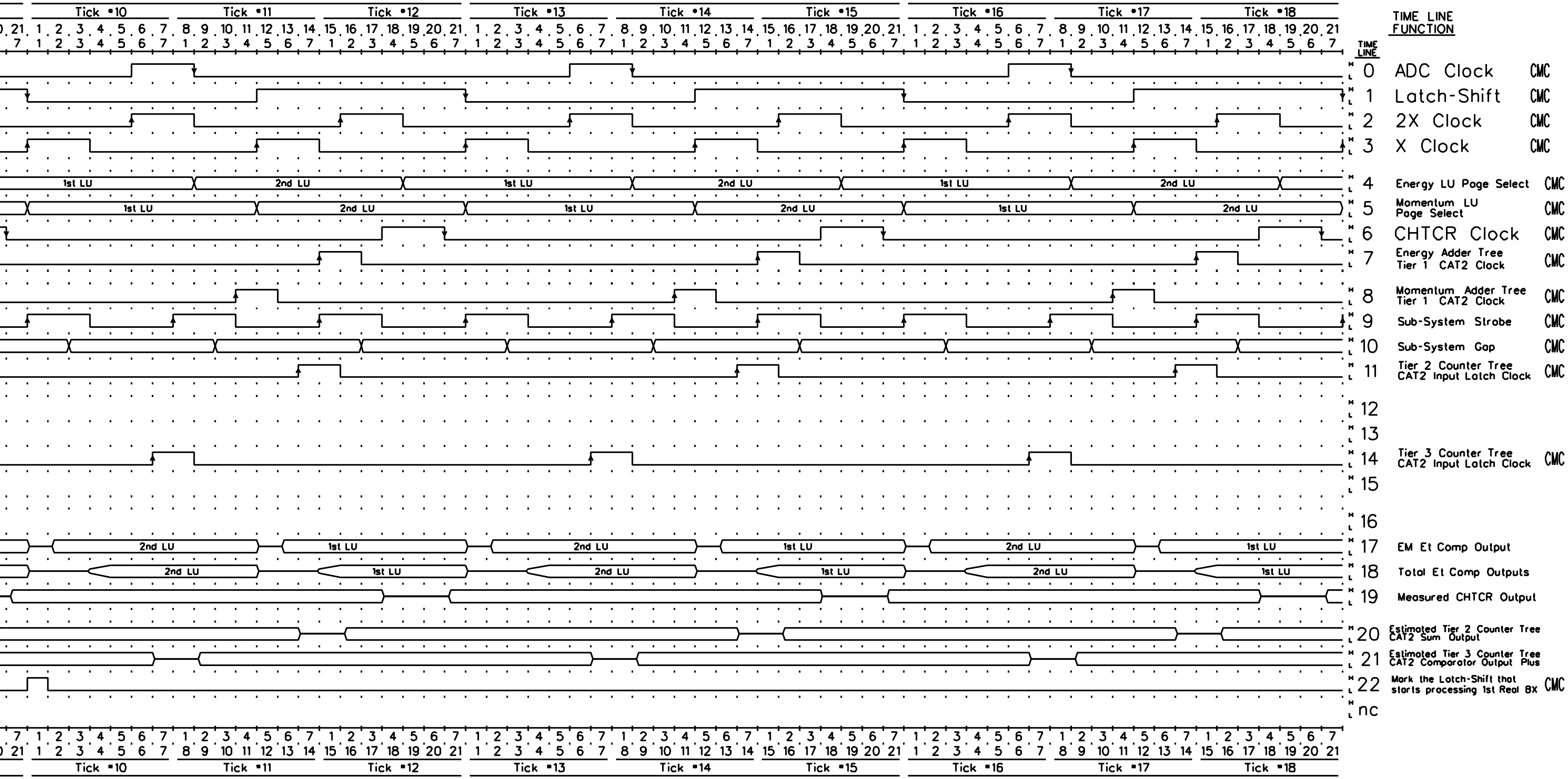
Calorimeter Trigger Tier 1 and Counter Tree Timing Diagram


Tick •10
Tick •11
Tick •12
Tick •13
Tick •14
Tick •15
Tick •16
Tick •17
Tick •18
TIME LINE
TIME LINE FUNCTION
0 ADC Clock CMC
1 Latch-Shift CMC
2 2X Clock CMC
3 X Clock CMC
4 Energy LU Page Select CMC
5 Momentum LU Page Select CMC
6 CHTCR Clock CMC
7 Energy Adder Tree Tier 1 CAT2 Clock CMC
8 Momentum Adder Tree Tier 1 CAT2 Clock CMC
9 Sub-System Strobe CMC
10 Sub-System Gap CMC
11 Tier 2 Counter Tree CAT2 Input Latch Clock CMC
12
13
14 Tier 3 Counter Tree CAT2 Input Latch Clock CMC
15
16
17 EM Et Comp Output
18 Total Et Comp Outputs
19 Measured CHTCR Output
20 Estimated Tier 2 Counter Tree CAT2 Sum Output
21 Estimated Tier 3 Counter Tree CAT2 Comparator Output Plus
22 Mark the Latch-Shift that starts processing 1st Real BX CMC
nc
1st LU
2nd LU
H
L

in the Cal_Trig_Readout_Helper FPGA, the ERPB_Input_Clk
l_Tot_Clk actually occur about 20 nsec later, with respect
2, and Tier 3 signals, than shown in this diagram.

Because of Cable, FanOut, and MBD Delays in the Timing & Control Signals to
Tier 1, Tier 2 and Tier 3, the outputs from Tier 1, Tier 2, and Tier 3 are really
about 50 nsec later, with respect to Sub System Strobe, than shown in this diagram.

CMC → Generated by Carmen
Master Clock on the
Indicated Time Line

Date: 11-OCT-02