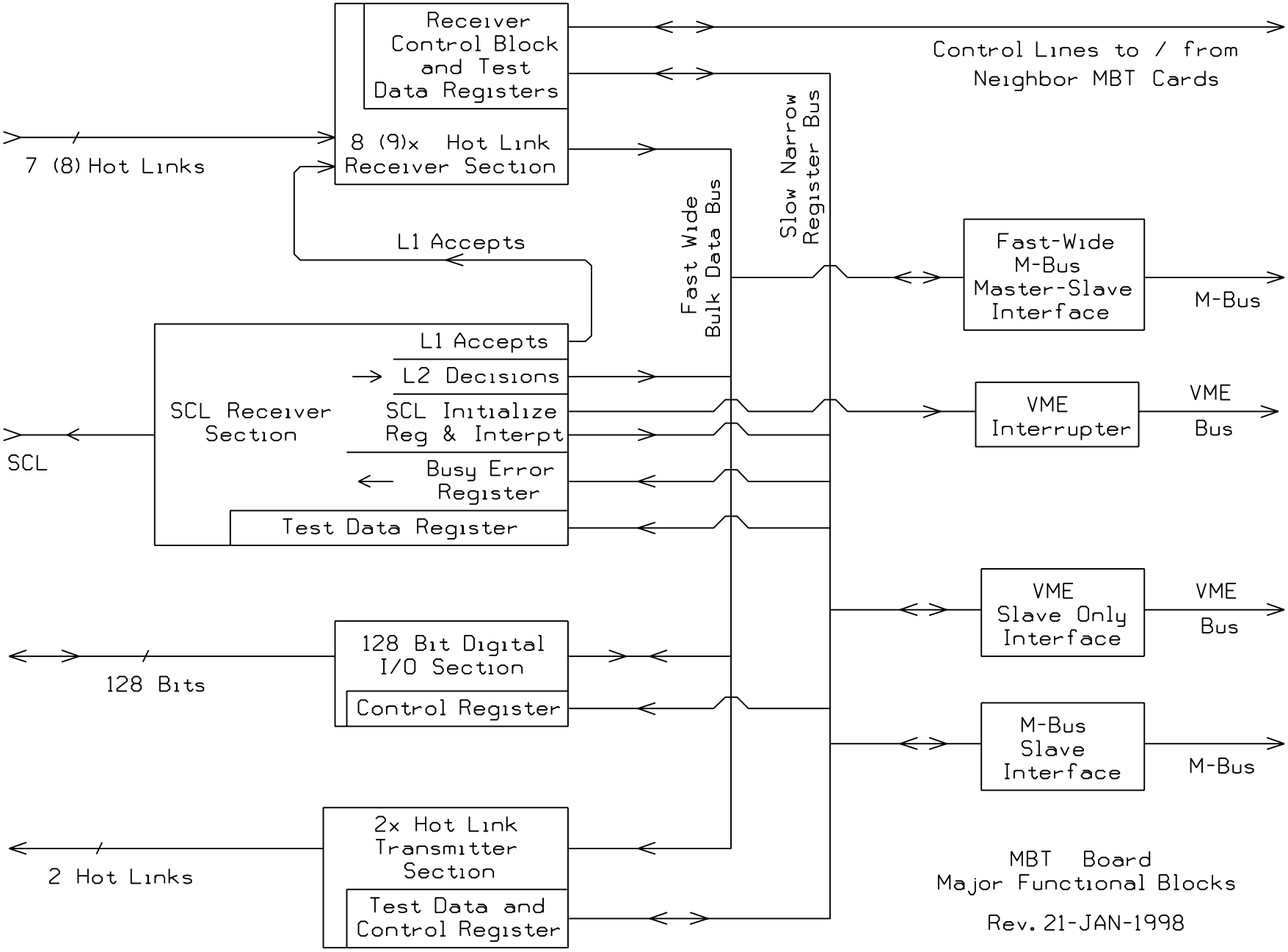
Receiver Control Block and Test Data Registers
8 (9)x Hot Link Receiver Section
7 (8) Hot Links
Control Lines to / from Neighbor MBT Cards
Slow Narrow Register Bus
Fast Wide Bulk Data Bus
L1 Accepts
Fast-Wide M-Bus Master-Slave Interface
M-Bus
L1 Accepts
L2 Decisions
SCL Receiver Section
SCL Initialize Reg & Interpt
Busy Error Register
Test Data Register
SCL
VME Interrupter
VME Bus
VME Slave Only Interface
VME Bus
128 Bit Digital I/O Section
Control Register
128 Bits
M-Bus Slave Interface
M-Bus
2x Hot Link Transmitter Section
Test Data and Control Register
2 Hot Links
MBT Board
Major Functional Blocks
Rev. 21-JAN-1998