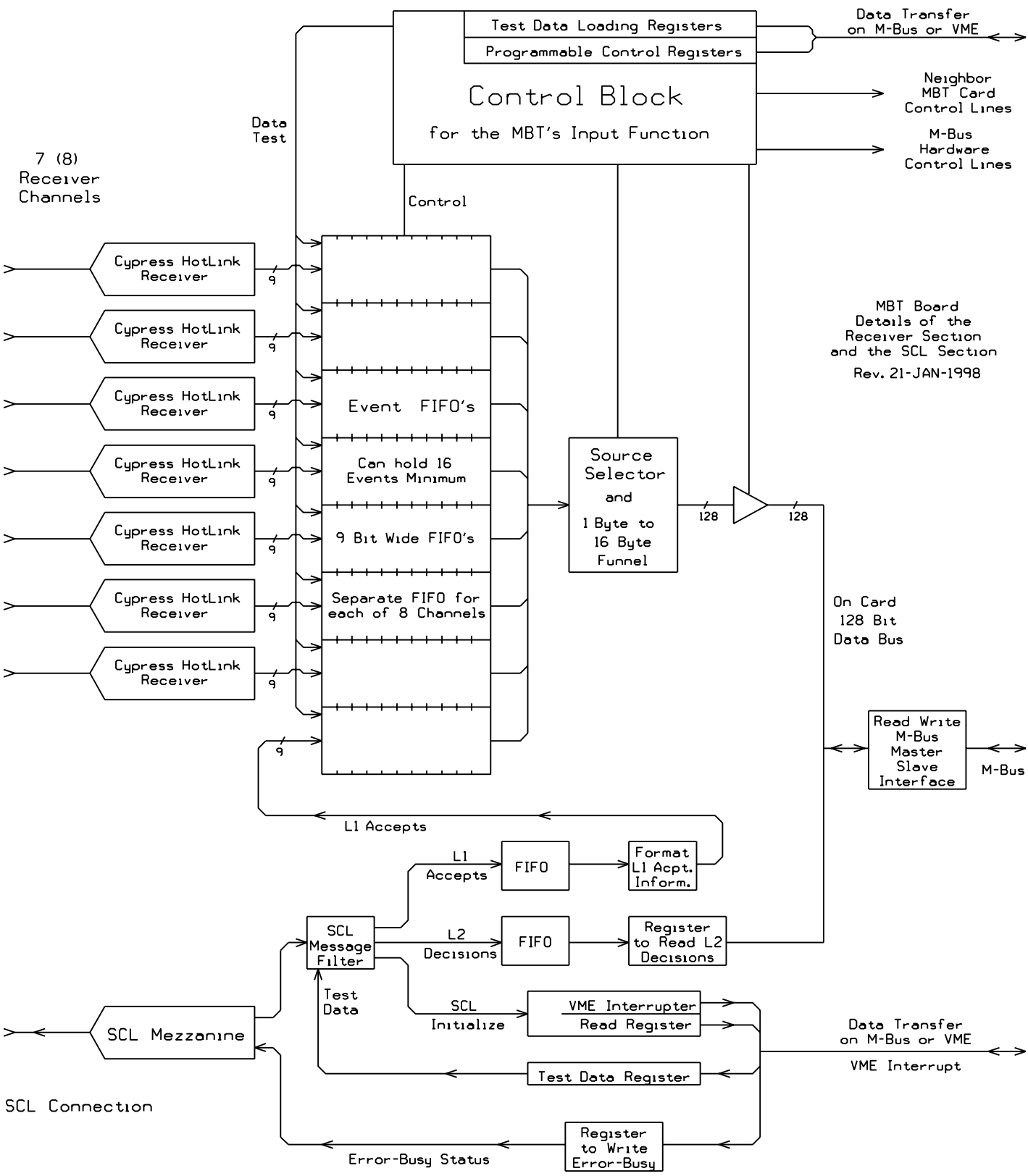
Test Data Loading Registers
Programmable Control Registers
Control Block
for the MBT's Input Function
Data Transfer on M-Bus or VME
Neighbor MBT Card Control Lines
M-Bus Hardware Control Lines
Data Test
Control
7 (8) Receiver Channels
Cypress HotLink Receiver
9
Event FIFO's
Can hold 16 Events Minimum
9 Bit Wide FIFO's
Separate FIFO for each of 8 Channels
Source Selector and 1 Byte to 16 Byte Funnel
128
128
MBT Board Details of the Receiver Section and the SCL Section
Rev. 21-JAN-1998
On Card 128 Bit Data Bus
Read Write M-Bus Master Slave Interface
M-Bus
L1 Accepts
L1 Accepts
FIFO
Format L1 Acpt. Inform.
SCL Message Filter
L2 Decisions
FIFO
Register to Read L2 Decisions
Test Data
SCL Initialize
VME Interrupter
Read Register
SCL Mezzanine
Data Transfer on M-Bus or VME
VME Interrupt
Test Data Register
SCL Connection
Register to Write Error-Busy
Error-Busy Status