Data Transport from L2 Preprocessors to L2 Global Stage

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- We need to use a common method for all L2 Preprocessors to send their data to the L2 Global Stage.

  1. All L2 Preprocessors use the same data format for sending their information to the L2 Global Stage as described in:
     http://www.pa.msu.edu/hep/d0/ftp/l2/data-transfer/global-input-format.doc
  2. All L2 Preprocessors use the same electrical link for transporting their data to the L2 Global Stage.

- Desired characteristics of the L2 Preprocessor to Global Stage data link.

  1. Must be able to transport about 20 MBytes/sec on the link. This is 10,000 events per sec x 1 kByte max from a given Preprocessor per event x factor of 2 for safety.
  2. An L2 Preprocessor should always be able to send its results form a given event as soon as it has finished processing that event. An L2 Preprocessor should never be blocked because the L2 Global Stage is not ready to absorb its data.
  3. The L2 Preprocessors do not run event synchronously so the data transport system to the Global Stage should not impose event synchronization.
  4. The data transport link to L2 Global must not mix up the pieces of an event even though it is transporting pieces of different events at the same time.
  5. These links may be physically long so we can not have a byte by byte handshake transfer. It must be a "data push" transfer.
  6. The L2 Preprocessor (the sending end of the link) must signal to the L2 Global (the receiving end of the link) when it has transferred all of its data for a given event.
  7. The L2 Global end of the link may need to signal to the L2 Preprocessor end of the link when it is OK for the Preprocessor to begin sending its data for the next event.

     It may be better to just design the receiving end of the link so that it guarantees that "k" usec after receiving the last data from a Preprocessor for event "N" it is OK for that Preprocessor to begin sending its data for event "N+1".

     In this way we would not need a back channel for flow control. This would just be an "event push" link.

- Transfer into the Main Memory of the Alpha Processor boards

  1. At the L2 Global crate data from the L2 Preprocessors will be received by a "link receiver card" and transferred over the Global crate's Magic-Bus to the Alpha processor node(s).
  2. A transfer from a link receiver card, over Magic-Bus, to the Alpha processor node(s) may be event synchronous or not event synchronous.

     CDF will use event synchronous transfers. Using non event synchronous transfers way will pester the Alpha processor with many interrupts in order to control the flow of various pieces of different events all at the same time.
  3. In order to allow the Preprocessors to send data to Global Stage asynchronously and still use the Magic-Bus for event synchronous transfers to the Alpha processor node(s), the link receiver card(s) will need to be able to buffer events.

     Adding event buffering to the link receiver card(s) should not be expensive. It is only a small amount of memory (a few kBytes per event times 17 events).

     For other technical reasons the link receiver card(s) will need to be able to buffer at least one event anyway.

     Adding event buffering to the link receiver card(s) may make the overall job of flow control and event synchronization easier and more robust.
  4. A transfer from a link receiver card, over Magic-Bus, to the Alpha processor node(s) may target any subset of the node(s) in the crate to receive the data.
  5. The link receiver card initiates the transfers over the Magic-Bus. A transfer contains in its "address": which processor nodes should receive the data, what source (i.e. which L2 Preprocessor) the data is coming from, and what event the data is coming from.

     The Alpha processor node uses the "data source field" and the "event number field" in the "address" to control where it stores the data from the transfer in its main memory.
  6. The link receiver card will have to add these three address fields (i.e. data source, event number, node target list) to the information that it receives from the L2 Preprocessor.

     This requires a sequential (packed) L1 trigger number. Data received from the L2 Preprocessors will contain the Serial Command Link Geographic Section L1 Trigger Number but not a sequential L1 trigger number.

     The L1 Framework has a sequential packed L1 trigger number that can be used for this. An Alpha node in the Global crate (the administrator node) will verify that the Geographic Section L1 Trigger Numbers contained in the data blocks from the various L2 Preprocessors match the Geographic Section L1 Trigger Number of the event that the Global Stage is processing.
  7. If the L2 Global Stage administrator node see a mismatch in Geographic Section L1 Trigger Numbers it can signal an error in its geographic section.

     To correct such an error will require that all L1 triggers be stopped, and all events that have not completed L2 processing be drained from the system.

- What can we buy ? What are we forced to design and build ?

  1. A 20 MByte per second link does not require a fancy serial link but we may want to use a serial link if we can take advantage of some standard Run II equipment.
  2. Link Receiver Card (Global end)

     I expect that the link receiver card is something that we must design and build. As I currently understand things, the CDF link receiver will not work at D-Zero because they use centralized buffer control, and their link receiver will not buffer events. There is little hope of finding a commercial "Magic-Bus card".
  3. Link Driver Card (Preprocessor end)

     Can all L2 Preprocessors use the same link driver card?

     Can we agree that the link driver will get the Preprocessor's data over VME ?

     Could this just be a dumb commercial VME (VME-64) DRV-11J that is a VME slave and use a DMA engine on the L2 Preprocessor it get the data?
  4. What commercial products or D-Zero Run II products or links designed for other purposes can we use for the Preprocessor to Global connection?

The next page shows the general layout of the data link from the L2 Preprocessors to the L2 Global Stage. Shown at the top is a sketch of what information needs to flow between these systems. The lower part of the drawing shows the link receiver with input event buffers using the M-Bus to send data to the Alpha processor nodes.

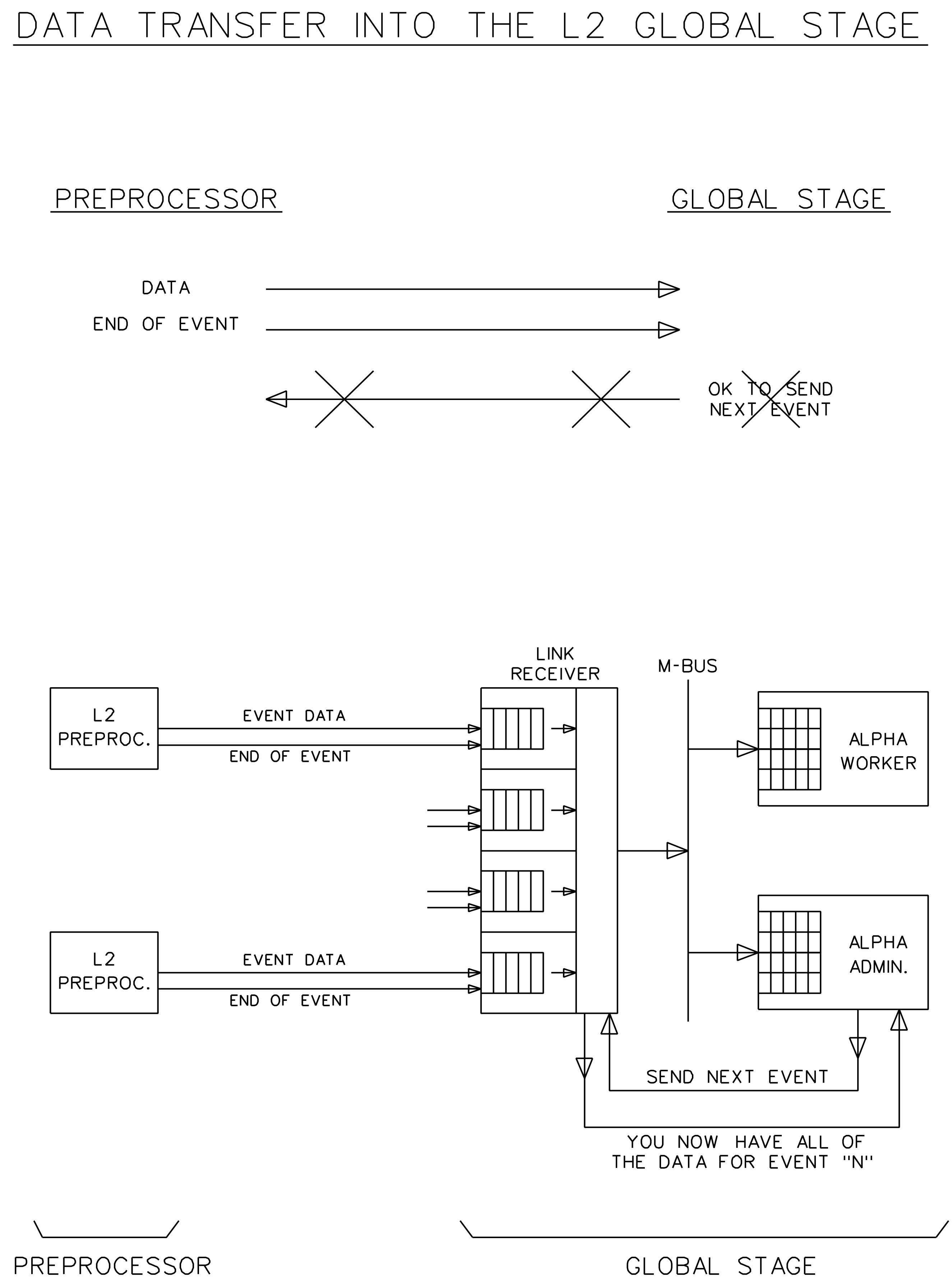

Figure 1: Data Transfer to the L2 Global Stage