The D0 Global Level 2 Trigger

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Timing Test on Frame

- Start with existing L3 frame
- remove unused features:
  - » zebra bank book/link find
  - » timing of scripts, tools
  - » filter subroutine calls
  - » timeout, out of space code
  - » “try as needed”
  - » L1.5 unbiased
- generate real script on VAX
- run on script in Alpha

More on Timing Test

- Always pass the tool
  - » about X 2 too many calls
- 3-4 L1 bits/event randomly
  - » 1-3 expected: X 2 too many
- 90 bit L2 x 32 bit L1 masks
  - » 64 L1 bits-> reorder loop
- Counters in full detail
- Fortran arrays(i,j,k) used

SO

PROBABLY X 5-10 too slow!

What is projected L3 output

10 - 20 Hz

Timing Results (3-10 X too slow)

VAX M60		Int 92 11.1	1300 μsec
α064 300L	100 MHz	46	110
500X	200	111	52
700	225	163	44
α164	500?	600?	20-10?

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M76: Int92 is 7.1; 2060 microsec

M90: Int92 is about 16 (estimated) , though specmark and FP ratio is more like 2.7; we saw 2.2 to 2.7 in filtering code

Extrapolation to final processor

- MHz, not Int92 scaling
  - » if code,data in cache
- MHz => X 2.2 Safe
- '164/'064 chip: X 1.5?
- OSF/VMS: X 1.2??
- Overall: X 2.2 -4 on speed
- Code: X 3-10

L2 ~ L3 frame in Global !

=> "no" L2 Hdwe Frame?

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Estimated factor from timing on Alpha 300 to 700 is thus 225/150 = 1.5

Last time I took 2 X 1.5 = 3 to get from 300 to final "500"

Now I would estimate 1.5 X 2.2 = 3.3

L2 Featuritis: What L3 to drop?

- Easiest to give up:
  - Counts by L1 bits
  - L2 SET, Unbias bits
  - Pass 1 of n (Monitor) independent on each L2 bit
- Have to think more:
  - Last tool run for each L2 bit
  - Counts by L2 tool
- Possible Physics Impact:

Single L2 bit for each L1 bit?

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pass 1 of n: can't overemphasize muons

but can still separate bits: just or "unbias" mask at end

L1 bit counts not needed if bits not e expanded in L2

L2SET covered by:

fixed processing order

last to run, if stopped

"aborted" bit

counts by: simulator has all counts?? this is most questionable

If no L2 bit expansion, no need for prescale

Prescaling Issues

- No need if L2 bits = L1bits
- If used, may need multiple settings
- Saturate BW by “Dynamic” prescaling? (used by CDF)
  - » bandwidth or fraction goal
  - » lum or Hz measurement to set
  - » feedback without oscillation
  - » VITAL to record scalars
  - » is it OK to vary L_{inst} during run, L2 bit by L2 bit?

Why drop features?

- Restrict escalation of control software from L1.5 -> L2
- Restrict number of bits to manage, and related databases and support, and monitoring
- Payoff:
  - faster frame
  - less manpower
  - more reliable

Single L2 bit for each L1 bit

- Refine L1 decision in L2
- Split L1 bits only in L3
- No reason to prescale in L2
- Rejection goal is ~10/bit

- If split L1 bits in L2 X (2-3):
- Rejection goal now 20-30/bit
- Is 1 overall Pass 1 of n rate adequate for efficiencies?

Cal Preprocessor Timing (μ sec)

	Electrons	Jets
Buffer Fill	13-50	13-50
Unpack L1 Seeds	2	2
Algorithm	3-10	8-30
Output	5	5

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2nd figure is for 132 nsec bunch spacing

Data input speed independent of processor; other factors scale

Times scaled from a model 300 Alpha, about 100 MIPS / 2 ~ M700

should be at least 1.5 X latest chip Vs. M700

in addition, UNIX C faster than VMS C

I have applied that scaling factor here

Global Processor Timing

- Data input: < 3 μsec
- .5-1.0 μsec / object
- 2-3 objects X few triggers => 10 μsec / event
- 10 μsec for formatting
- Total of 25 μsec (currently known tasks)

256 B/80 MB/sec = 3 usec or so (u is worst case)

Here timing is on M300/2, VMS C, so really expect * 1.5 better

but beware, this is 2* as fast as CDF saw for real

room for expansion here

mu track matching NOT included so far