The Standard L2 Crate

James T. Linnemann
Michigan State University

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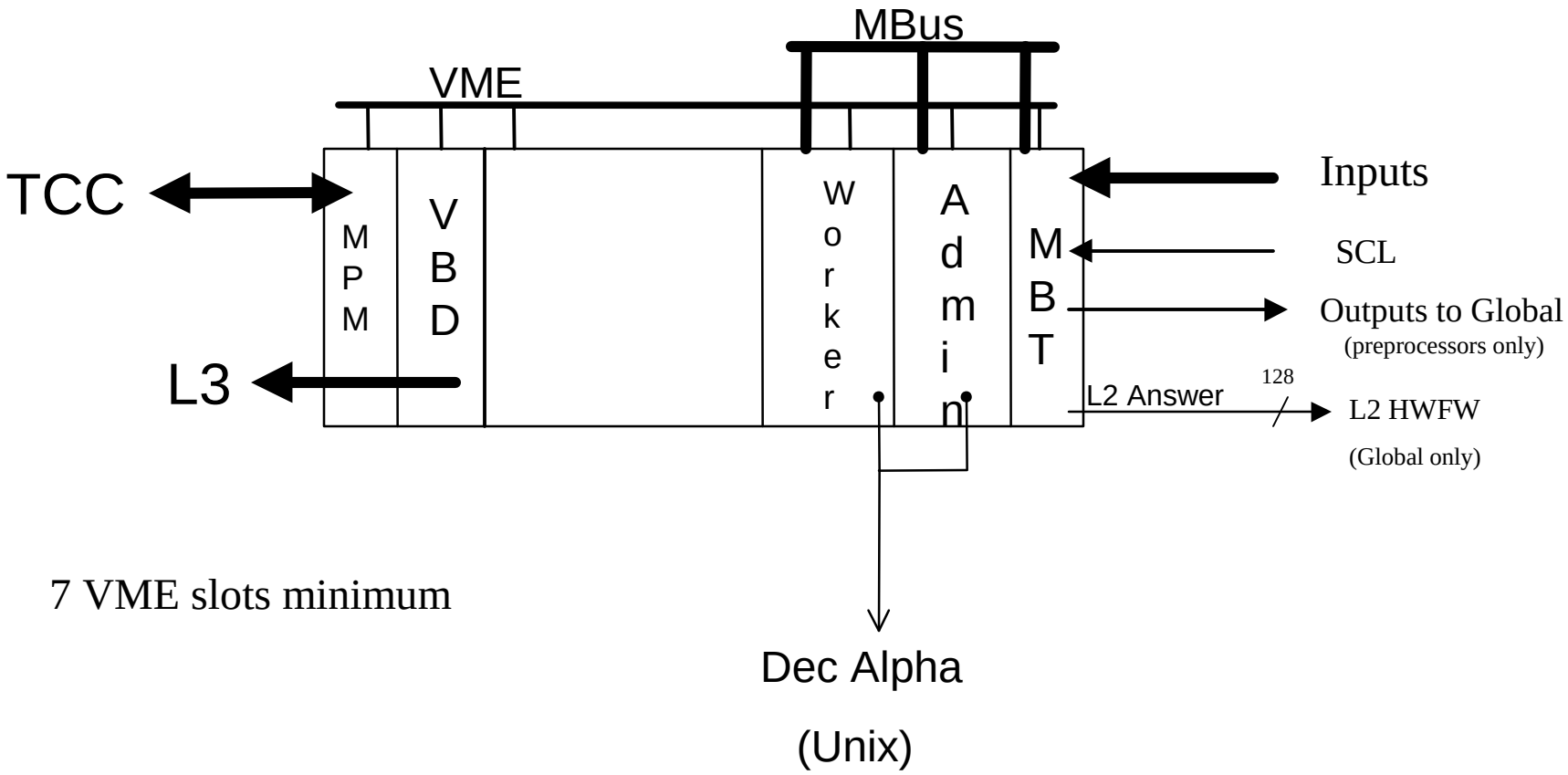
Standard Crate



JTL, MSU 12/18/97

Standard Crate VME Slot Assignments

- 1: Bit3 (Crate Controller) no J3 (1 slot)
- 2: VBD (2 signals from J3 to Admin)
  - through hole in blank Mbus
- 3-6 J3 connector for VTM
  - up to 4 FIC's, or any non-MBus cards (SLIC/SFO)
- 7-21 J3 Magic Bus:
  - 20-21 Administrator (all Alphas 2 slots)
  - 19 Pilot MBT (preproc. : 1MBT for 2 Workers)
  - 18 down [Assistant MBT as needed]
    - [need 1 MBT per 2 Workers for output]
  - 7-8 up up to 5 Workers (or non-MBus cards)

Bit3 MPM

- To PCI of a PC; VME master,crate controller
- Add Multiport Memory Module
- Perform general VME I/O, generate interrupts
- Download parameters for run
- Run begin/end commands
- Collect Monitoring information
  - preferably, already placed in MPM by Administrator Alpha
  - If necessary, can collect from other modules

VBD

- VME Master to read out to L3
- Not interruptable during Readout
- Probably 10-20 MB/s effective
- Must read from SAME set of VME addresses every event
  - some of wordcounts may be zero
  - faster if fewer addresses
  - intent is readout from Worker Alpha

Alphas

- Up to 1 GIP Alpha 21164 on VME card
  - small local disk for bootup
  - Enet to Dec Unix Alpha for user .EXE, debugging
- All Mbus I/O via MBT card
  - Mbus DMA input 80-100 MB/s
  - Mbus bidirectional programmed I/O 20 MB/s?
- 64-128b parallel I/O
- 2 per crate
  - Worker formatting, Output to Global
  - Administrator housekeeping, L3 R/O

MBT
Magic Bus Transceiver

- Vme slave; Mbus Master and slave
  - Administrator controls card(s)
- 7 Cypress Hotlink inputs
  - 160 or 320 MB/s in Copper Cables
  - broadcast to Alphas (Workers & Admin) on Mbus
  - normal data Input path
- 3 Cypress Outputs
  - 2 Preprocessor outputs to L2 Global input MBT's
  - 1 Echo of L1 SCL info

MBT, continued

- Serial Command Link (SCL) Receiver
  - broadcast L1 to Alphas on Mbus
    - synchronization check
    - L1 Qualifiers
    - echo'd on Cypress output for SLIC
  - Queue L2 for Administrator Mbus reads
- 128 b Parallel I/O
  - Global uses to send L2 decision to L2 HWFW
  - Misc communication/control signals (VBD?)

Standard Crate Uses

- Global JUST Standard Crate described so far
- Cal: more workers
- Standard Crate can also be used with non-Alpha, non-MBus pre-preprocessor
  - Cypress inputs to Worker via MBT
    - format, massage data for Global
  - handle L2, L3 buffering & I/O, most of monitoring
  - *Completely standard data movement software*
    - *User code testable once data structure fixed*
  - Penalty: extra latency (lose a buffer)
    - *"pre-preprocessor"*

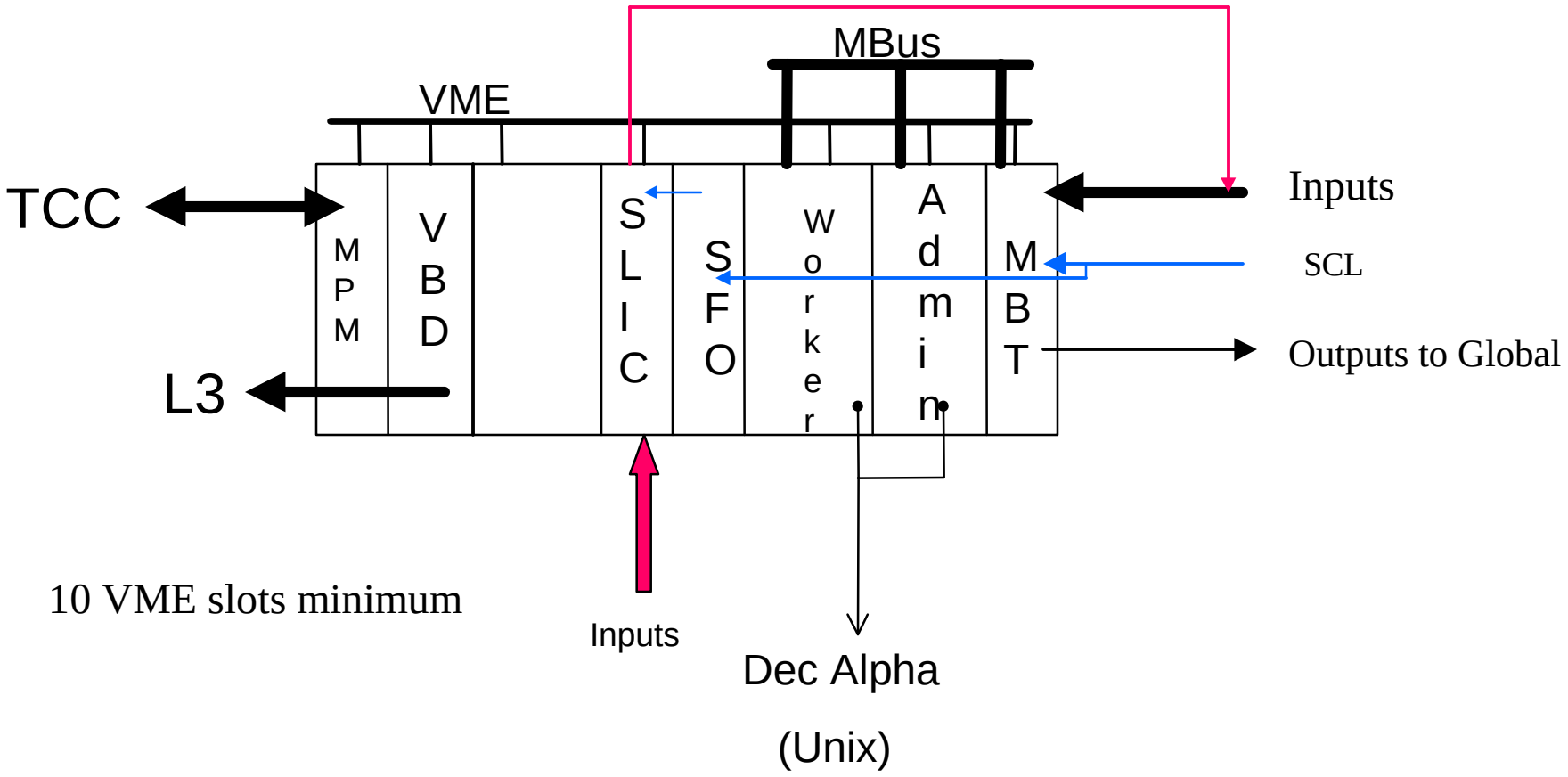
SLIC:
Serial Link Input Card

- 16 Cypress serial inputs
  - 1-slot VME slave card
  - 4 TI DSP's, up to 2 GIPS each
- more inputs, CPU / slot than Alpha
- output via Hotlink to MBT
- Readout via Worker Alpha via MBT
  - Acts as pre-preprocessor
- test registers on all inputs (eg. SCL)

SFO:
SCL Fanout

- Receives L1 SCL information
  - from MBT as Cypress Hotlink
- Fans out as Cypress output to 12 SLIC cards
  - event synchronization
  - L1 Qualifiers
- purely analog fanout

Standard Crate with SLIC



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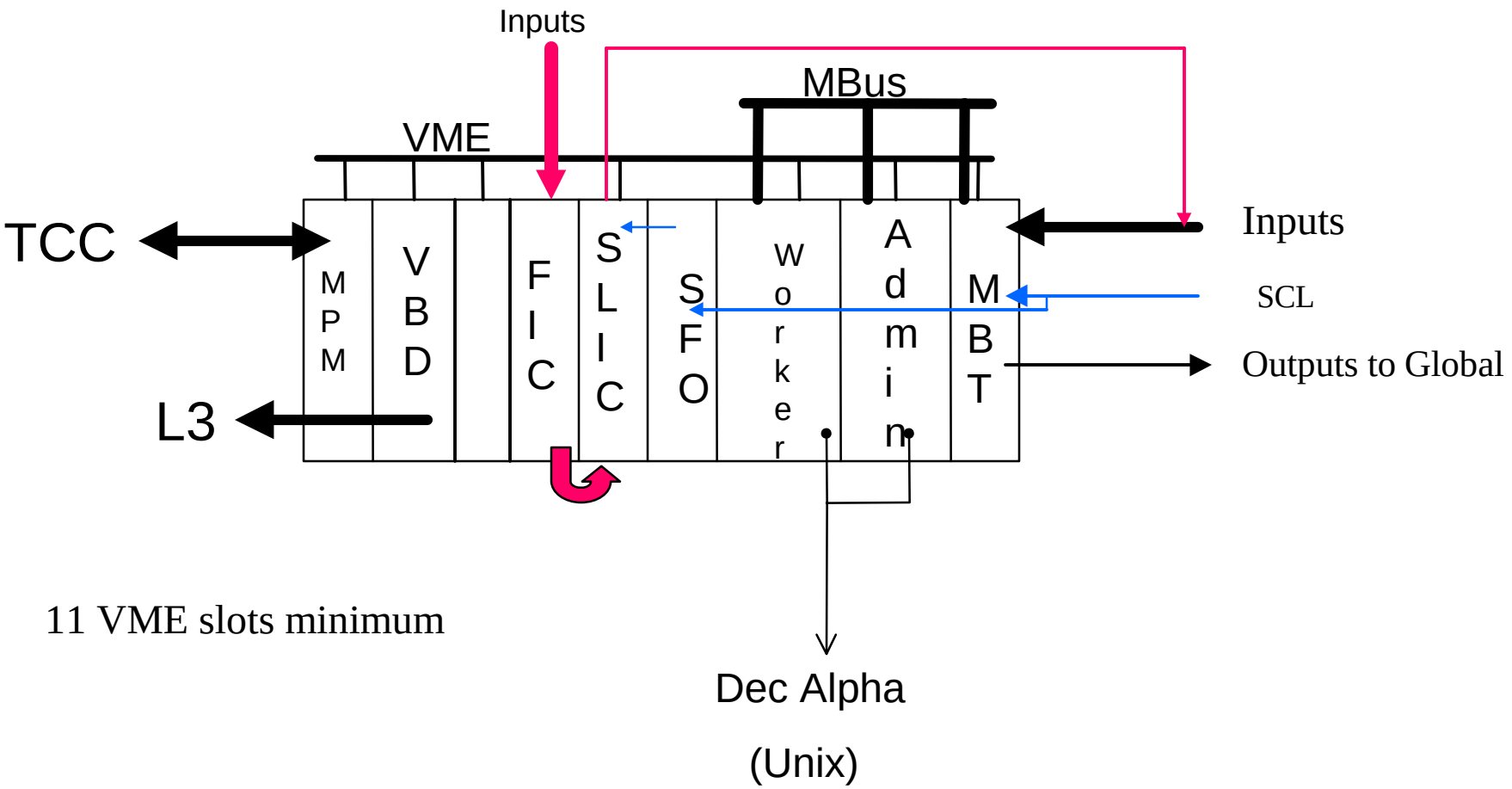
Fiber Input Converter (FIC)

- Convert Fiber Input to Cu Cypress Hotlink
  - G-link input 16b data in 20b data frame (24b total)
    - input thru J3 by standard VTM transition module
  - Cypress 160 out
- Front end to *either* SLIC or MBT
  - avoids variants of complex card
- VME used for control, monitoring
- 4 independent channels per card

Standard Crate with FIC to SLIC



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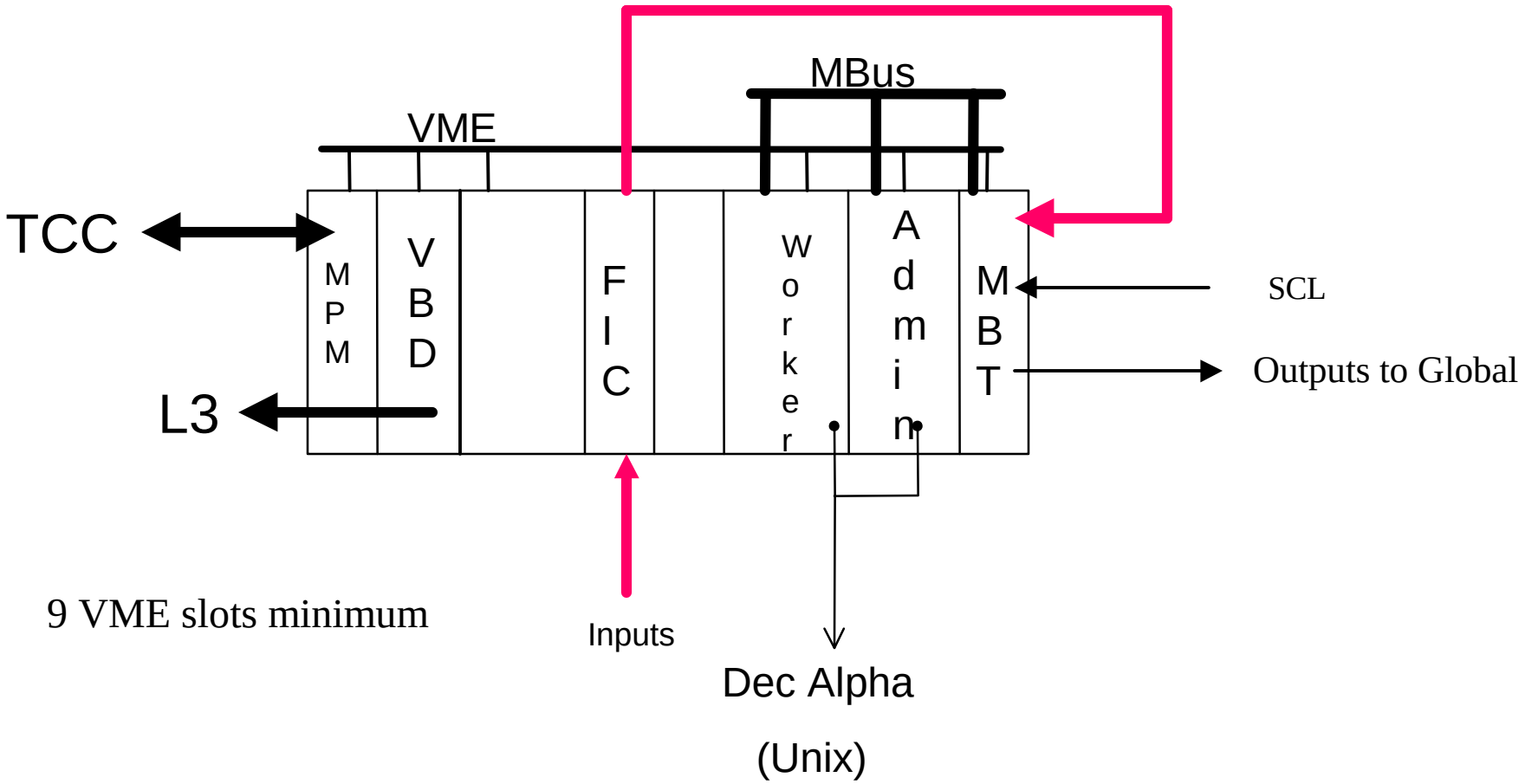
Standard Crate with FIC to MBT



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FIC: L2CFT from L1 CFT trigger (& L1 Cal)

- Presently, plan g-link 1.3Gb/s = 100MB/s
  - L1CFT: 100B (50 tracks)/fiber to STT in 1 μs
    - L1CFT plans to send fixed length, pad w/ trailing zeros
    - add physical trailer with parity and error indication
- 4 g-link inputs per card max
- 8 fibers = 2 cards for L2CFT

FIC: Raw Data Input

- Split of raw data fiber *requires* 1.3 Gb/s g-link
- not needed currently
  - no cable count yet
  - use as part of STT?
    - More likely, recycle part of VRB input

MBT Simplifications: *are* all sources intelligent?

- Enforce padding to 16 B? No?
  - probably can't if accepting raw data
- Enforce maximum event size? Try.
  - Input FIFOs hold 16 worst-case M+P events
    - need definition from EVERY know source
  - Truncate if overflow anyway (no marker added!)
    - In-band marker makes assumptions about data formats!
    - OK *if* processors can recognize w/o extra work
      - OK for L2-formatted inputs (trailers broken)
      - what about raw fiber data?
- SAME issues for SLIC inputs

MBT Testing Questions

- VME OR MBus
  - Control/Setup
  - Fake data for inputs, outputs
  - Loopback test of output(s) to inputs at full speed
    - VME readback of filled FIFO's needed
- MBus only: need MBus, Alphas
  - Broadcast input test
  - Parallel I/O test
  - Mbus Control/Setup
- SCL Test Jig?
  - SCL L1formatting + standard input
  - SCL L2: need Alpha?
  - Check with SCL designers: Walter Knopf in Barsotti group

Development System Questions

- Digital Unix Alpha required for debugging
  - compile, link at any Alpha; serve disk anywhere?
- Most user software needs only simulator with correct data format and buffer structure
  - should build into simulator
- Data movement software from Global & Cal
  - MINOR modifications
    - specific qualifiers needed

Development System, II

- How long do which systems stay at home?
  - Current estimate is 50K for a Standard Crate
  - Attempt communication with Global before commissioning--requires extra development crate
  - Timing may force production of Alpha cards early
    - lose potential for later speedup?

Test Stand at Fermi

- Global, Cal-like, Mu/Track-like, Data Source
- Incomplete system--
  - no HWFW
  - not enough parts for full code of any/all crates
    - except maybe full playback for Global
    - could reconfigure if need be--painful!

L2 Parts Count															
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	PC	Alpha	MBT	SLIC	SCL Fa	Fiber	Bit3 MPM	VBD	Cables	Crate	Mbus	Power	Cooling	Cost	
Unit Cost	3000	10000	5000	10000	5000	10000	5000	0	100	3300	1500	4000	2000		
Count of Standard Parts															
Global	1	2	2	0	0	0	1	1	16	1	1	1	0.5	49400	
Cal	0	3	1	0	0	0	1	1	3	1	1	1	0.5	50100	
Mu/Tracking	0	2	1	2	1	1	1	1	3	1	1	1	0.5	75100	
Data	0	2	2	0	0	0	1	0	10	1	1	1	0.5	45800	
Less Cal Development	-1	-2	-2	0	0	0	-1	0	-3	-1	-1	-1	0	-47100	
Spares	1	1	1	1	2	2	1	1	5	1	1	1	1	74300	
Test System/Spares	1	8	5	3	3	3	4	4	34	4	4	4	3	173300	
System	1	2	2	0	0	0	1	1	16	1	1	1	1	50400	
Development	0	2	1	0	0	0	1	0	5	1	1	1	0	39300	MSU
Global	1	4	3	0	0	0	2	1	21	2	2	2	1	89700	
System	0	4	2	0	0	0	1	1	16	1	1	1	1	67400	
Development	1	2	2	0	0	0	1	0	3	1	1	1	0	47100	UIC to D0
Cal	1	6	4	0	0	0	2	1	19	2	2	2	1	114500	
System	0	2	2	2	1	1	1	1	20	1	1	1	1	82800	
Development	1	2	1	0	0	0	1	0	3	1	1	1	0	42100	UMD
CFT	1	4	3	2	1	1	2	1	23	2	2	2	1	124900	
System	0	4	4	16	2	0	2	2	250	2	2	2	1	284600	
Development	1	0	0	0	0	0	0	0	0	0	0	0	0	3000	NIU to D0
Mu	1	4	4	16	2	0	2	2	250	2	2	2	1	287600	
System	0	4	4	4	2	2	2	2	100	2	2	2	1	169600	
Development	1	0	0	0	0	0	0	0	0	0	0	0	0	3000	SB
Preshower	1	4	4	4	2	2	2	2	100	2	2	2	1	172600	
Totals for Parts	6	30	23	25	8	6	14	11	447	14	14	14	8	962600	
System	0	2	2	0	0	0	1	1	16	1	1	1	1	47400	
Development	1	2	1	0	0	0	1	0	5	1	1	1	0	42300	BU?
STT	1	4	3	0	0	0	2	1	21	2	2	2	1	89700	
Less STT Devel in Test	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Totals Parts (w/ STT)	7	34	26	25	8	6	16	12	468	16	16	16	9	1656700	