XC9500XL CPLD Power Sequencing and Hot Plugging

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Summary

This application note describes how to properly configure XC9500XL CPLDs in 5V/3.3V mixed systems, 3.3V-only systems, and 3.3/2.5V mixed systems.

Introduction

Mixed signal systems—typically 5V/3.3V today—require logic parts that can operate with multiple power supplies. Xilinx XC9500XL CPLDs are designed to operate in either mixed 5V/3.3V systems, 3.3V only systems or 3.3V/2.5V systems. To handle all conditions, care has been taken to assure that designers need not introduce elaborate circuitry to guarantee that any power supplies rise or fall in any particular sequence. This application note describes the underlying XC9500XL circuitry to give designers the understanding they need to best use these powerful CPLDs. Also, the ability to plug unpowered boards into live chassis without disturbing the operation of the target system is discussed with design considerations provided to ensure successful operation.

XC9500XL CPLDs are provided with two separate power supply pins. V_{CCINT} supplies power for the internal logic, memory and charge pumps. V_{CCIO} supplies power for the output drivers. The I/O supply allows the CPLD to be used in either 5V, 3.3V or 2.5V logic level systems by appropriate attachment. This approach raises the issue of biasing internal structures in nonstandard configurations. Experimentation and analysis of the structures has shown that the devices are safe under all anticipated power sequences. Figure 1 details the basic structure. Impedances Z1 and Z2 provide superior ESD protection to the pins. Their behavior is key to understanding the hot plugging and power sequencing behavior.

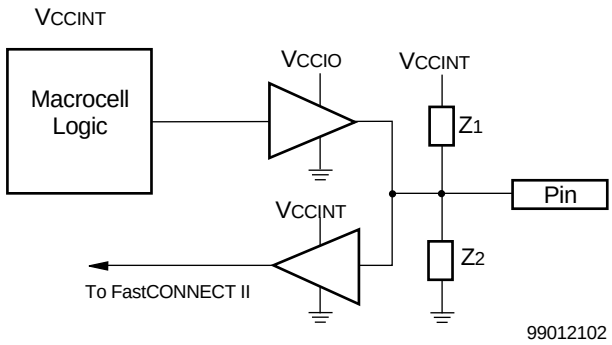

Figure 1: **Simplified XC9500XL I/O Structure**

Discussion

Two common power supply configurations occur. First, the single supply system involves attaching both V_{CCINT} and V_{CCIO} to the same voltage, 3.3V +/- 0.3V. The second configuration is V_{CCINT} is attached to 3.3V and V_{CCIO} is attached to 2.5V. Connecting both supplies to 2.5V is not permitted as well as connecting V_{CCINT} to 3.3V and V_{CCIO} to 5V. We will not consider these two cases. Under these restrictions, it is unlikely that V_{CCIO} and V_{CCINT} will be split up if a 3.3V only system is used, but the following analysis also covers this case. Of specific interest

is the case of having V_{CCIO} = 2.5V and V_{CCINT} = 3.3V which in turn, produces two cases of interest.

Specific concern arises if one of the power supplies is off while the other is on. There are two ways this could happen. Figure 2 shows the situation where V_{CCINT} is turned on and V_{CCIO} is turned off. Figure 3 shows the case where V_{CCINT} is turned off and V_{CCIO} is turned on.

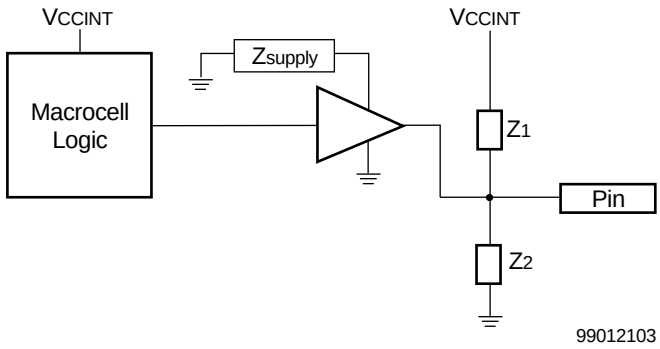

Figure 2: **XC9500XL Output Driver with V_{CCIO} Turned Off (Input Receiver not Shown)**

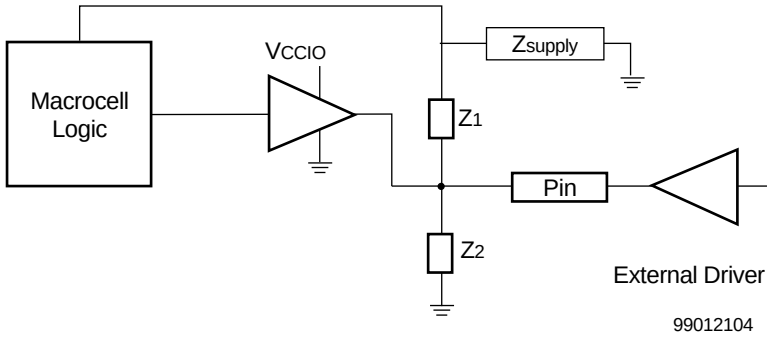

Figure 3: **XC9500XL Output Driver with V_{CCIO} Turned On (Input Receiver not Shown)**

At least two factors come into play:

- the supply impedance (Zsupply)
- the state of the macrocell logic driving into the output driver.

Let's see how these affect the condition of the CPLD when power sequencing occurs.

Supply Impedance

The supply impedance is important because current may flow from the CPLD into the turned off power supply, if a path and an available source (ie, the other supply) exists. This can occur if an external CMOS chip is driving into the CPLD pin (see Figure 3).

Most power supplies are either linear (series pass) or switching. In either case, the supply output typically has some silicon impedance and a fairly large capacitor to ground. The supply output capacitor can accept substantial current, but as current arrives, the accumulated charge increases the capacitor voltage. If the turned off supply is initially uncharged, there might be a substantial initial current. As we will see in the Hot Plugging section, this current will be tiny.

Note that for this discussion, we are assuming the power supplies remain attached to the chip pins electrically, whether they are powered up or not. Adding a series switch will physically break the connection, changing the assumptions.

Macrocell State

Figure 4 shows a simplified model of the output driving structure for an XC9500XL CPLD. If point A is low and V_{CCIO} is on, the pin drives high. If point A is high and V_{CCIO} is on, the pin drives low. If point A switches slowly, the pin inverts, but I_{CC} through the attached input receiver (not shown) can be substantial, if V_{CCINT} is powered up.

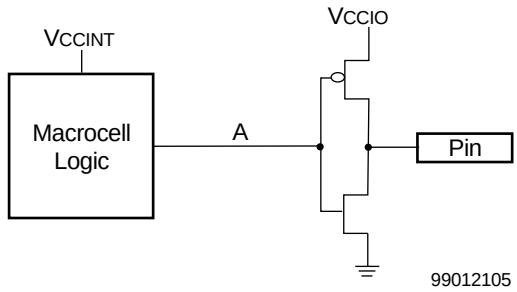

Figure 4: **Close-Up View of Simplified Output Stage (ESD Circuits Not Shown)**

Figure 4 suggests that the condition of an output driver is affected by the voltage driven onto its gate(s) by the macrocell. If V_{CCIO} is powered up first, a possible issue may arise, particularly with hot plugging (see **Hot Plugging**, page 3). Figure 5 shows the voltage rising in a macrocell output. It tracks V_{CCINT} until the configuration trip point occurs, which clears the macrocell flop and reloads the macrocell. This results in a low voltage notch right before the final configuration occurs. This notch may briefly introduce a not-tristate (i.e. active) driver at the pin. **To avoid this behavior, it is best if V_{CCINT} rises before VCCIO.**

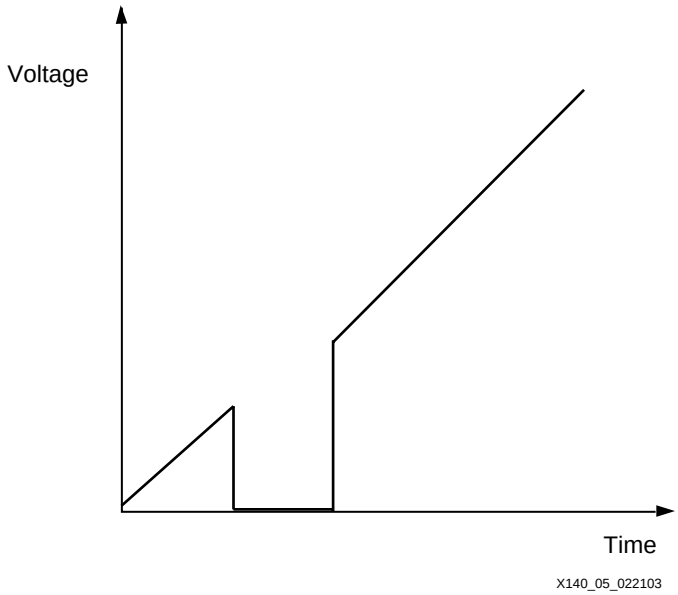

Figure 5: **Macrocell Voltage versus Time During Power Up**

Hot Plugging

Hot plugging (aka Live Insertion or sometimes "hot socketing") is the ability for logic parts to be inserted into a powered up digital system and have no adverse effects. Hot plugging is crucial for industries that require changes to digital systems but cannot tolerate power down to do so. Typically, these systems are found in telephone exchanges, electric utilities and air traffic control systems. Various suppliers meet this need, but each defines it somewhat different and may introduce caveats that are not workable for all systems. Due to the power supply tolerance of Xilinx CPLDs and additional circuit capabilities, XC9500XL parts have very favorable Hot

Plugging behavior. Fundamentally, this stems from the automatic power up feature whereby the outputs are tri-stated.

Let's consider the Hot Plugging process by looking at the number of combinations of things that can occur. Remember that XC9500XL CPLDs have two power supplies, ground and an I/O pin as a basic model. When Hot Plugging, literally any combination of pin voltage arrivals to their target condition can occur. As noted earlier, the power sequencing for XC9500XL CPLDs does not matter, so this is of little concern.

From a chip point of view, two critical features are important: the chip being attached should go into high impedance while connection is being made and its ESD circuitry should not present an invasive load to the target system during the initial settling down. We have already discussed the power-up operation of XC9500XL parts earlier. The critical consideration is that less than 25 µA of current can flow into or out of the pin to or from the power supply. In most systems, this tiny fraction of current is not sufficient to upset external bus voltages.

If it is known early that Hot Plugging will occur, planning can make it even safer. For instance, it is possible to design PCBs that physically present the power connections to the target prior to insertion of the logic points. This assures power is on the chips prior to the attachment of signals. It would be possible for a signal to be powered up, and in its natural state, drive low when attached to the system which drives the corresponding point low. This can be handled by designing the board to include logic managing the pins so that pins are tri-stated until the system dictates they be enabled. Reference 1 outlines a procedure for precharging the decoupling capacitors and all attachment metal to a half charged condition to assure that absolute minimal electrical perturbation occurs. Xilinx XC9500XL CPLDs deliver their part by being tristated and minimizing any current passed through the ESD circuits. Careful PCB planning can handle the rest.

Conclusion

XC9500XL CPLDs are designed to operate in single 3.3V , mixed 3.3V/5V systems and 3.3V/2.5V systems and tolerate any power supply sequencing applied to them without damaging the CPLD, the supply or the external circuits assuming correct logic design has occurred. Mixed voltage design has never been easier.

References

1. **XC9500XL Family Datasheet** (DS054)
2. "Live Insertion", SDYA012, Texas Instruments, Eilhard Hasselhoff, October 1996

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/28/03	1.0	Initial Xilinx release.