

Fermi National Accelerator Laboratory

**D-Zero Detector Calorimeter Electronics
Run II b Upgrade Project**

**Test Waveform Generator System
System Specification**

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1 Introduction

This document specifies the Test Waveform Generator System (TWG). The TWG is part of the electronics of the D-Zero detector Calorimeter Trigger Test System at Fermilab. More information on the experiments performed at Fermilab is available on the laboratory web page:

<http://www.fnal.gov/>

More information on the D0 Detector is available on:

<http://www-d0.fnal.gov/>

The designers welcome suggestions and corrections [Ref. 13], which can be addressed directly to the engineer responsible of the project. Contact information is available on the Electronics System Engineering (ESE) web page:

<http://www-ese.fnal.gov/>

More information and documentation on the Test Waveform Generator Project are available on:

http://www-ese.fnal.gov/D0Cal_TWG/

2 Overview

The Test Waveform Generator (TWG) is a system used for testing some components of the D0 Calorimeter Level 1 Trigger electronics [Paragraph 7]. The TWG has been assembled using a commercial one-channel “arbitrary waveform generator”, a commercial multiplexer system and a custom VME 64x [5] transition module.

2.1 System Under Test - The D0 calorimeter Level 1 Trigger System

The main purpose of the TWG is to test the ADF cards/system [Paragraph 7]. Figure 2.1 briefly describes the ADF system and its interfaces. The TWG will not be a part of the D0 Trigger system but will be used only to verify performance and functionality of the ADF cards in a separate test environment. Besides emulating the signals produced by the Baseline Subtractor System (BLS) the TWG is able to generate arbitrary waveforms that can be used to measure the characteristics of the ADF's analog input stage.

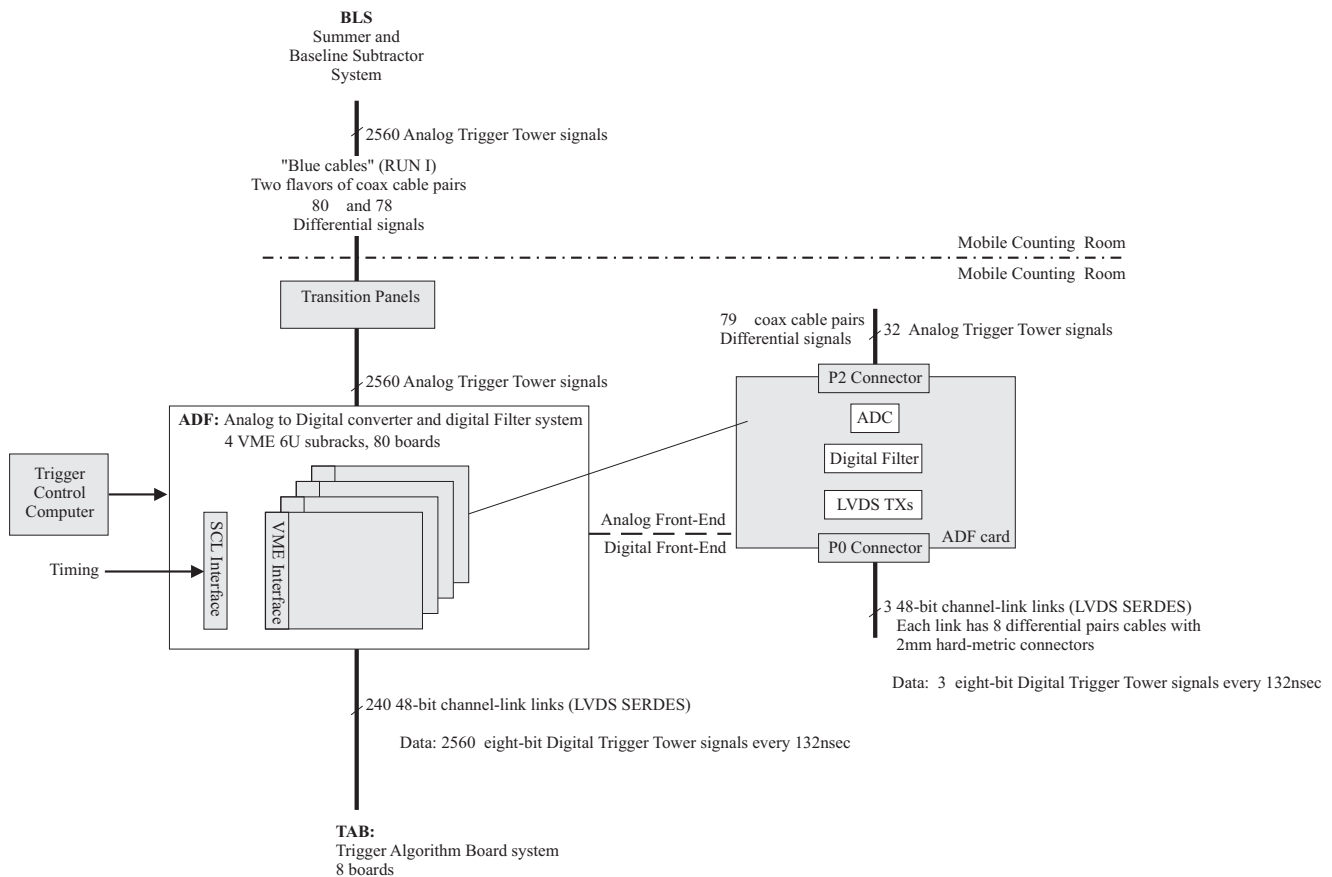


Figure 2.1, Block diagram of the ADF section on the L1 trigger system

The TWG system is used to test only one ADF card at a time. The TWG can be controlled from a PC using RS-232 [Ref. RS-232] and/or IEEE-488 (GPIB, HPIB) [Ref.GPIB].

3 Test Waveform Generator system

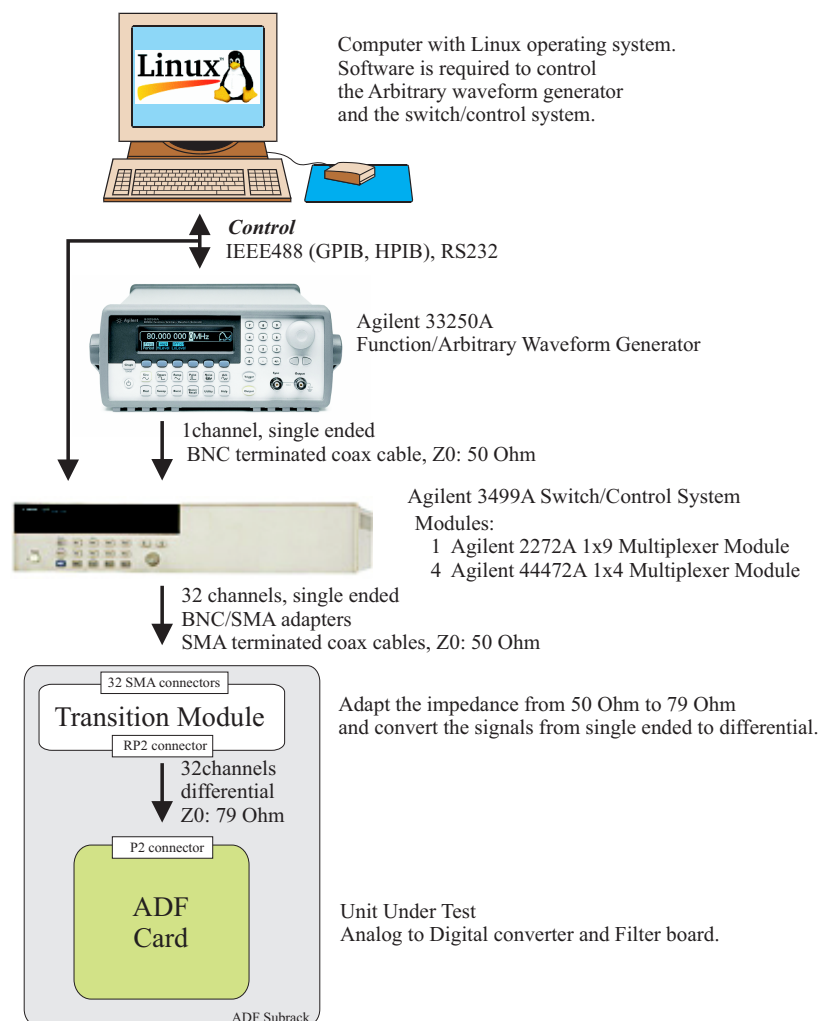


Figure 3.1, Test Waveform Generator system.

3.1 Computer

3.1.1 Minimum Requirements

Interface ports to control the TWG system: GPIB I/O or RS-232 (2 ports).

3.2 Arbitrary Waveform Generator

One Arbitrary Waveform Source: **Agilent 33250A**



Figure 3.2, Agilent 33250A Function/Arbitrary Waveform Generator

The Agilent 33250A Function/Arbitrary Waveform generator uses direct digital synthesis to create output waveform down to 1 μ Hz frequency resolution.

Waveforms

80MHz sine and square wave outputs

50MHz pulse waveform with variable rise/fall times

12-bit, 200Msa.s, 64K-point deep arbitrary waveform.

Output characteristics

Signal source impedance: 50 Ω

Amplitude (into 50 Ω): 10 mV_{pp} to 10 V_{pp}

Interfaces

IEEE-488 (GPIB, HPIB)

RS232

Power Supply

100-240 VAC, 50-60Hz

100-127 VAC, 50-400Hz

Power consumption: 140 VA

3.3 Switch System

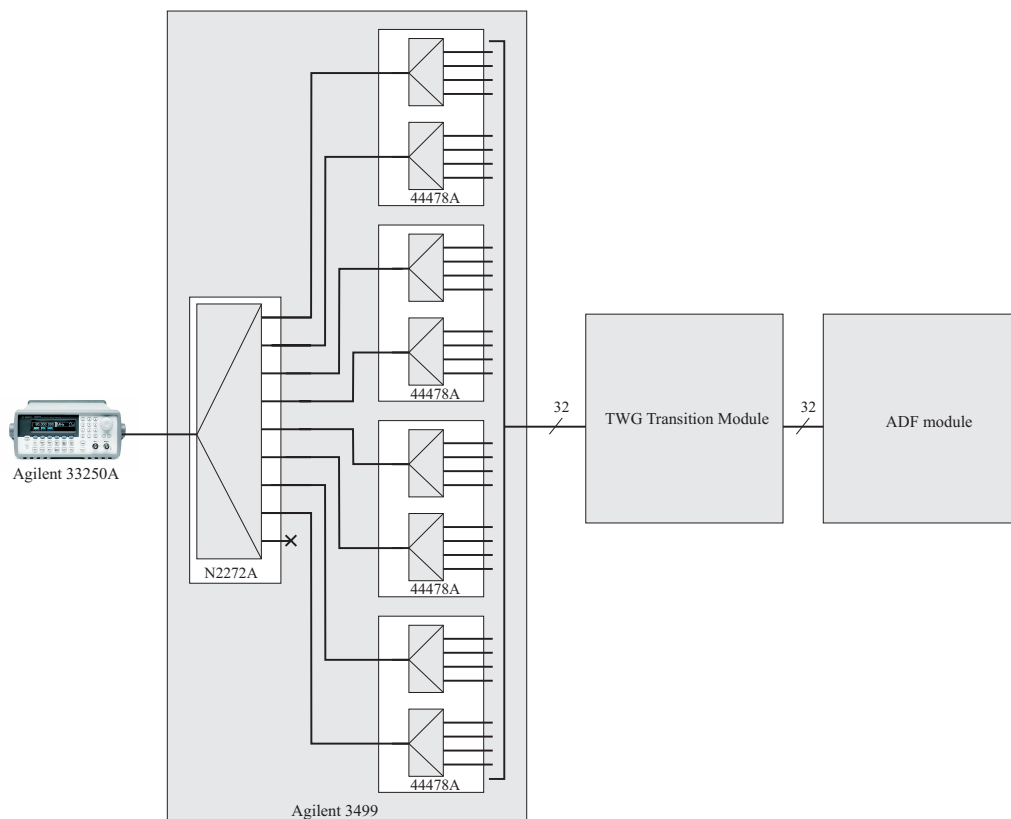


Figure 3.3, Switch system diagram

3.3.1 Mainframe

Agilent 3499A Switch/Control System, 5 slot mainframe



Figure 3.4, Agilent 3499A Switch/Control System

Interfaces

IEEE-488 (GPIB, HPIB)

RS232

Power Supply

100-240 VAC, 50-60Hz

100-127 VAC, 50-400Hz

Power consumption: 40 VA maximum

3.3.2 1x9 Multiplexer module

Agilent N2272A, 1 GHz 1x9 RF Multiplexer Module

Insertion loss (100MHz): <0.5 dB

Cross talk (100MHz): <-75dB

SWR (100MHz): <1.20

Bandwidth: 1.0 GHz

Characteristic impedance: 50 Ω

Signal delay: 2.5 nsec

Initial channel closed resistance: 0.8 Ω

Connector: BNC

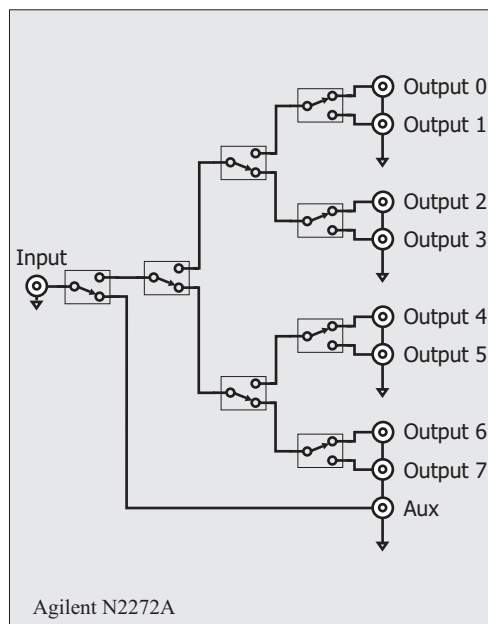


Figure 3.5, N2272A multiplexing diagram

3.3.3 1x4 Multiplexer module

Agilent 44478A, Dual 1x4 RF Multiplexer(1.3GHz, 50 Ω)

Insertion loss (100MHz): <0.7 dB

Cross talk (100MHz):<-80dB

SWR (100MHz): <1.25

Bandwidth: 1.3 GHz

Characteristic impedance: 50 Ω

Signal delay: 3 nsec

Initial channel closed resistance: 1 Ω

Connector: BNC

Off-channels termination: Yes



Figure 3.6, Agilent 44478A Dual 1x4 VHF Multiplexer

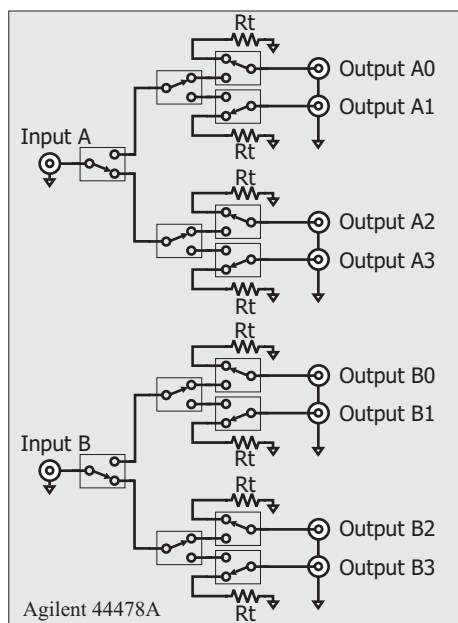


Figure 3.7, 44478A multiplexing diagram

3.4 Custom VME 64x Transition Module

A detailed description of the transition module is given in paragraph 4.

4 Custom VME 64x Transition Module

A custom module has been designed to interface the waveform generation and switching components of the TWG system with the ADF system.

4.1 Specifications

The module complies with the VME64x [Ref.VME64x] transition module specifications.

It has 32 inputs, one for each of the ADF analog input channels.

The module convert single ended signals to differential using transformers; the output impedance is then matched to the input stage of the ADF

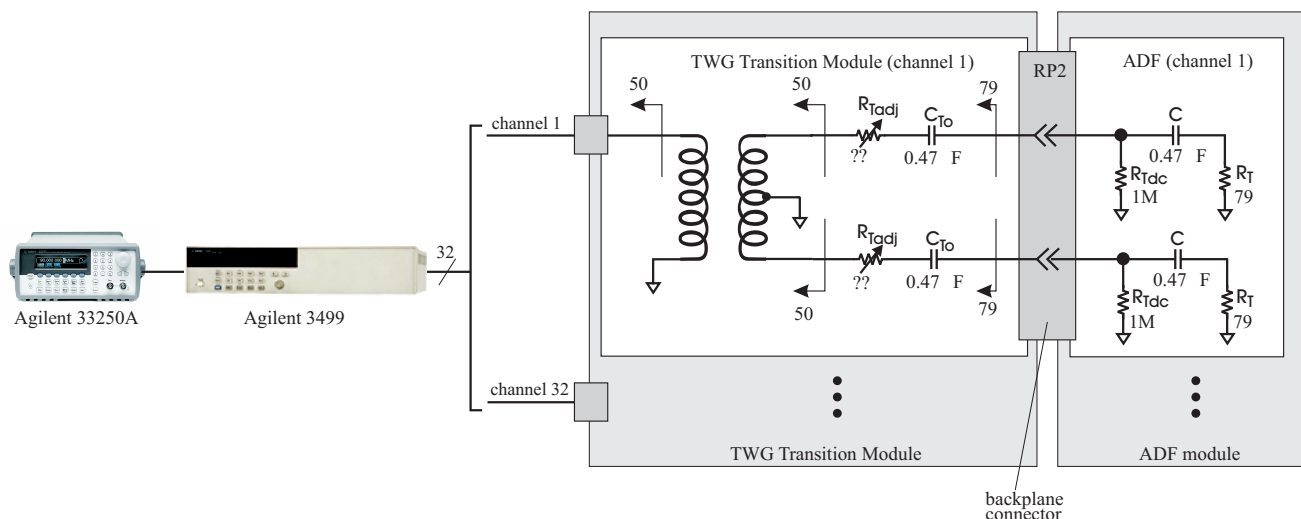


Figure 4.1, ADF Interfacing diagram

4.2 Interfaces

[To be specified]

4.3 Monitoring and diagnostic features

[To be specified]

4.3.1 Power supply

[To be specified]

4.4 Appendix D - TWG Transition Module Components and Layout

[To be specified]

5 Appendix A - VME64x Backplane - connectors pinout

Pin#	Row Z	Row A	Row B	Row C	Row D
1	MPR (Bus Pause Request)	D00 (Data Bus)	BBSY* (Bus Busy)	D08 (Data Bus)	VPC (Voltage Pre-Charge)
2	GND (Ground)	D01 (Data Bus)	BCLR* (Bus Clear)	D09 (Data Bus)	GND (Ground)
3	MCLK (Module Clock)	D02 (Data Bus)	ACFAIL* (AC Power Fail)	D10 (Data Bus)	+V1 (auxiliary power)
4	GND (Ground)	D03 (Data Bus)	BG0IN* (Bus Grant daisy-chain)	D11 (Data Bus)	+V2 (auxiliary power)
5	MSD (Slave Data)	D04 (Data Bus)	BG0OUT* (Bus Grant daisy-chain)	D12 (Data Bus)	ResvU (reserved Unbussed)
6	GND (Ground)	D05 (Data Bus)	BG1IN* (Bus Grant daisy-chain)	D13 (Data Bus)	-V1 (auxiliary power)
7	MMD (Module Data)	D06 (Data Bus)	BG1OUT* (Bus Grant daisy-chain)	D14 (Data Bus)	-V2 (auxiliary power)
8	GND (Ground)	D07 (Data Bus)	BG2IN* (Bus Grant daisy-chain)	D15 (Data Bus)	ResvU (reserved Unbussed)
9	MCTL (Module Control)	GND (Ground)	BG2OUT* (Bus Grant daisy-chain)	GND (Ground)	GAP* (Geographical Address Parity)
10	GND (Ground)	SYSCLK	BG3IN* (Bus Grant daisy-chain)	SYSFAIL* (System Fail)	GA0* (Geographical Address)
11	RESP* (Response)	GND (Ground)	BG3OUT* (Bus Grant daisy-chain)	BERR* (Bus Error)	GA1* (Geographical Address)
12	GND (Ground)	DS1* (Data Strobe)	BR0* (Bus Request)	SYSRESET* (System Reset)	Power:+3.3V
13	ResBus (Reserved Bussed)	DS0* (Data Strobe)	BR1* (Bus Request)	LWORD* (Long Word)	GA2* (Geographical Address)
14	GND (Ground)	WRITE* (Read/Write)	BR2* (Bus Request)	AM5 (Address Modifier)	Power:+3.3V
15	ResBus (Reserved Bussed)	GND (Ground)	BR3* (Bus Request)	A23 (Address Bus)	GA3* (Geographical Address)
16	GND (Ground)	DTACK* (Data Transfer Acknowledge)	AM0 (Address Modifier)	A22 (Address Bus)	Power:+3.3V
17	ResBus (Reserved Bussed)	GND (Ground)	AM1 (Address Modifier)	A21 (Address Bus)	GA4* (Geographical Address)
18	GND (Ground)	AS* (Address Strobe)	AM2 (Address Modifier)	A20 (Address Bus)	Power:+3.3V
19	ResBus (Reserved Bussed)	GND (Ground)	AM3 (Address Modifier)	A19 (Address Bus)	ResBus (Reserved Bussed)
20	GND (Ground)	IACK* (Interrupt Acknowledge)	GND (Ground)	A18 (Address Bus)	Power:+3.3V
21	ResBus (Reserved Bussed)	IACKIN* (Interrupt Acknowledge daisy-chain)	SERA (Serial Bus)	A17 (Address Bus)	ResBus (Reserved Bussed)
22	GND (Ground)	IACKOUT* (Interrupt Acknowledge daisy-chain)	SERB (Serial Bus)	A16 (Address Bus)	Power:+3.3V
23	ResBus (Reserved Bussed)	AM4 (Address Modifier)	GND (Ground)	A15 (Address Bus)	ResBus (Reserved Bussed)
24	GND (Ground)	A07 (Address Bus)	IRQ7* (priority Interrupt request)	A14 (Address Bus)	Power:+3.3V
25	ResBus (Reserved Bussed)	A06 (Address Bus)	IRQ6* (priority Interrupt request)	A13 (Address Bus)	ResBus (Reserved Bussed)
26	GND (Ground)	A05 (Address Bus)	IRQ5* (priority Interrupt request)	A12 (Address Bus)	Power:+3.3V
27	ResBus (Reserved Bussed)	A04 (Address Bus)	IRQ4* (priority Interrupt request)	A11 (Address Bus)	LI/I*
28	GND (Ground)	A03 (Address Bus)	IRQ3* (priority Interrupt request)	A10 (Address Bus)	Power:+3.3V
29	ResBus (Reserved Bussed)	A02 (Address Bus)	IRQ2* (priority Interrupt request)	A09 (Address Bus)	LI/O*
30	GND (Ground)	A01 (Address Bus)	IRQ1* (priority Interrupt request)	A08 (Address Bus)	Power:+3.3V
31	ResBus (Reserved Bussed)	Power: -12V	Power: +5VSTDBY	Power: +12V	GND (Ground)
32	GND (Ground)	Power: +5V	Power: +5V	Power: +5V	VPC (Voltage Pre-Charge)

Table 5.1. VME64x J1 Pin Assignments

Pin#	Row Z	Row A	Row B	Row C	Row D
1	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
2	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
3	UD (User Defined)	UD (User Defined)	RETRY*	UD (User Defined)	UD (User Defined)
4	GND (Ground)	UD (User Defined)	A24 (Address Bus)	UD (User Defined)	UD (User Defined)
5	UD (User Defined)	UD (User Defined)	A25 (Address Bus)	UD (User Defined)	UD (User Defined)
6	GND (Ground)	UD (User Defined)	A26 (Address Bus)	UD (User Defined)	UD (User Defined)
7	UD (User Defined)	UD (User Defined)	A27 (Address Bus)	UD (User Defined)	UD (User Defined)
8	GND (Ground)	UD (User Defined)	A28 (Address Bus)	UD (User Defined)	UD (User Defined)
9	UD (User Defined)	UD (User Defined)	A29 (Address Bus)	UD (User Defined)	UD (User Defined)
10	GND (Ground)	UD (User Defined)	A30 (Address Bus)	UD (User Defined)	UD (User Defined)
11	UD (User Defined)	UD (User Defined)	A31 (Address Bus)	UD (User Defined)	UD (User Defined)
12	GND (Ground)	UD (User Defined)	Ground	UD (User Defined)	UD (User Defined)
13	UD (User Defined)	UD (User Defined)	Power: +5V	UD (User Defined)	UD (User Defined)
14	GND (Ground)	UD (User Defined)	D16 (Data Bus)	UD (User Defined)	UD (User Defined)
15	UD (User Defined)	UD (User Defined)	D17 (Data Bus)	UD (User Defined)	UD (User Defined)
16	GND (Ground)	UD (User Defined)	D18 (Data Bus)	UD (User Defined)	UD (User Defined)
17	UD (User Defined)	UD (User Defined)	D19 (Data Bus)	UD (User Defined)	UD (User Defined)
18	GND (Ground)	UD (User Defined)	D20 (Data Bus)	UD (User Defined)	UD (User Defined)
19	UD (User Defined)	UD (User Defined)	D21 (Data Bus)	UD (User Defined)	UD (User Defined)
20	GND (Ground)	UD (User Defined)	D22 (Data Bus)	UD (User Defined)	UD (User Defined)
21	UD (User Defined)	UD (User Defined)	D23 (Data Bus)	UD (User Defined)	UD (User Defined)
22	GND (Ground)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)
23	UD (User Defined)	UD (User Defined)	D24 (Data Bus)	UD (User Defined)	UD (User Defined)
24	GND (Ground)	UD (User Defined)	D25 (Data Bus)	UD (User Defined)	UD (User Defined)
25	UD (User Defined)	UD (User Defined)	D26 (Data Bus)	UD (User Defined)	UD (User Defined)
26	GND (Ground)	UD (User Defined)	D27 (Data Bus)	UD (User Defined)	UD (User Defined)
27	UD (User Defined)	UD (User Defined)	D28 (Data Bus)	UD (User Defined)	UD (User Defined)
28	GND (Ground)	UD (User Defined)	D29 (Data Bus)	UD (User Defined)	UD (User Defined)
29	UD (User Defined)	UD (User Defined)	D30 (Data Bus)	UD (User Defined)	UD (User Defined)
30	GND (Ground)	UD (User Defined)	D31 (Data Bus)	UD (User Defined)	UD (User Defined)
31	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	GND (Ground)
32	GND (Ground)	UD (User Defined)	Power: +5V	UD (User Defined)	VPC

Table 5.2. VME64x J2 Pin Assignments

Pin#	Row E	Row E	Row D	Row C	Row B	Row A	Row Z
1	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
2	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
3	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
4	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
5	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
6	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
7	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
8	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
9	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
10	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
11	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
12	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
13	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
14	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
15	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
16	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
17	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
18	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)
19	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)	UD (User Defined)	UD (User Defined)	GND (Ground)

Table 5.3. VME64x P0 Pin Assignments

6 Appendix B - ADF System - backplane connectors pinout

Pin#	Row Z	Row A	Row B	Row C	Row D
1	N.C.	VME_DATA(0)	N.C.	VME_DATA(8)	N.C.
2	GROUND	VME_DATA(1)	N.C.	VME_DATA(9)	GROUND
3	N.C.	VME_DATA(2)	N.C.	VME_DATA(10)	N.C.
4	GROUND	VME_DATA(3)	BUS_GRANT_0	VME_DATA(11)	N.C.
5	N.C.	VME_DATA(4)	BUS_GRANT_0	VME_DATA(12)	N.C.
6	GROUND	VME_DATA(5)	VME_BUS_GRANT_1_IN_B	VME_DATA(13)	N.C.
7	N.C.	VME_DATA(6)	VME_BUS_GRANT_1_OUT_B	VME_DATA(14)	N.C.
8	GROUND	VME_DATA(7)	BUS_GRANT_2	VME_DATA(15)	N.C.
9	N.C.	GROUND	BUS_GRANT_2	GROUND	N.C.
10	GROUND	N.C.	BUS_GRANT_3	N.C.	VME_GEO_B(0)
11	N.C.	GROUND	BUS_GRANT_3	N.C.	VME_GEO_B(1)
12	GROUND	VME_DS1_B	N.C.	VME_SYSRESET_B	VME_3V3
13	BKPLN_BEGIN_TURN_B	VME_DS0_B	N.C.	VME_LWORD_B	VME_GEO_B(2)
14	GROUND	VME_WRITE_B	N.C.	VME_AM5	VME_3V3
15	BKPLN_LIVE_BX_B	GROUND	N.C.	VME_ADDR(23)	VME_GEO_B(3)
16	GROUND	VME_DTACK_B	VME_AM0	VME_ADDR(22)	VME_3V3
17	BKPLN_SAVE_MONIT_D ATA_B	GROUND	VME_AM1	VME_ADDR(21)	VME_GEO_B(4)
18	GROUND	VME_AS_B	VME_AM2	VME_ADDR(20)	VME_3V3
19	BKPLN_SCL_INIT_B	GROUND	VME_AM3	VME_ADDR(19)	CRATE_STATUS_B(0)
20	GROUND	VME_IACK_B	GROUND	VME_ADDR(18)	VME_3V3
21	BKPLN_BX_CLOCK	VME_IACKIN_B	N.C.	VME_ADDR(17)	CRATE_STATUS_B(1)
22	GROUND	VME_IACKOUT_B	N.C.	VME_ADDR(16)	VME_3V3
23	BKPLN_BX_CLOCK_B	VME_AM4	GROUND	VME_ADDR(15)	CRATE_STATUS_B(2)
24	GROUND	VME_ADD(7)	N.C.	VME_ADDR(14)	VME_3V3
25	BKPLN_SCLD_SPARE_B	VME_ADD(6)	N.C.	VME_ADDR(13)	CRATE_STATUS_B(3)
26	GROUND	VME_ADD(5)	N.C.	VME_ADDR(12)	VME_3V3
27	VME_RSVBUS(7)	VME_ADD(4)	N.C.	VME_ADDR(11)	N.C.
28	GROUND	VME_ADD(3)	N.C.	VME_ADDR(10)	VME_3V3
29	VME_RSVBUS(8)	VME_ADD(2)	VME_IRQ_B(2)	VME_ADDR(9)	N.C.
30	GROUND	VME_ADD(1)	N.C.	VME_ADDR(8)	VME_3V3
31	VME_RSVBUS(9)	VME_N12V	N.C.	VME_P12V	GROUND
32	GROUND	VME_5V	VME_5V	VME_5V	N.C.

Table 6.1. P1 Pin Assignments

Pin#	Row Z	Row A	Row B	Row C	Row D
1	N.C.	Ch_00_HD_P	VME_5V	Ch_00_EM_P	N.C.
2	GROUND	Ch_00_HD_N	GROUND	Ch_00_EM_N	N.C.
3	N.C.	Ch_04_HD_P	N.C.	Ch_04_EM_P	N.C.
4	GROUND	Ch_04_HD_N	N.C.	Ch_04_EM_N	N.C.
5	N.C.	Ch_08_HD_P	N.C.	Ch_08_EM_P	N.C.
6	GROUND	Ch_08_HD_N	N.C.	Ch_08_EM_N	N.C.
7	N.C.	Ch_12_HD_P	N.C.	Ch_12_EM_P	N.C.
8	GROUND	Ch_12_HD_N	N.C.	Ch_12_EM_N	N.C.
9	N.C.	Ch_01_HD_P	N.C.	Ch_01_EM_P	N.C.
10	GROUND	Ch_01_HD_N	N.C.	Ch_01_EM_N	N.C.
11	N.C.	Ch_05_HD_P	N.C.	Ch_05_EM_P	N.C.
12	GROUND	Ch_05_HD_N	GROUND	Ch_05_EM_N	N.C.
13	N.C.	Ch_09_HD_P	VME_5V	Ch_09_EM_P	N.C.
14	GROUND	Ch_09_HD_N	N.C.	Ch_09_EM_N	N.C.
15	N.C.	Ch_13_HD_P	N.C.	Ch_13_EM_P	N.C.
16	GROUND	Ch_13_HD_N	N.C.	Ch_13_EM_N	N.C.
17	N.C.	Ch_02_HD_P	N.C.	Ch_02_EM_P	N.C.
18	GROUND	Ch_02_HD_N	N.C.	Ch_02_EM_N	N.C.
19	N.C.	Ch_06_HD_P	N.C.	Ch_06_EM_P	N.C.
20	GROUND	Ch_06_HD_N	N.C.	Ch_06_EM_N	N.C.
21	N.C.	Ch_10_HD_P	N.C.	Ch_10_EM_P	N.C.
22	GROUND	Ch_10_HD_N	GROUND	Ch_10_EM_N	N.C.
23	N.C.	Ch_14_HD_P	N.C.	Ch_14_EM_P	N.C.
24	GROUND	Ch_14_HD_N	N.C.	Ch_14_EM_N	N.C.
25	N.C.	Ch_03_HD_P	N.C.	Ch_03_EM_P	N.C.
26	GROUND	Ch_03_HD_N	N.C.	Ch_03_EM_N	N.C.
27	N.C.	Ch_07_HD_P	N.C.	Ch_07_EM_P	N.C.
28	GROUND	Ch_07_HD_N	N.C.	Ch_07_EM_N	N.C.
29	N.C.	Ch_11_HD_P	N.C.	Ch_11_EM_P	N.C.
30	GROUND	Ch_11_HD_N	N.C.	Ch_11_EM_N	N.C.
31	N.C.	Ch_15_HD_P	GROUND	Ch_15_EM_P	GROUND
32	GROUND	Ch_15_HD_N	VME_5V	Ch_15_EM_N	N.C.

Table 6.2. P2 Pin Assignments

Pin#	Row E	Row E	Row D	Row C	Row B	Row A	Row Z
1	GROUND	LX0_T1_N (Link 0 Serial Data 1)	LX0_T1_P (Link 0 Serial Data 1)	GROUND	LX0_T0_N (Link 0 Serial Data 0)	LX0_T0_P (Link 0 Serial Data 0)	GROUND
2	GROUND	LX0_TC_N (Link 0 Serial Data Clock)	LX0_TC_P (Link 0 Serial Data Clock)	GROUND	LX0_T2_N (Link 0 Serial Data 2)	LX0_T2_P (Link 0 Serial Data 2)	GROUND
3	GROUND	LX0_T4_N (Link 0 Serial Data 4)	LX0_T4_P (Link 0 Serial Data 4)	GROUND	LX0_T3_N (Link 0 Serial Data 3)	LX0_T3_P (Link 0 Serial Data 3)	GROUND
4	GROUND	LX0_T6_N (Link 0 Serial Data 6)	LX0_T6_P (Link 0 Serial Data 6)	GROUND	LX0_T5_N (Link 0 Serial Data 5)	LX0_T5_P (Link 0 Serial Data 5)	GROUND
5	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
6	GROUND	LX1_T1_N (Link 0 Serial Data 1)	LX1_T1_P (Link 0 Serial Data 1)	GROUND	LX1_T0_N (Link 1 Serial Data 0)	LX1_T0_P (Link 1 Serial Data 0)	GROUND
7	GROUND	LX1_TC_N (Link 0 Serial Data Clock)	LX1_TC_P (Link 0 Serial Data Clock)	GROUND	LX1_T2_N (Link 1 Serial Data 2)	LX1_T2_P (Link 1 Serial Data 2)	GROUND
8	GROUND	LX1_T4_N (Link 0 Serial Data 4)	LX1_T4_P (Link 0 Serial Data 4)	GROUND	LX1_T3_N (Link 1 Serial Data 3)	LX1_T3_P (Link 1 Serial Data 3)	GROUND
9	GROUND	LX1_T6_N (Link 0 Serial Data 6)	LX1_T6_P (Link 0 Serial Data 6)	GROUND	LX1_T5_N (Link 1 Serial Data 5)	LX1_T5_P (Link 1 Serial Data 5)	GROUND
10	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
11	GROUND	LX2_T1_N (Link 0 Serial Data 1)	LX2_T1_P (Link 0 Serial Data 1)	GROUND	LX2_T0_N (Link 2 Serial Data 0)	LX2_T0_P (Link 2 Serial Data 0)	GROUND
12	GROUND	LX2_TC_N (Link 0 Serial Data Clock)	LX2_TC_P (Link 0 Serial Data Clock)	GROUND	LX2_T2_N (Link 2 Serial Data 2)	LX2_T2_P (Link 2 Serial Data 2)	GROUND
13	GROUND	LX2_T4_N (Link 0 Serial Data 4)	LX2_T4_P (Link 0 Serial Data 4)	GROUND	LX2_T3_N (Link 2 Serial Data 3)	LX2_T3_P (Link 2 Serial Data 3)	GROUND
14	GROUND	LX2_T6_N (Link 0 Serial Data 6)	LX2_T6_P (Link 0 Serial Data 6)	GROUND	LX2_T5_N (Link 2 Serial Data 5)	LX2_T5_P (Link 2 Serial Data 5)	GROUND
15	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
16	GROUND	SCL_LIVE_BX_N (SCL Live Beam Crossing)	SCL_LIVE_BX_P (SCL Live Beam Crossing)	GROUND	CRATE_TO_SCLD_0_N (Crate to SCLD signal #0)	CRATE_TO_SCLD_0_P (Crate to SCLD signal #0)	GROUND
17	GROUND	CRATE_TO_SCLD_1_N (Crate to SCLD signal #1)	CRATE_TO_SCLD_1_P (Crate to SCLD signal #1)	GROUND	SCL_INIT_N (SCL Initialization)	SCL_INIT_P (SCL Initialization)	GROUND
18	GROUND	SCL_BEGIN_TURN_N (SCL Begin of Turn Marker)	SCL_BEGIN_TURN_P (SCL Begin of Turn Marker)	GROUND	SCL_BX_CLOCK_N (7.57MHz Beam Cross Clock)	SCL_BX_CLOCK_P (7.57MHz Beam Cross Clock)	GROUND
19	GROUND	SCLD_SPARE_P (Spare Signal)	SCLD_SPARE_P (Spare Signal)	GROUND	SAVE_MONIT_DATA_N (Save Monitoring Data)	SAVE_MONIT_DATA_P (Save Monitoring Data)	GROUND

Table 6.3. J0 Pin Assignments

7 Appendix C - D0 Level 1 Trigger System

Calorimeter

A component of the D0 detector experiment is a liquid argon calorimeter. The calorimeter is made by 55296 cells and consists of three units, the Center Calorimeter (CC), and the two End-cap Calorimeters (EC). The calorimeter readout system is being upgraded to improve its performance and the quality of the measurements.

Preamplifiers:

The charge from the calorimeter cells is integrated in the charge sensitive preamplifiers located on the calorimeter. The preamplifier input impedance is matched to the 30 Ω coaxial cables from the detector and the preamplifiers have compensated to match the varying detector capacitances.

BLS: Summer and Baseline Subtractor card.

The voltage signal generated by the preamplifier are then transmitted single ended on twisted-pair cable to the shaper and baseline subtractor (BLS) cards. The BLS process shapes the signal and removes slowly varying voltage offsets.

The signals from different depths in the electromagnetic and hadronic sections of the calorimeter are added with appropriate weights to form the “analog trigger tower sums”.

The BLS cards take care of the signal conditioning from pre-amplification to weighted sums. The cards are located in a limited access area directly beneath the detector (detector platform).

ADF: Analog to Digital converter and digital Filter board.

The 2560 “trigger tower sums” generated by the BLS cards are sent differentially over long ribbons of 80 Ω coaxial cables to the ADF (ADC and Digital Filter) boards. The Level 1 calorimeter trigger system, including the ADF sub-system, is located on the first floor of the moving counting house.

The ADF board performs the following functions:

Analog-to-Digital conversion of trigger pickoff signals, digital filtering, peak-detector, conversion from energy to transverse energy.

The Level 1 trigger system has 80 ADF boards distributed in 4 VME crates. An ADF board serializes the data and transmits it to the TAB (Trigger Algorithm Board) system over three 48-bit LVDS SER/DES links. These three links transmit exactly the same data to three different TAB boards.

Each ADF crate includes an interface to the Trigger Control Computer (TCC). This slow path is used for downloading, calibration and monitoring.

A timing distribution card connected to a Serial Control Link (SCL) receiver is in charge of distributing the necessary clocks, synchronization and control signals within the ADF system.

In order to perform preliminary test of the new L1 Calorimeter trigger system analog signal splitter cards have been designed. These cards duplicate the analog signals of several BLS's and connect to the CTFEs and the ADF cards being tested.

TAB: Trigger Algorithm Board. Each TAB connects to 30 LVDS input links from the ADF system. A TAB board runs the physics selection (sliding window) algorithms on one eighth of the

data produced by the ADF system. Results are transmitted to the Level 1 Global Algorithm Board (GAB), Level 2 / Level 3 and to the Calorimeter Track Match system.

GAB: Global Algorithm Board. Gathers results and computes global quantities such as missing transverse energy.

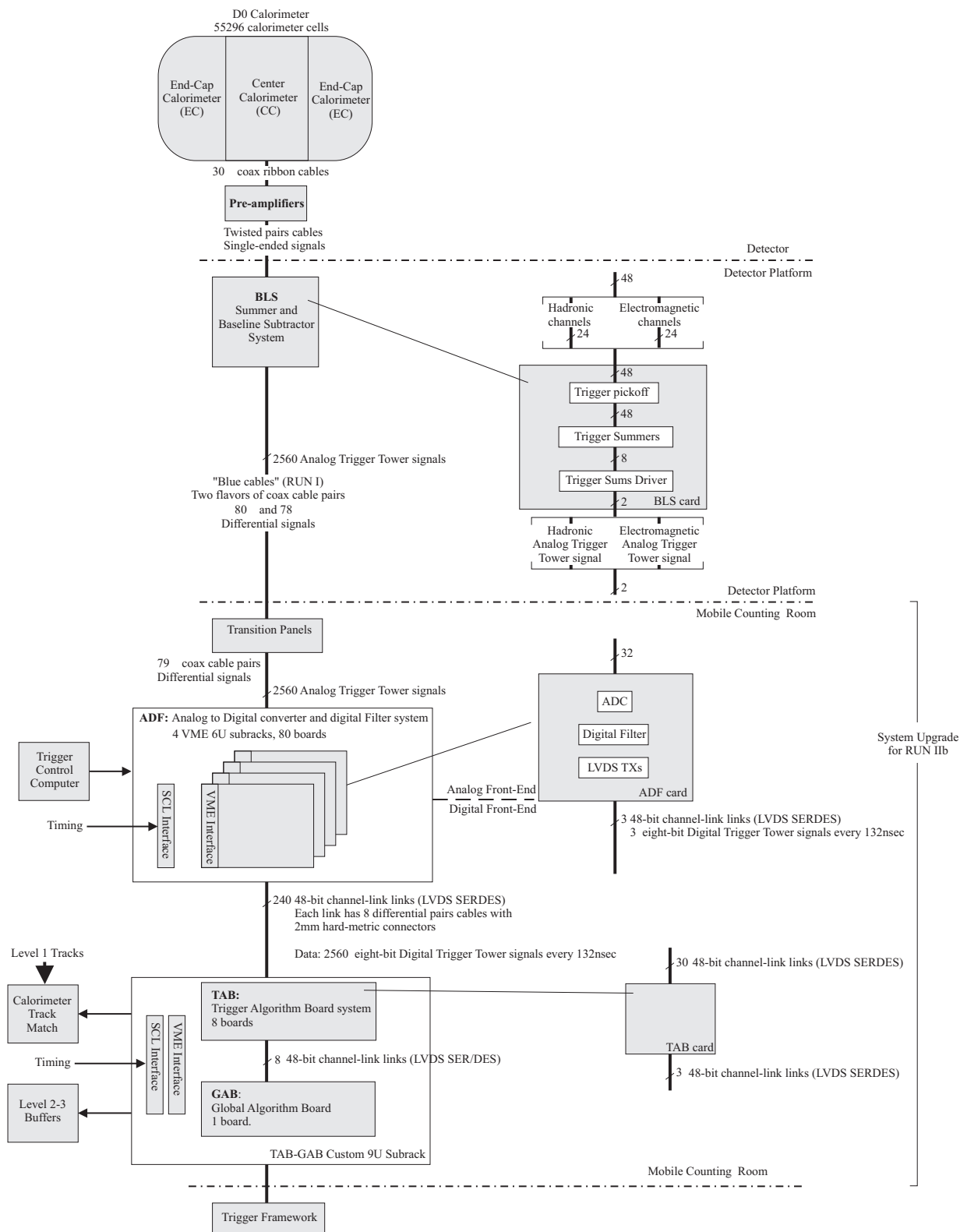


Figure 7.1, Calorimeter Level 1 Trigger block diagram

8 Glossary

ADF: Analog to Digital converter and Filter board. Component of the Run IIb D0 Level 1 Calorimeter System. See system diagram ().

BLS: Summer and Baseline Subtractor card. BLSs are a component of the Run IIb D0 Level 1 Calorimeter System. See system diagram ().

TAB: Trigger Algorithm Board. TABs are a component of the Run IIb D0 Level 1 Calorimeter System. A TAB run the physics selection algorithms on one eighth of the data produced by the ADF (Analog to Digital converter and Filter) boards. See system diagram ().

GAB: Global Algorithm Board. GABs are a component of the Run IIb D0 Level 1 Calorimeter System. See system diagram ().

SCL: Serial Command Link.

EM: Electromagnetic (calorimeter).

HD: hadronic (calorimeter).

IEEE: Institute of Electrical and Electronics Engineers, Inc. More information is available on the Internet:
<http://www.ieee.org/>

Jitter: The JEDEC Standard No. 65 (EIA/JESD65) defines jitter as the magnitude of the time deviation of a controlled edge from its nominal position.

Skew: The JEDEC Standard No. 65 (EIA/JESD65) defines skew as The magnitude of the time difference between two events that ideally would occur simultaneously.

VME/VME64X: [Ref.16] The VME (VERSAmodule Eurocard) standard was first defined in 1979 by Motorola Corporation. The VMEbus is an asynchronous bus that utilizes a *Master/Slave* architecture. The leftmost slot is the *Master*, and the remaining slots are *Slaves*. The VMEbus is composed of four sub-buses called the *Data Transfer Bus*, the *Data Transfer Arbitration Bus*, the *Priority Interrupt Bus*, and the *Utility Bus*. The original VMEbus standard maximum transfer speed is 40 Mbytes/sec. With the features of the newer VME64X standard described below, that transfer speed has quadrupled to 160 Mbytes/sec. Other features of VMEbus are:

-) 16, 24, or 32-bit addressing
-) 8, 16, 24, or 32-bit data path width
-) Allows unaligned data transfers
-) Error detection through *BERR signal
-) 7 levels of interrupts
-) System diagnostic capability using the *SYSFAIL signal
-) Mechanical standard allows 3U, 6U, or 9U printed circuit boards

The VME64X standard is a superset of the VME standard. Some of the added abilities for VME64X are:

-) Larger 64-bit data and address paths for 6U boards
-) 4 times the bandwidth (160 Mbytes/sec)
-) Cycle retry capability
-) Bus LOCK cycles
-) First slot detector
-) Automatic 'plug and play' features
-) A new 160-pin connector family
-) A 95-pin J0 connector

-) 3.3V supply pins
-) Geographical addressing
-) 141 more user-defined I/O pins

The VME64X standard utilizes 3 sets of connectors that plug into the backplane. They are a 95-pin connector J0/P0, and two 160-pin connectors, J1/P1 and J2/P2.

9 Attachment 1 - Purchase Proposal

9.1 Commercial equipment

One Arbitrary Waveform Source: **Agilent 33250A**

Listed Price: US\$ 4,552. Lead time: 3 weeks.



Figure 9.1, Agilent 33250A Function/Arbitrary Waveform Generator

Switch/Control System:

One **Agilent 3499A** Switch/Control System, 5 slot mainframe

Listed Price: US\$ 2,300. Lead time: 2 weeks.



Figure 9.2, Agilent 3499A Switch/Control System Mainframe

One **Agilent N2272A** 1 GHz 1x9 RF Multiplexer Module

Listed Price: US\$ 1,296. Lead time: 2 weeks.

Four **Agilent 44478A** Dual 1x4 RF Multiplexer Module (1.3GHz, 50 Ω)

Listed Price: US\$ 1,322. Lead time: 2 weeks.



Figure 9.3, Agilent 44478A Dual 1x4 RF Multiplexer Module

Equipment Cost (list): US\$ 13,406

Approximate discounted (GS) cost: **US\$ 12,065**

9.2 Extra equipment/component needed

a) One custom Transition Module to interface with ADF card.

(32 BNC or SMA inputs, single-ended to differential converters, impedance adapters, 32 differential output on a J2 style connector.

b) 32 SMB 50 Ω terminations. To terminate unused ADF inputs on the Agilent 44478A modules.

c) 41 coaxial cables terminated with BNC jacks, 50 Ω characteristic impedance.

One of the cables is used to connect the waveform generator to the switch system.

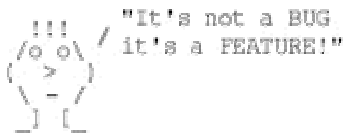
Eight cables to connect the first multiplexer (1x9) to the other four multiplexing modules (dual 1x4).

Thirty-two cables to connect the switch system to the VME64x transition module.

d) 32 BNC to SMA adapters if the transition module has SMA input connectors.

References

- [1] Test Waveform Generator System documentation
http://www-ese.fnal.gov/D0Cal_TWG/
- [2] D0 Calorimeter RunIIb Level 1 Trigger documentation:
<http://www.nevis.columbia.edu/~evans/l1cal/index.html>
- [3] Agilent (formerly Hewlett-Packard) documentation:
 - a) Probing Solutions for Agilent Technologies Logic Analysis Systems.
Information available on Internet:
<http://www.agilent.com/>
- [4] Feedback is very welcome.



- [5] The VMEbus Handbook, Wade D. Peterson, 4th Edition 1997. ISBN 1-885731-08-6.
- [6] RS-232
- [7] GPIB