# The ATLAS Level 2 Trigger

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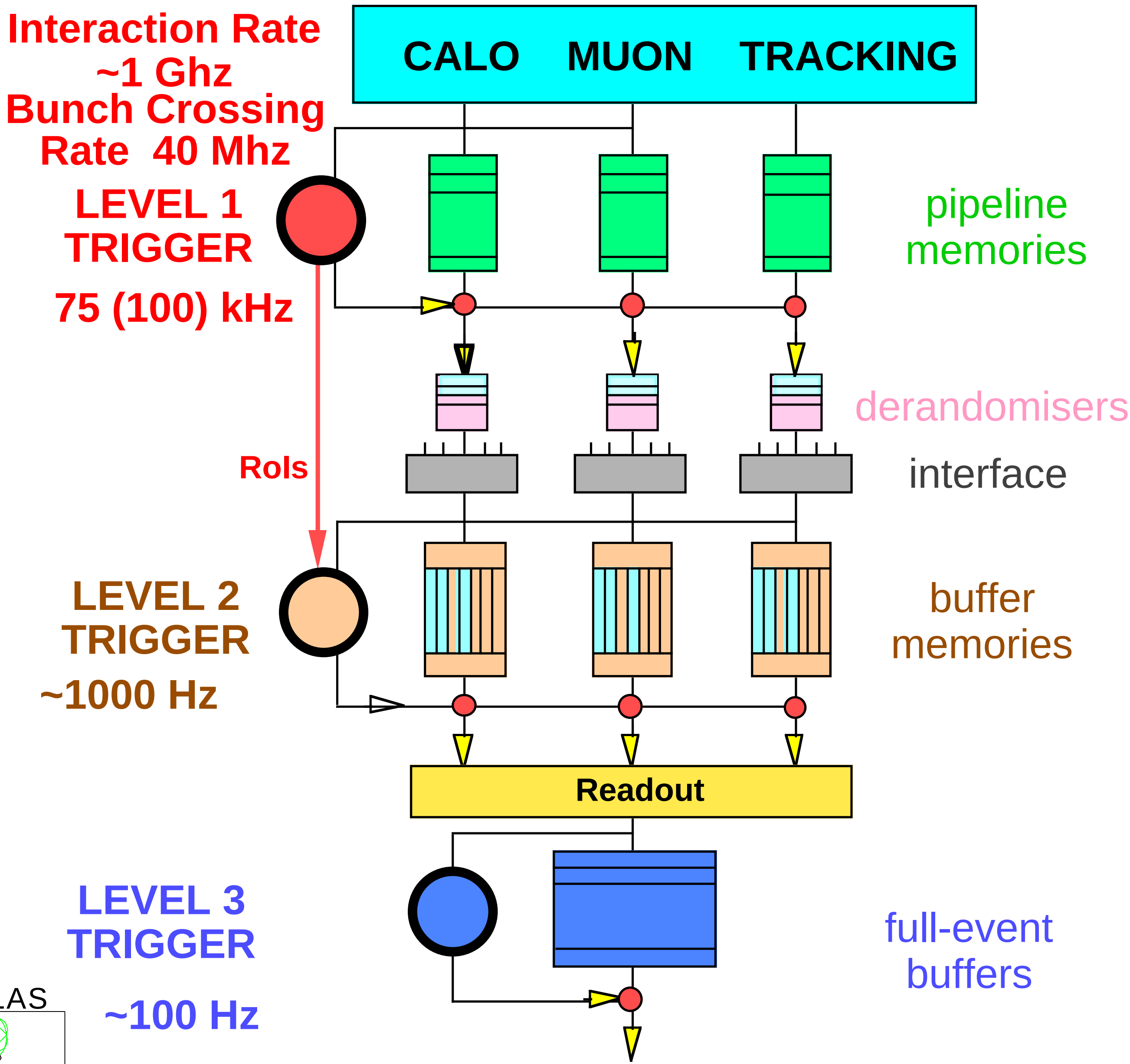
# Outline

- Trigger Overview
- Physics Challenges
- Level 2 Guidelines
- Longterm Strategy
- The Demonstrator Program
  - Demonstrator A
  - Demonstrator B
  - Demonstrator C
  - Common Activities
  - Modelling and Simulation
  - Hybrid Solutions
- Conclusions

# Trigger System Overview

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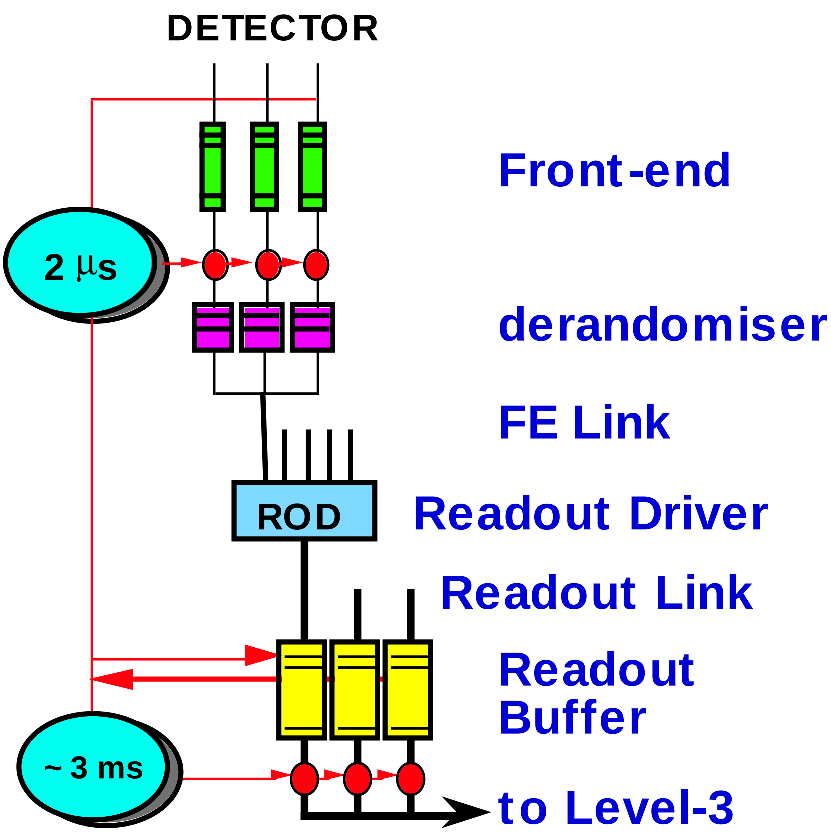
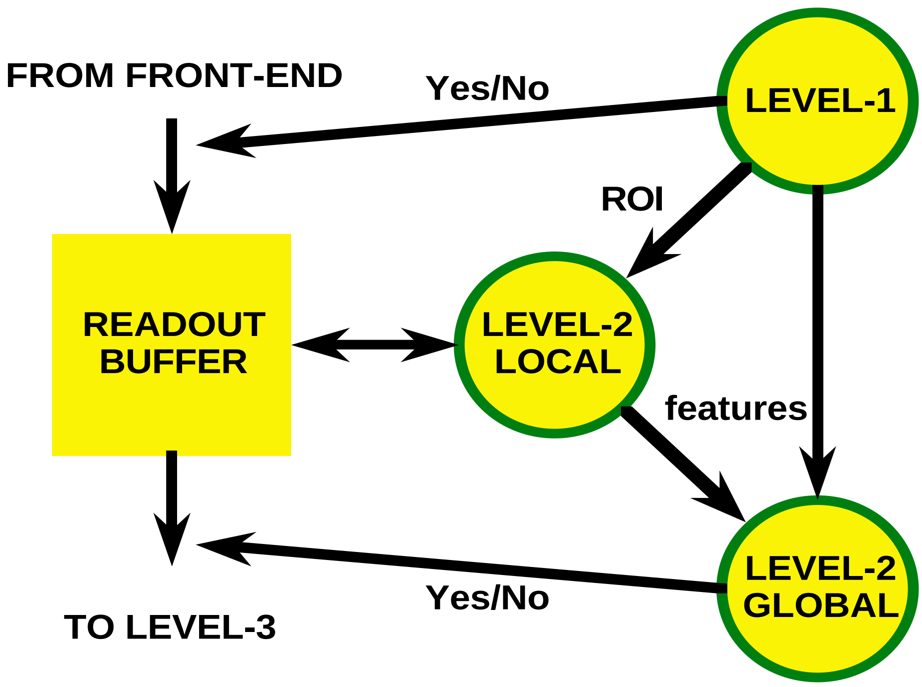
# Readout Buffers

- After a LVL1 accept, data are moved through a Readout Driver into an ATLAS standard Readout Buffer (ROB)
- The data are held in the ROB during LVL2 decision
- The data are moved to the LVL3 farm on receipt of a LVL2 accept



# Level 2 Trigger

- Works with data at full granularity
- Uses the Region of Interest (RoI) principle
  - LVL1 supplies RoI information
  - LVL2 transfers small fraction of data (~few %)
- Processing
  - Local - Feature extraction from sub-detectors
  - Global - Combine features

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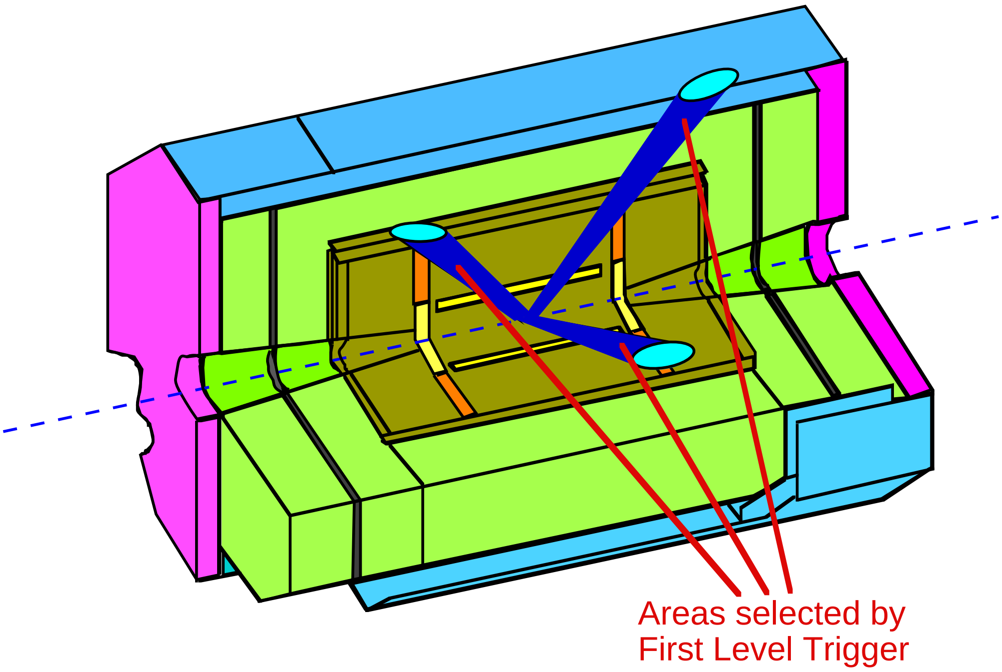
# Regions of Interest

## Regions of Interest (RoI)

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# Regions of Interest

- Number of RoI's
  ATLAS jet generation, 35 GeV threshold, $|\eta| \leq 3$
  - $\geq$ 5 GeV isolated em clusters = 2.6 average
  - $\geq$ 6 GeV no isolation (em) = 3.7 average
- RoI size
  - calorimeter - em cluster $\Delta\eta x \Delta\phi$ = 0.5x05
    --> 0.6% of total calorimeter area
  - SCT- size increased by z vertex spread
    -->1 - 4% of total Inner Detector area
- RoI Data Volume ~few % of total data volume
- Mapping of data onto ROB's may increase fraction

| System | RoI Size (kB) | Rate to L2 (GB/S) | Total Rate (GB/s) |
|---|---|---|---|
| SCT + pixels | 1.0 | 0.3 | 21 |
| TRT | 3.5 | 1.0 | 50 |
| Calo. | 2.5 | 0.7 | 35 |
| Muon | 1.0 | 0.3 | 20 |
| TOTAL | | 2.3 | 131 |

# RoI's continued

- Primary RoI's - those RoI's responsible for the LVL1 trigger
- Other RoI's
  - LVL1 tagged e.g. lower calorimeter thresholds
  - generated by Level 2 in sequential processing

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# Triggering Principles

- Level 1
  - 1% Deadtime
  - Pipelined
  - Uses custom hardware with fixed algorithms and programmable parameters
- Level 2 - to be determined
- Level 3
  - A farm of commercial processors
  - Running “offline” code

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# Examples of Physics Signatures

## $L = 10^{34} cm^{-2} s^{-1}$

| **Process** | **Level-1** | **Level-2** (I = isolated) |
|---|---|---|
| $H^0 \to \gamma\gamma$ | $\geq 2$ em, $E_T > 20$ GeV | $2\ \gamma$, $E_T > 20$ GeV |
| $H^0 \to ZZ^* \to \ell^+ \ell^- \ell^+ \ell^-$ | $\geq 2$ em, $E_T > 20$ GeV<br>$\geq 2\mu$, $p_T > 6$ GeV<br>$\geq 1$ em, $E_T > 30$ GeV<br>$\geq 1\mu$, $p_T > 20$ GeV | $2\ e$, $E_T > 20$ GeV<br>$2\ \mu$, $E_T > 6$ GeV, I<br>$1\ e$, $E_T > 30$ GeV<br>$1\ \mu$, $E_T > 20$ GeV, I |
| $(Z \to \ell^+ \ell^-) + X$ | $\geq 2$ em, $E_T > 20$ GeV<br>$\geq 2\mu$, $p_T > 6$ GeV<br>$\geq 1$ em, $E_T > 30$ GeV<br>$\geq 1\mu$, $p_T > 20$ GeV | $2\ e$, $E_T > 20$ GeV<br>$2\ \mu$, $E_T > 6$ GeV, I<br>$1\ e$, $E_T > 30$ GeV<br>$1\ \mu$, $E_T > 20$ GeV, I |
| $t\bar{t} \to$ leptons + jets | $\geq 1$ em, $E_T > 30$ GeV<br>$\geq 1\mu$, $p_T > 20$ GeV | $1\ e$, $E_T > 30$ GeV<br>$1\ \mu$, $E_T > 20$ GeV, I |
| $W', Z' \to$ jets | $\geq 1$ jet, $E_T > 150$ GeV | 1 jet, $E_T > 300$ GeV |
| SUSY $\to$ jets $\to E_T^{miss}$ | $\geq 1$ jet, $E_T > 150$ GeV<br>$E_T^{miss} > 150$ GeV | 3 jet, $E_T > 150$ GeV<br>$E_T^{miss} > 200$ GeV |

$\ell\,\gamma$ for $|\eta| < 2.5$; Jets for $|\eta| < 3.$; Missing $E_T$ for $|\eta| < 5$; RoI's on all $e/\gamma > 10$ GeV& $\mu$'s > 6 GeV $p_T$.

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# Trigger Rates - Level 1

| **Trigger selection** | **Rate at $L = 10^{34}$ cm$^{-2}$ s$^{-1}$** |
|---|---|
| Single muon, $\geq 1\ \mu$, $p_T \geq 20$ GeV | 4 kHz |
| Single e.m. cluster, $E_T \geq 30$ GeV, e.m. and hadronic isolation | 20 kHz |
| Double muon, $\geq 2\ \mu$, $p_T \geq 6$ GeV | 1 kHz |
| Double e.m. cluster, $E_T \geq 20$ GeV, e.m. and hadronic isolation | 4 kHz |
| Single jet, $\geq 1$ jet, $p_T \geq 150$ GeV | 3 kHz |
| $E_t^{miss} > 150$ GeV | 1 kHz |
| other triggers | 5 kHz |
| **Combined rate** | **~38 kHz** |

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# Expected LVL2 trigger rates (TP)

indicative rates for inclusive selections

| **Trigger selection** | **Rate at $L = 10^{34}$ cm$^{-2}$ s$^{-1}$** |
|---|---|
| Isolated muon, ≥ 1 μ, $p_T$ ≥ 20 GeV,<br>single muon, ≥ 1 μ, $p_T$ ≥ 40 GeV | 0.2 kHz<br>0.1 kHz |
| Single electron, ≥ 1 e $E_T$ ≥ 30 GeV,<br>single gamma, ≥ 1 γ $E_T$ ≥ 60 GeV | 0.3 kHz<br>0.1 kHz |
| Isolated di-muon, ≥ 2 μ ,$p_T$ ≥ 6 GeV<br>double muon, ≥ 2 μ ,$p_T$ ≥ 10 GeV | 0.1 kHz<br>0.08 kHz |
| Di-electron or di- gamma, $p_T$ ≥ 20 GeV, | 0.2 kHz |
| Single jet, ≥ 1 jet, $p_T$ ≥ 300 GeV | 0.1 kHz |
| $E_T^{miss}$ > 200 GeV | 0.1 kHz |
| other triggers | 0.1 kHz |
| **Combined rate** | **~1.4 kHz** |

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# Expected LVL2 Inclusive rates at Low Luminosity (TP)

| **Trigger selection** | **Rate at $L = 10^{33} cm^{-2} s^{-1}$** |
|---|---|
| B-physics Level-2 triggers,<br>single muon, ≥ 1 μ, $p_T$ ≥ 20 GeV | 0.8 kHz<br>0.2 kHz |
| Single electron, ≥ 1 e $p_T$ ≥ 20 GeV,<br>single gamma, ≥ 1 γ $p_T$ ≥ 40 GeV | 0.2 kHz<br>0.06 kHz |
| Dual electron, ≥ 2 e $p_T$ ≥ 15 GeV,<br>dual gamma, ≥ 2 γ $p_T$ ≥ 20 GeV | 0.01 kHz<br>0.01 kHz |
| Single jet, ≥ 1 jet, $p_T$ ≥ 200 GeV<br>three jet, ≥ 3 jet, $p_T$ ≥ 100 GeV | 0.06 kHz<br>0.02 kHz |
| $E_T^{miss}$ > 200 GeV | 0.01 kHz |
| Prescaled triggers | 0.1 kHz |
| **Combined rate** | **~1.5 kHz** |

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More recent Trigger Menu Studies
can be found in DAQ-NO-54

# Rates for B-physics (TP)

| **Trigger selection** | **Rate at $L = 10^{33}$ cm$^{-2}$ s$^{-1}$** |
|---|---|
| Level-1 single muon, $p_T \geq 6$ GeV | 8000 Hz |
| Level-2 single muon, $p_T \geq 6$ GeV | 4000 Hz |
| Additional Level-2 requirements | |
| second muon, $p_T \geq 5$ GeV | 56 Hz |
| electron, $p_T \geq 5$ GeV | 112 Hz |
| electron pair, $p_T \geq 1$ GeV | 400 Hz |
| hadron pair, $p_T(h) \geq 6$ GeV with $p_T(\text{pair}) \geq 15$ GeV | 100 Hz |
| $D_S^{\pm} \rightarrow \phi\pi^{\pm} \rightarrow K^{+}K^{-}\pi^{\pm}$ with $p_T \geq 1$ GeV and loose mass cuts | 160 Hz |
| **Combined rate** | **~830 Hz** |

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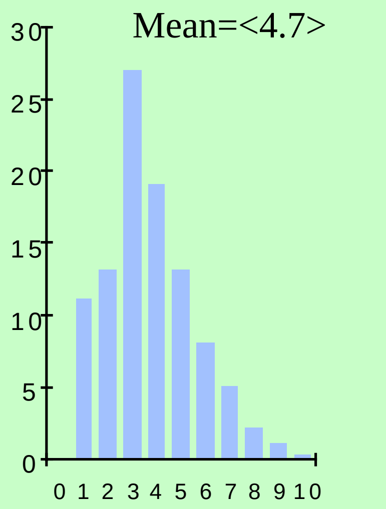
# Level-2 Processing

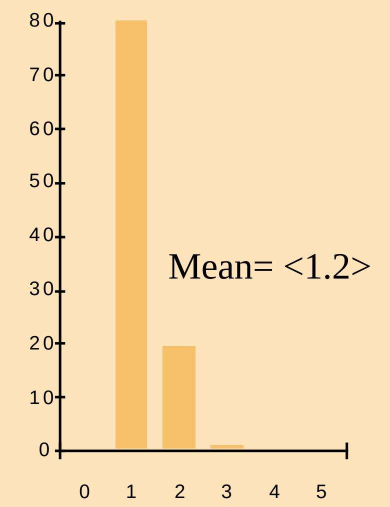
- Algorithms only: no preprocessing or system overhead
- Calorimeter
  peak find and shape analysis - 100 µs @500 mips
- Continuous Tracking (TRT)
  histogramming method - 600 µs @500 mips
- Precision Tracking
  histogramming method - 800 µs @500 mips
- Muon (2 step process)
  - Pattern recognition
  - $p_T$ calculation

100 µs with non-optimised code

# Motivation for Sequential Processing




**Total Number of RoI's**




**No. of "Trigger" RoI's**

| Luminosity | Low | High |
|---|---|---|
| Thrshld (Gev) | 20 | 40 |
| Calo alone | 3 | 10 |
| Calo +Track | 25 | 60 |

**Background Rejection Factor at 90% eff. for em Trigger RoI's**

| Algorithm | Proc. time |
|---|---|
| Calor | 50-100 μsec |
| Muon | < 100 μsec |
| Track | 500-5000 μsec |

**Timing Benchmarks for Selected Algorithms**

**500 Mips processors**

- Only 1.2 Trigger RoI's for 4.7 L1 "objects"
- Only 10%-20% of Trigger RoI's survive first step
- Tracking algorithms are slower by x 10

**Suggested Procedure:**

**•Confirm Trigger RoI's using Calorimeter and Muon alone**

**•Do track finding only if necessary**

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# Strategy Meeting (Cosener's House, June '95)

- Decision made to produce User Requirement Document (URD)
- Establish Milestones
  - Architectural Choice e.g.
    - data driven elements vs multiple farms
    - control via network or separate lines
    - algorithmic complexity
    - "push" (data transfer initiated by source node) or "pull" (data transfer initiated by target node)
  - Technological Choice e.g.
    - switch and data concentrator technology
    - farm technology
    - network technology

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# Demonstrator Program

- Why
  - Explore architectural options
  - Explore technical options
  - Optimize choice financially and technologically
  - Time and expertise on hand
- Common Yardstick
  - 100 kHz operation
  - Demonstration of scalability to full detector
  - User Requirement Document
- Task Force Decision
  - Three Demonstrators (A, B, C)
  - Mix architectural and technological considerations in a single demonstrator program

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# Interim Milestones
# (to be updated)

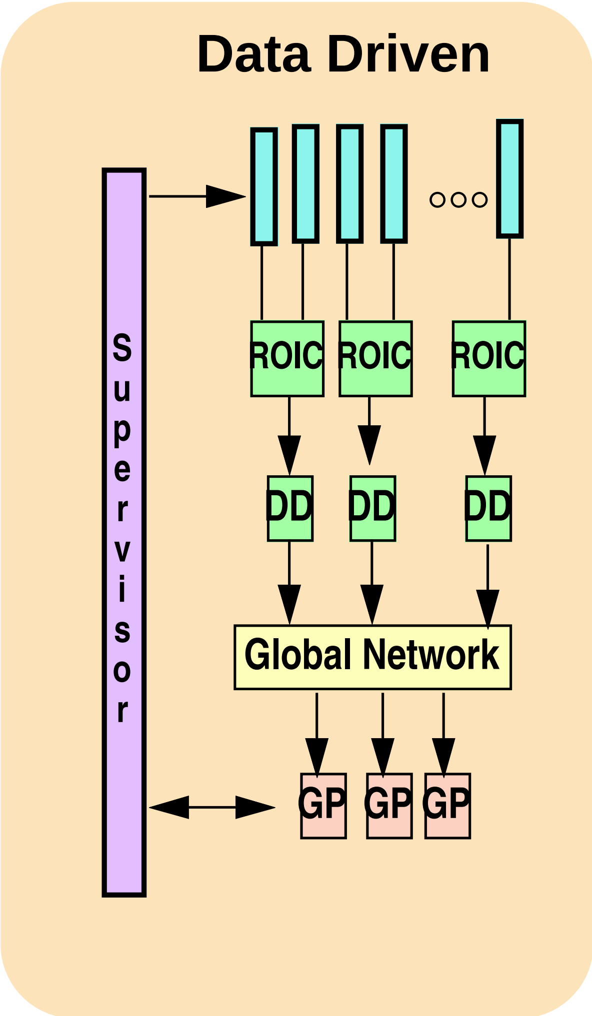
- **Sep 1997** - Major Architecture Choices Made
- **Dec 1997**-T/DAQ Technical Proposal Due
- → **Jul 1998** - Major Technology Choices Made
  Small-Scale Prototype (SSP) Defined
- **Jul 1999** - SSP assembled
- **Jan 2001** - Full-chain prototype (FCP) defined
- **Jan 2002** - FCP accepted
- **Jan 2003** - Commissioning of LVL2
- **Jul 2003** - Integration of LVL2 with rest of T/DAQ
- **Jan 2004** -Integration of LVL2 with subdetectors
- **Jan 2005** - Run with cosmic rays
- **Jul 2005** - Full Level-2 ready for collisions

# Demonstrator Participants

Overall Coordinator: Fred Wickens

- Demonstrator "A" -
  - Coordinator: Prof. Reiner Maenner
  - Institutes: Cracow, Heidelberg, Jena, Mannheim, Weizmann
- Demonstrator "B"
  - Coordinator: John Renner Hansen
  - Institutes: Argonne, CERN, NBI(Copenhagen), Cracow, Edinburgh, JINR, Lecce, Liverpool, Manchester, Michigan State, NIKHEF, Oxford, RAL, RHBNC, UFRJ(Rio), Rome INFN, Valencia, UCL
- Demonstrator "C"
  - Coordinator: Patrick Le Du]
  - Institutes: Argonne, CERN, Michigan State, Oxford, Rome, Lecce, Saclay, Prague

# L2 Architecture "A"




- Optimized for Fast Feature Extraction (FPGA). Based on Enable++.
- Operates in Push Mode

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# Architecture A

## Potential advantages

- "On the fly" RoI collection
- Feature Extraction at 100 kHz.  Typical FPGA execution times: 10 μs. Minimal latency
- Smaller system
- Simplified supervision and control

## Possible problems

- Algorithmic complexity may be limited $\rightarrow$ higher output rates
- May be difficult to combine detectors with different geometries e.g. barrel and endcap
- Sequential processing probably ruled out

# Critical Demonstrations for Architecture A

- In parallel collection of several RoI's in a given subdetector at 100 kHz
- Data-driven feature extraction for all detectors at 100 kHz
- Demonstration of satisfactory algorithmic adaptability to different luminosity conditions, changing run requirements and to evolving physics demands
- Event synchronization

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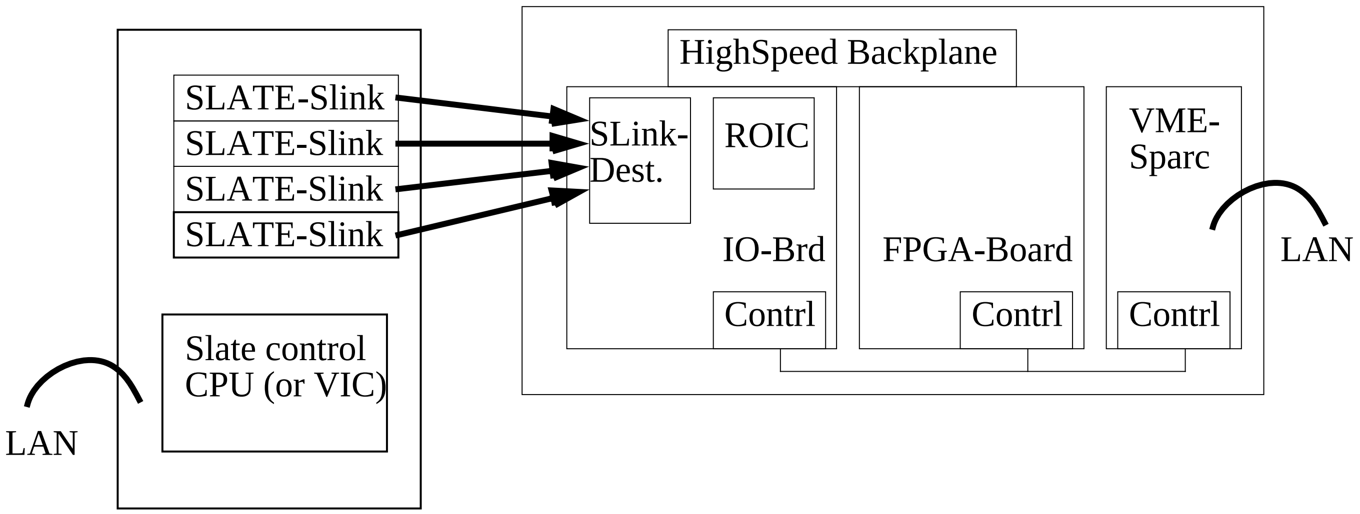
# Demonstrator A Hardware Layout

Goal: RoI collection and FEX @ 100 kHz

Slate crate, VME

Enable ++ System crate




1 Slate = 1 ROB Crate or input from preceeding RoIC

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## SLATE is a fast data emulation device

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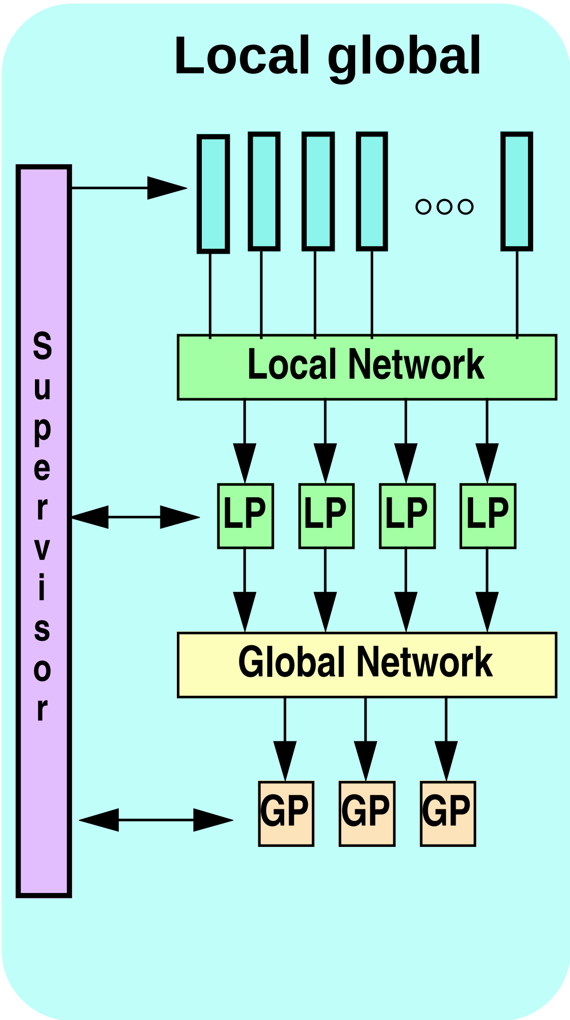
# L2 Architecture B
# Data Flow Diagram




- Optimized for parallel processing of RoI's and detectors
- Operates in push mode
- This is the Technical Proposal Design
- The two networks shown may be partitions of the same network

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# Architecture B

## Potential Advantages

- Flexibility inherent in general purpose processors
- Lower latency from parallel processing and data flow

## Possible Problems

- Sequential processing presents challenges
  - logic control
  - latency issues
- More processing power may be needed

## Critical Demonstrations

•Achieve complete RoI collection at 100 kHz.  Involves ROB’s, supervisor and network interacting with feature extraction (FEX) processors.

•Feature extraction can be done for all detectors within local network bandwidth limits and financial constraints.

•Supervisor functioning at full rate.

•Sequential processing control paths and performance at full bandwidth. Event synchronization.

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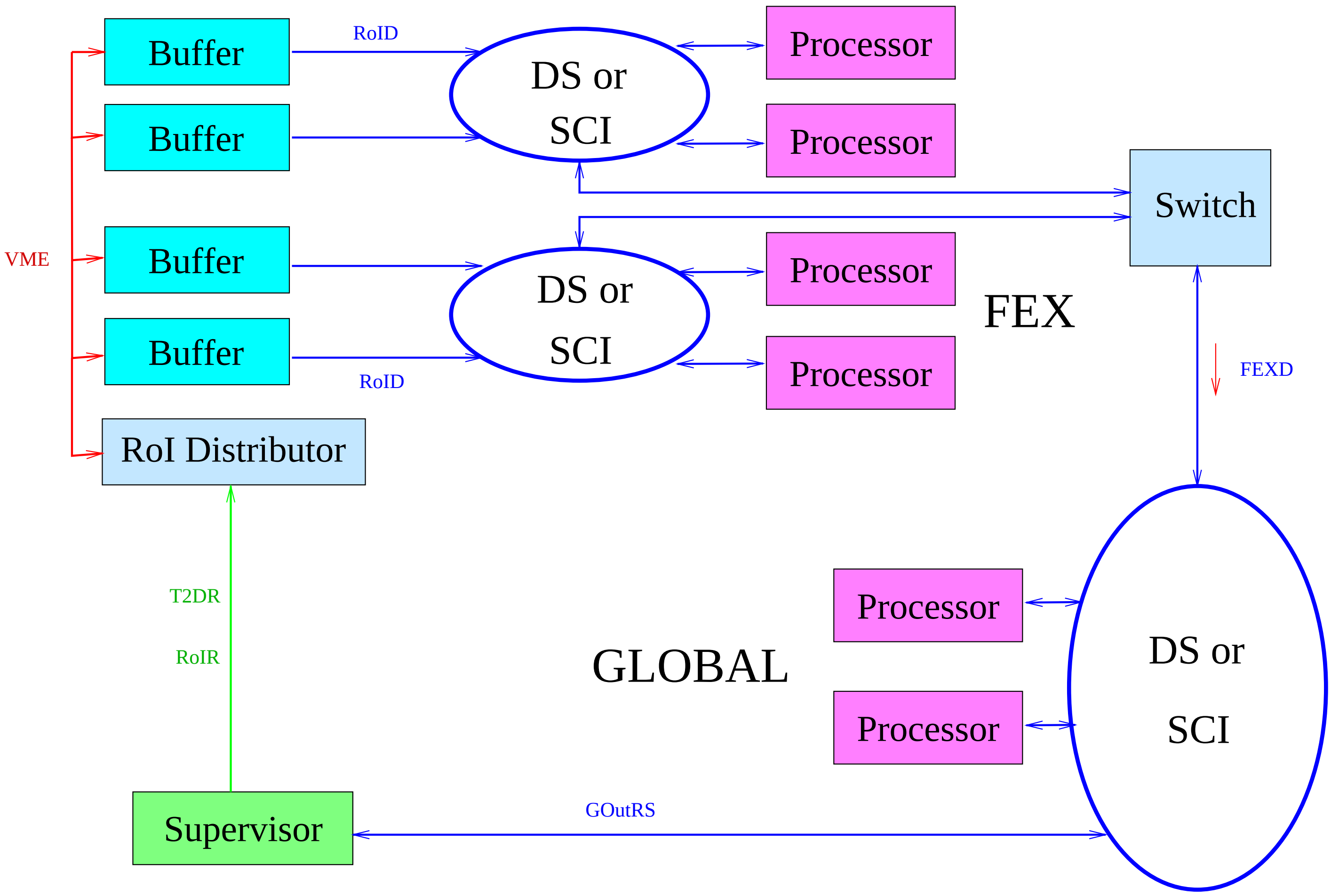
# Demonstrator B2

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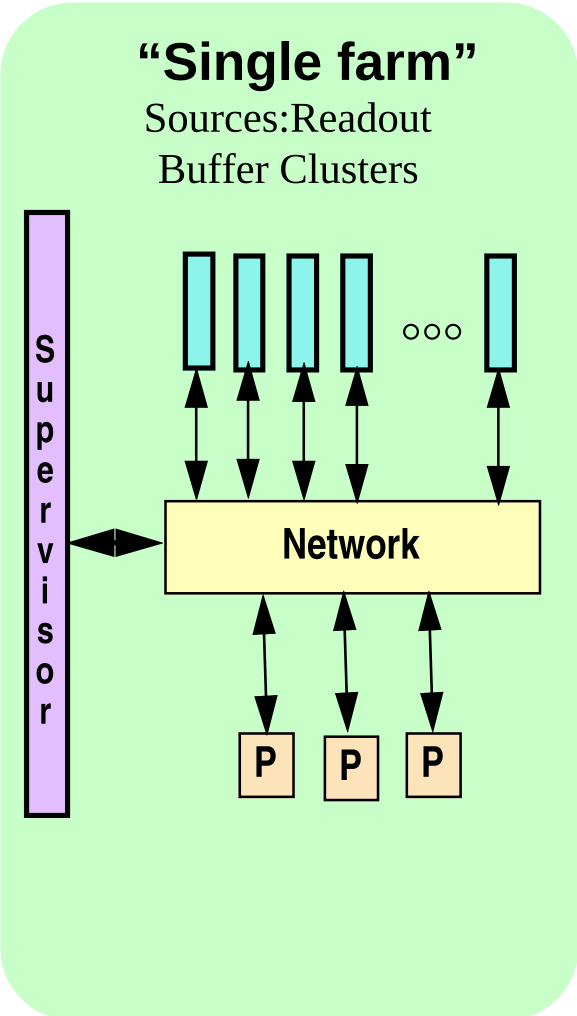
# L2 Architecture C




- Optimized for sequential processing of RoI's
- Operates in pull mode
- Distinction between Level 2 and Level 3 disappears

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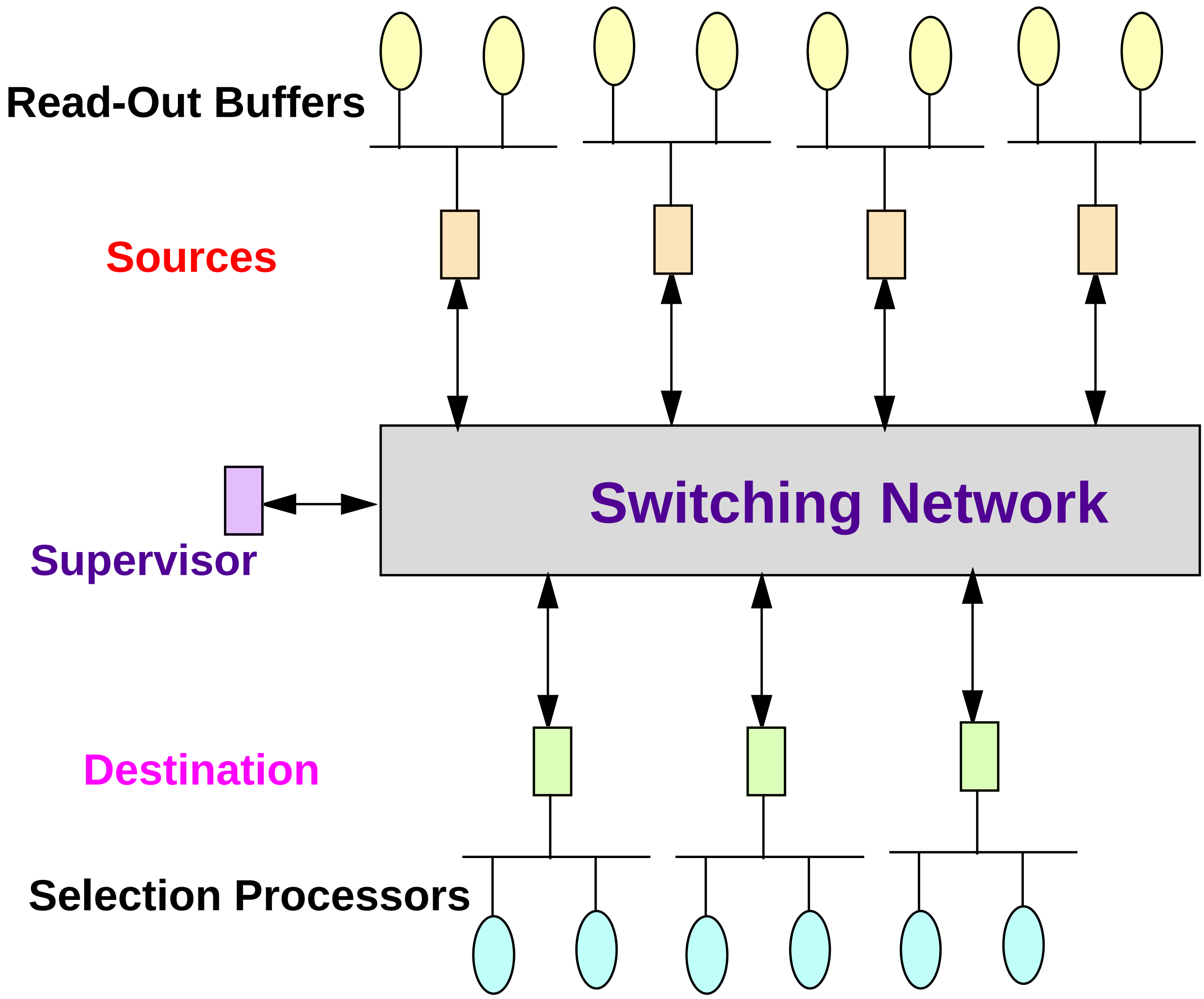
# The Single Farm Idea




*Main features*

- **Integration of data and protocol networks**
- **Pull data flow control strategy**
- **Single processor per event**
- **Several events per processor**

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# Architecture C

## Potential Advantages

- Well adapted to sequential processing
- Destination can also be Event Builder and Level 3 processor

## Possible Problems

- Data and control traffic on same switch
- Multiple events per processor

## Critical Demonstrations

•Data and control traffic patterns are within network capabilities.

•Complete RoI collection can be achieved.

•Data concentrators do not impede data flow

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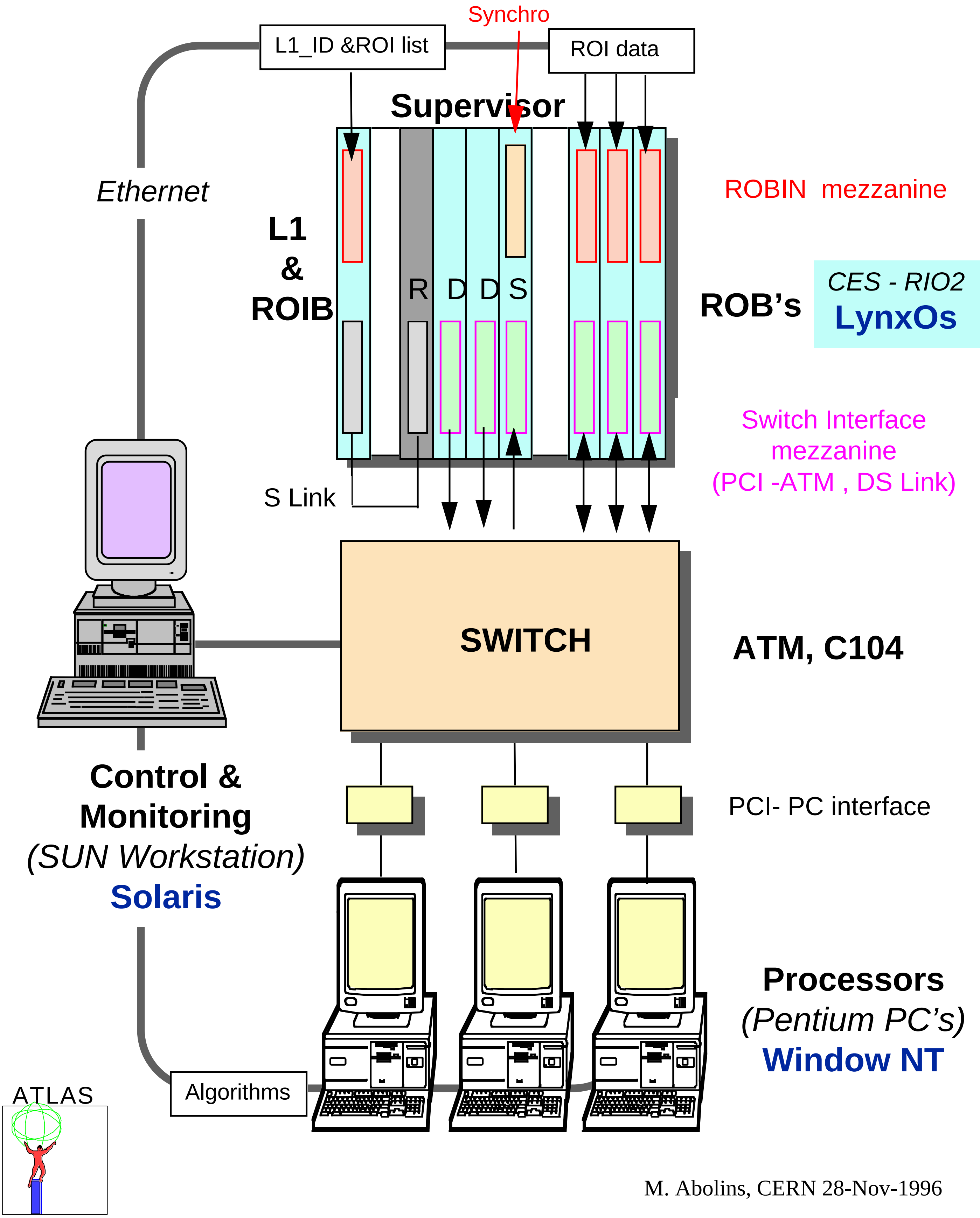
# Demo C for Testlab

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# Common Areas for Demonstrators

- Base-line definitions of
  - detectors
  - data formats
  - ROB/RoI sizes
  - algorithms
  - data samples
- Common hardware and software
  - ROB's
  - Supervisor
- Modelling and Emulation
- Performance Measurements

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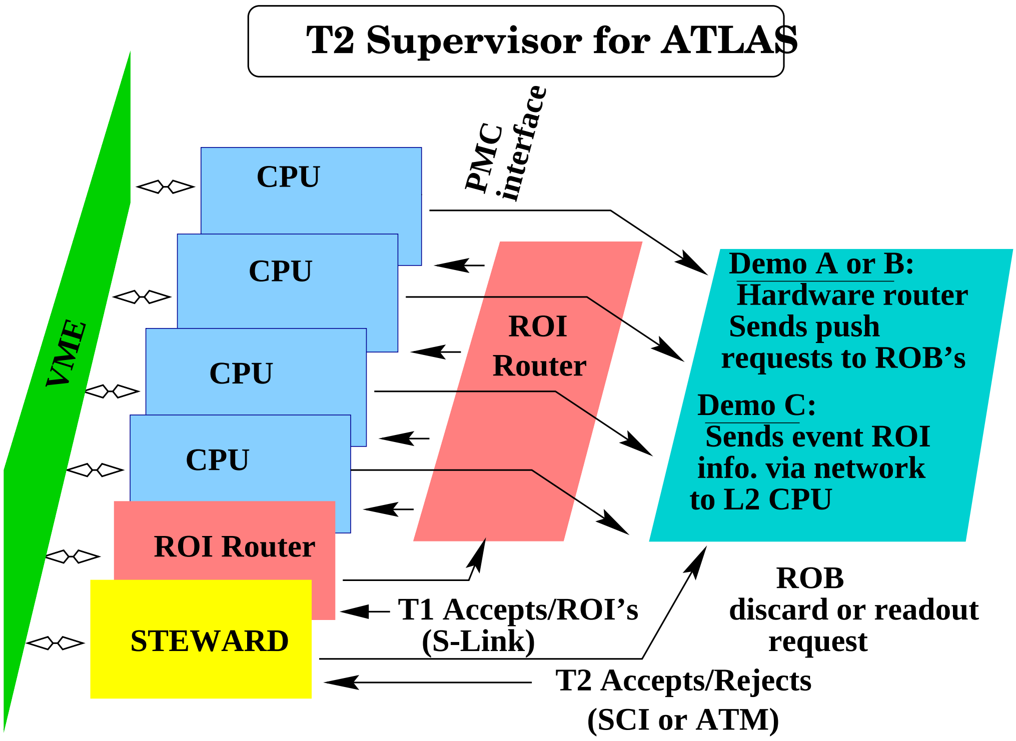
# Level 2 Supervisor




**TASKS**

**STEWARD: Manages (frees and reviews usage of) local and global processors**

**ROI Router: dispatches ROI information to CPU's**

**CPU's: determine appropriate free local/global processors to use and determine buffers to request data from and assemble request packet**

**ROB Router: routes buffer requests to appropriate crates (A&B only)**

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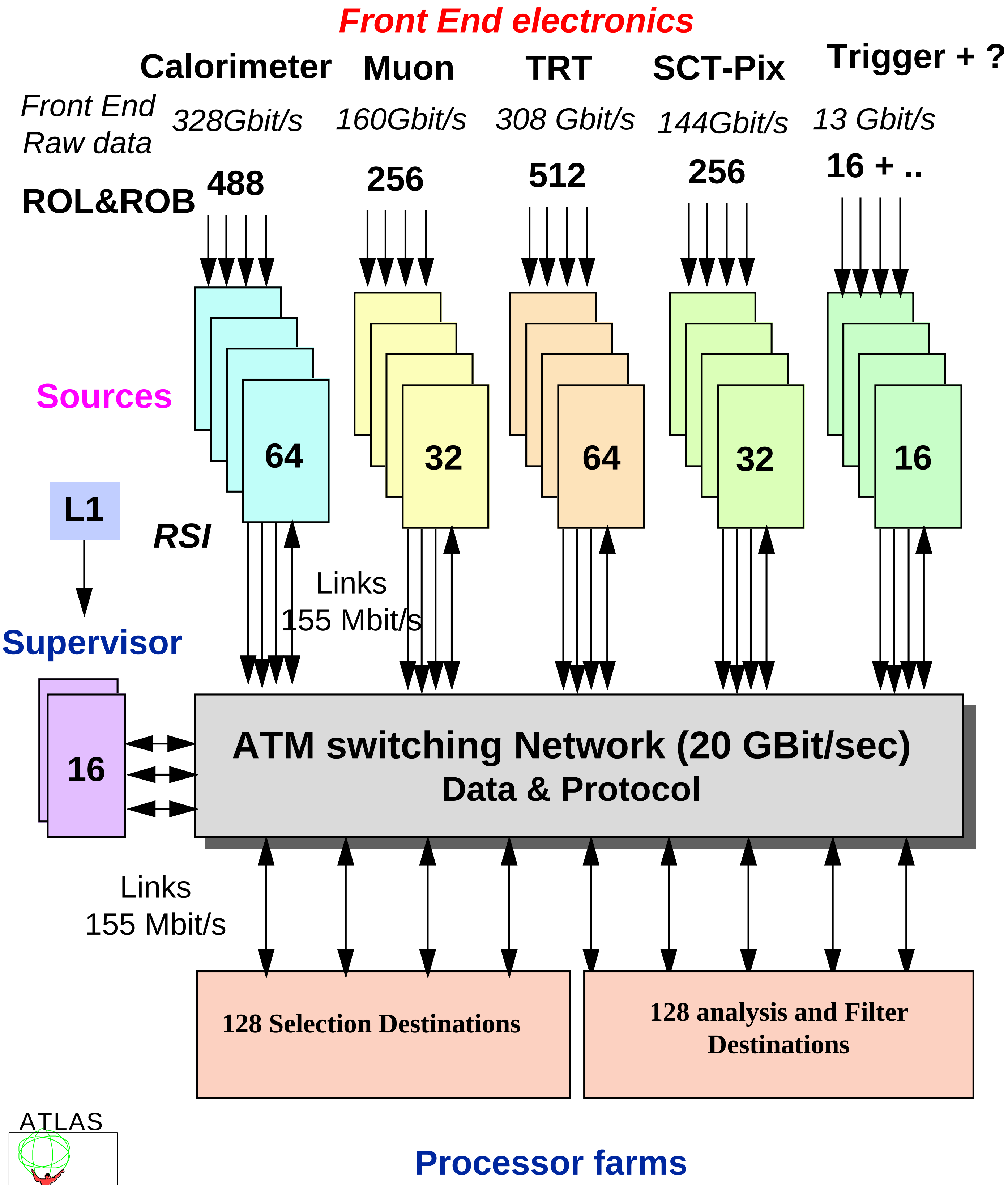
# Modelling and Simulation

- Paper Models
  - Inputs
    - Full Trigger Menus
    - Average Numbers of RoI's
    - Average processing times, overheads, circuit delays etc.
  - Output
    - Number of processors needed
    - Switching bandwidth needed
    - Link occupancy
    - Overall latency
  - Does not model
    - Possible queueing problems
    - Data flow fluctuations
  - Initial studies for Model C at Saclay now A & B also modelled.
- Modsim II and C++ Studies underway

# Paper Model - Architecture C

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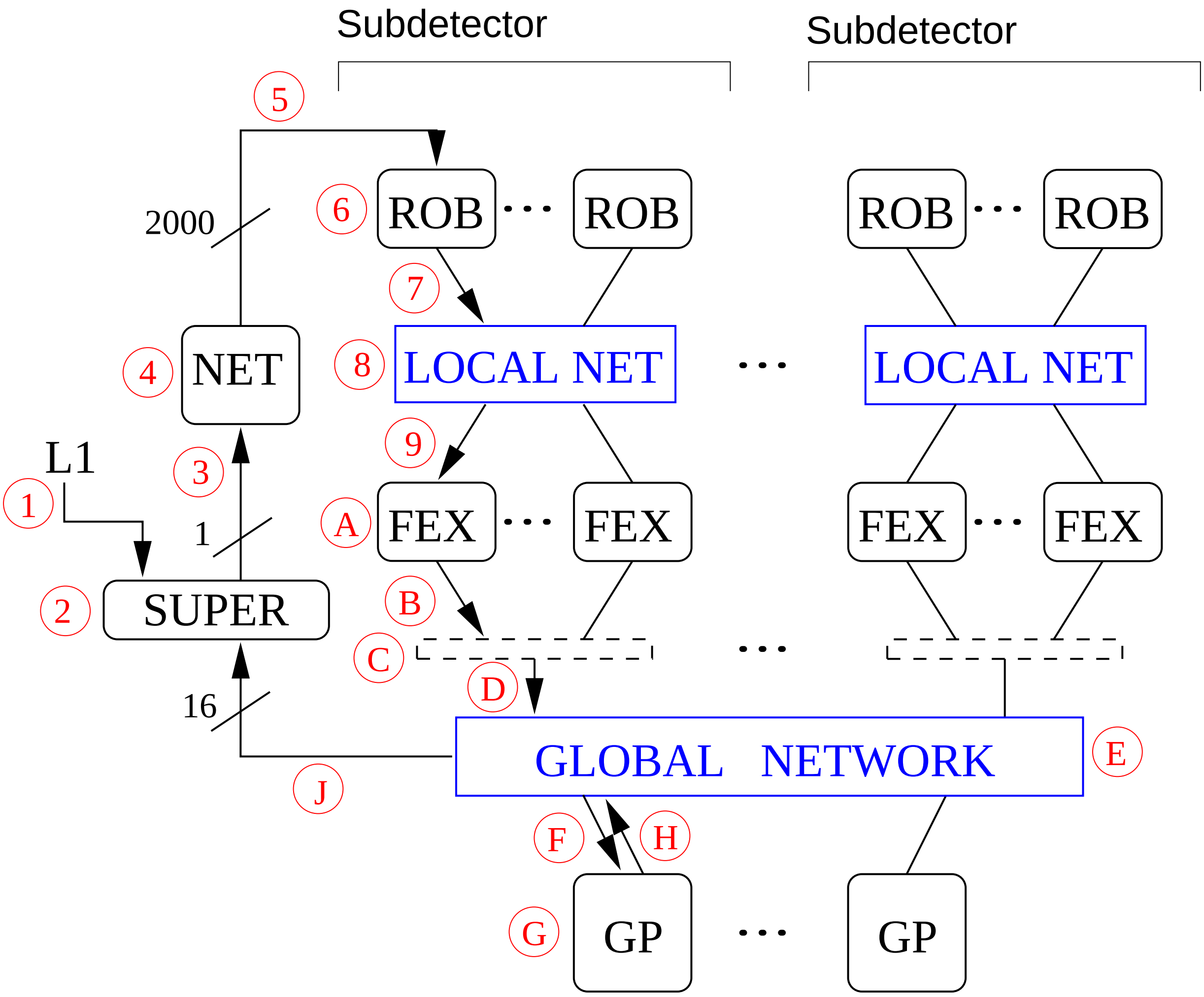
# Paper Model Diagram
# Architecture B

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# Hybrid Solutions

- We are actively examining the relative merits of general purpose versus FPGA processors for specific high intensive computing tasks.

- Both architecture B and architecture C are considering FPGA processors for full TRT scans and for b-jet scans of the SCT.

# Questions and Conclusions

- Questions
  - Is sequential processing necessary?
  - Are secondary RoI's necessary?
  - Does missing $E_T$ need to be recalculated at Level 2?
  - Do we need a full TRT scan at Level 2?
  - Do we need b-jet tag at Level 2?
  - How is the LVL2/LVL3 boundary defined?
  - Do we need preprocessing?
- Conclusions
  - A robust and comprehensive demonstrator program is underway
  - Efforts are being made to integrate elements of the separate architectures for an optimal design
  - Prospects are good for a Level 2 that will be optimized in price and performance and that will benefit from technological innovations in the commercial sector