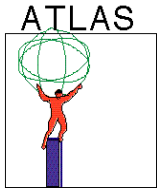
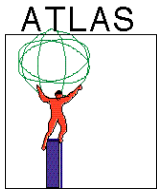


LVL2 RoI Builder

Maris Abolins

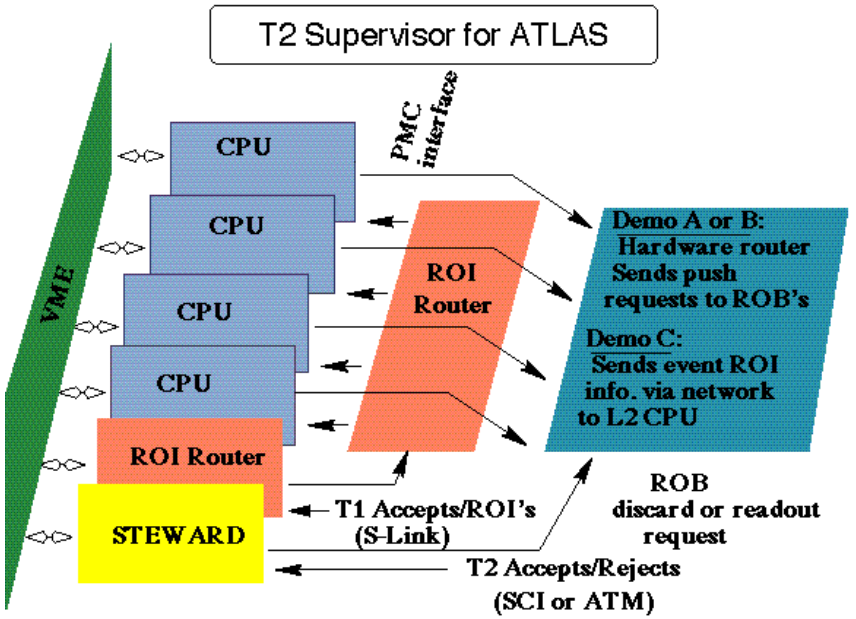
Michigan State University



Outline

- Review of Supervisor/RoI Builder (SRB)
- Guiding Principles in SRB Design
- RoI Data from LVL1
  - Raw data from calorimeter
  - Compressed data input from LVL1
- Bandwidth Issues
- Steward Limitations
- Possible Solutions

Supervisor/RoI Builder



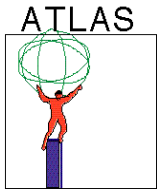
TASKS

STEWARD: Manages (frees and reviews usage of) local and global processors

ROI Router: dispatches ROI information to CPU's

CPU's: determine appropriate free local/global processors to use and determine buffers to request data from and assemble request packet

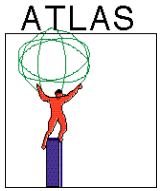
ROB Router: routes buffer requests to appropriate crates (A&B only)



Guiding Principles

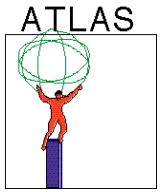
- Bandwidth is important: Compress data at LVL1 end - don’t ship 0’s. Must get data into a single processor in < 10μs.
- Processing will not be a problem. Processors are getting faster and we can always add more processors.
- Arrange data for quick retrieval of co-ordinates
  - When compressing data, respect Byte or word boundaries. This eliminates time-consuming bit shifting/masking operations.

Raw Data from Calorimeter



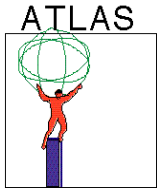
- jets
  - For each of 8 thresholds a map of 0.4 x 0.4 granularity-->256 Bytes
- e/γ
  - As for jets: 256 Bytes
  - For one threshold a map of 01 x 0.1 granularity-->512 Bytes
- Single hadron/τ - Same as jets?

Compressed LVL1 Data to SRB

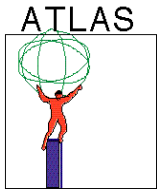


- Jets - Use maximal compression: RoI coordinate = 8 bits, threshold 3 bits. Pad 11 bits to 16. For 5 RoI's get 10 Bytes; add 2 Bytes for header and trailer. Total = 12 Bytes
- e/γ - 16 bits/RoI for coarse maps is the same as for Jets. Fine map needs 12 bits per hit; pad to 16. Assuming 5 RoI's in each this gives 24 Bytes.
- hadron/t - assume same as Jets = 12 Bytes
- Muon - 90 Bytes (Ph. Farthouat 5-Feb-1997)
- $E_T$miss - 4 Bytes
- CTP - Assume 64 Bytes
- **Total** (overestimate) = 12 + 24 + 12 + 90 + 4 + 64 = **206 B**

RoI Router Bandwidth Issues

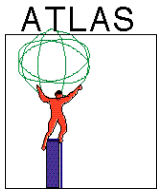


- At 100 KHz, average bandwidth into 1 processor must be ~ 20 MB/s
- Data comes in on 6 cables
- Input Router bandwidth (JWD) = 200 MB/s but there is arbitration.
- Limitations at input to a single processor: PCI bus
  - Nominal standard - 133 MB/s
  - As implemented on RIO2 < 133/2 MB/s
  - Actual measurement ~ 40 MB/s
  - “Realistic” expectation with arbitration ~20 MB/s
- Conclusion - Maybe OK.



Steward Limitations

- Global processors send 64 Bytes to Steward - Average Bandwidth ok.
- Bus Contention by many (100's?) global processors will present problems.
- Must respond to free processor list requests from RoI procesors. More bus contention.
- Processing time is limited ~10 μs



Possible Solutions

- Multiple Stewards - Each manages a fraction of processors thereby addressing input bandwidth problems
- Problems - Probably implies inefficient use of processing resources.
- Other ideas are being discussed. Realistic modelling of RoI Builder/Supervisor is needed and is being planned.