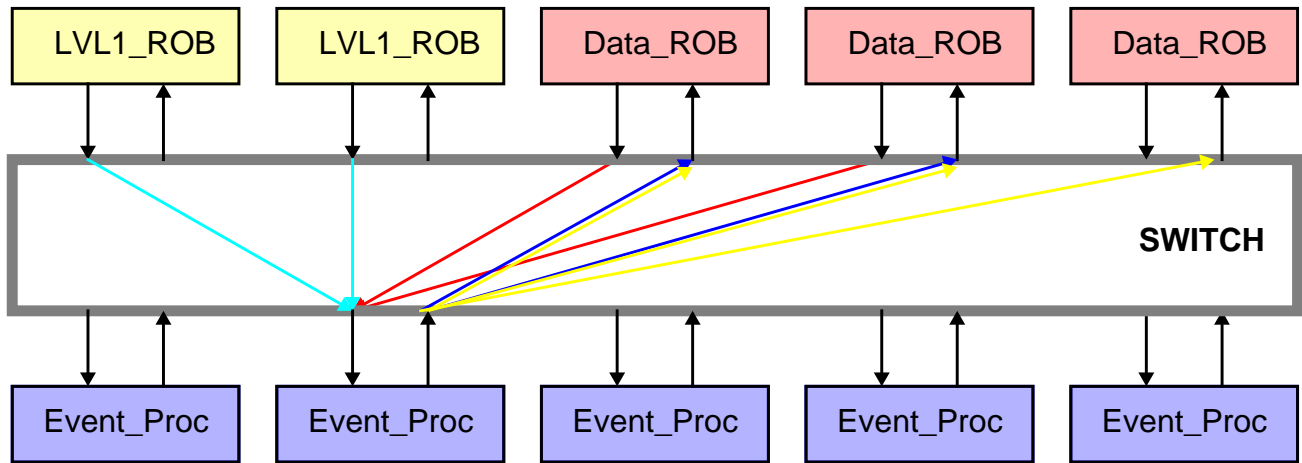


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# The Level-2 Supervisor for the Demo-C

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## Distributed Supervision (Architecture C)



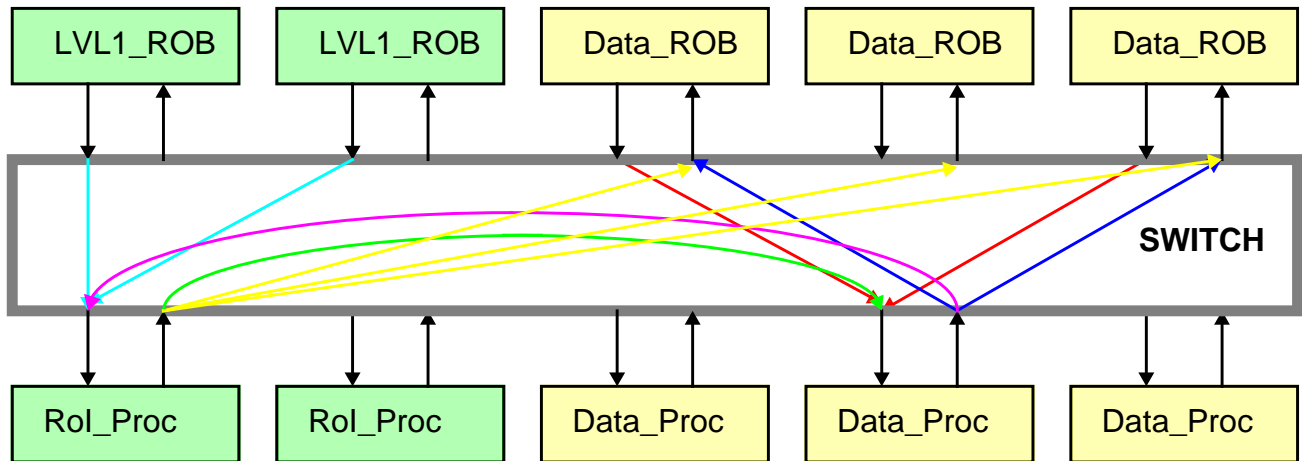
**LVL1 data sending**  
**Data request**  
**Data delivery**  
**Decision broadcast (T2DR)**

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# The Level-2 Supervisor for the Demo-C

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## Distributed Supervisor (Architecture C)



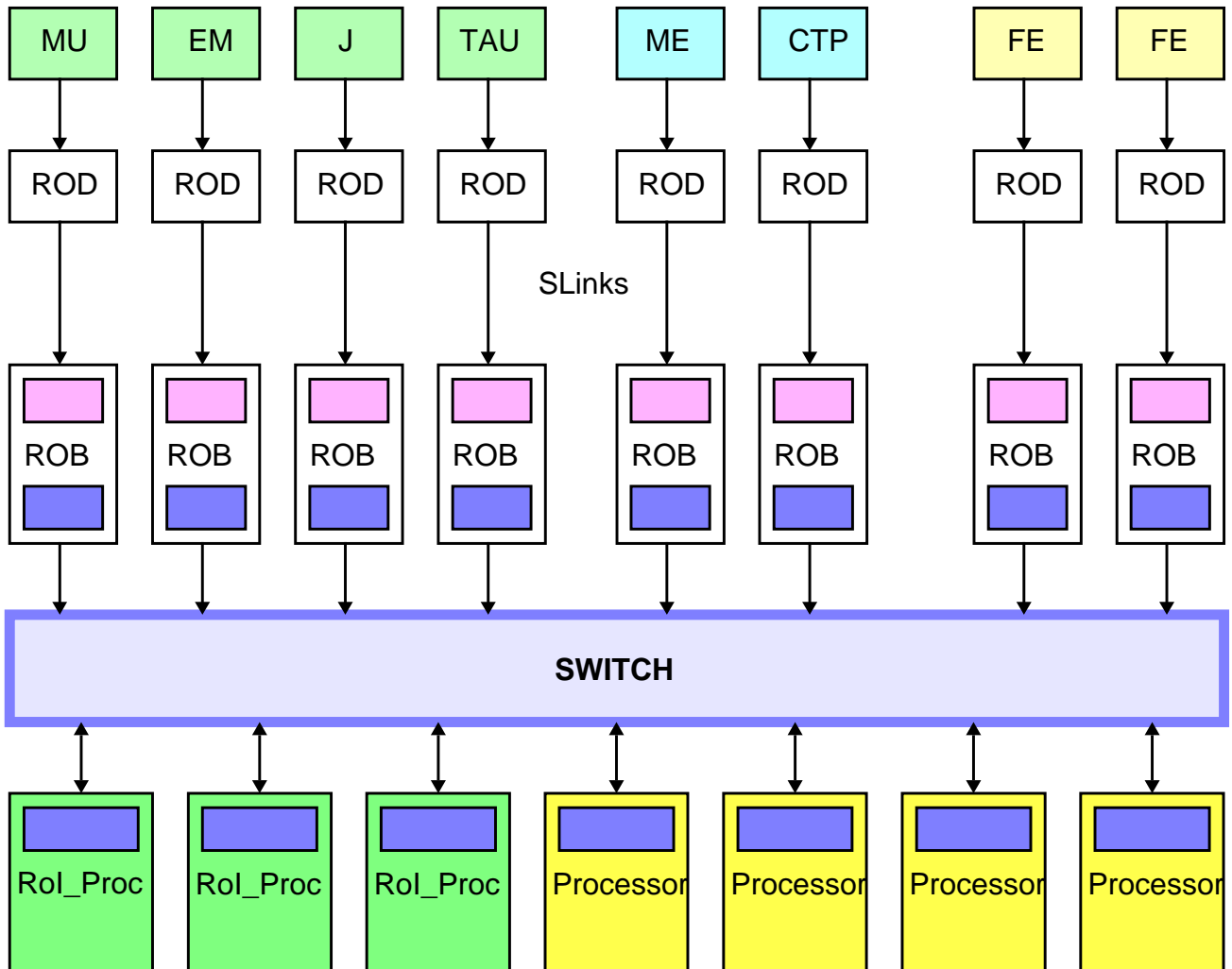
**LVL1 data sending**  
**Processor allocation (RoIRSF)**  
**Data request**  
**Data delivery**  
**Processor status (COutR)**  
**Decision broadcast (T2DR)**

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## The Level-2 Supervisor for the Demo-C

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### Common SWITCH?



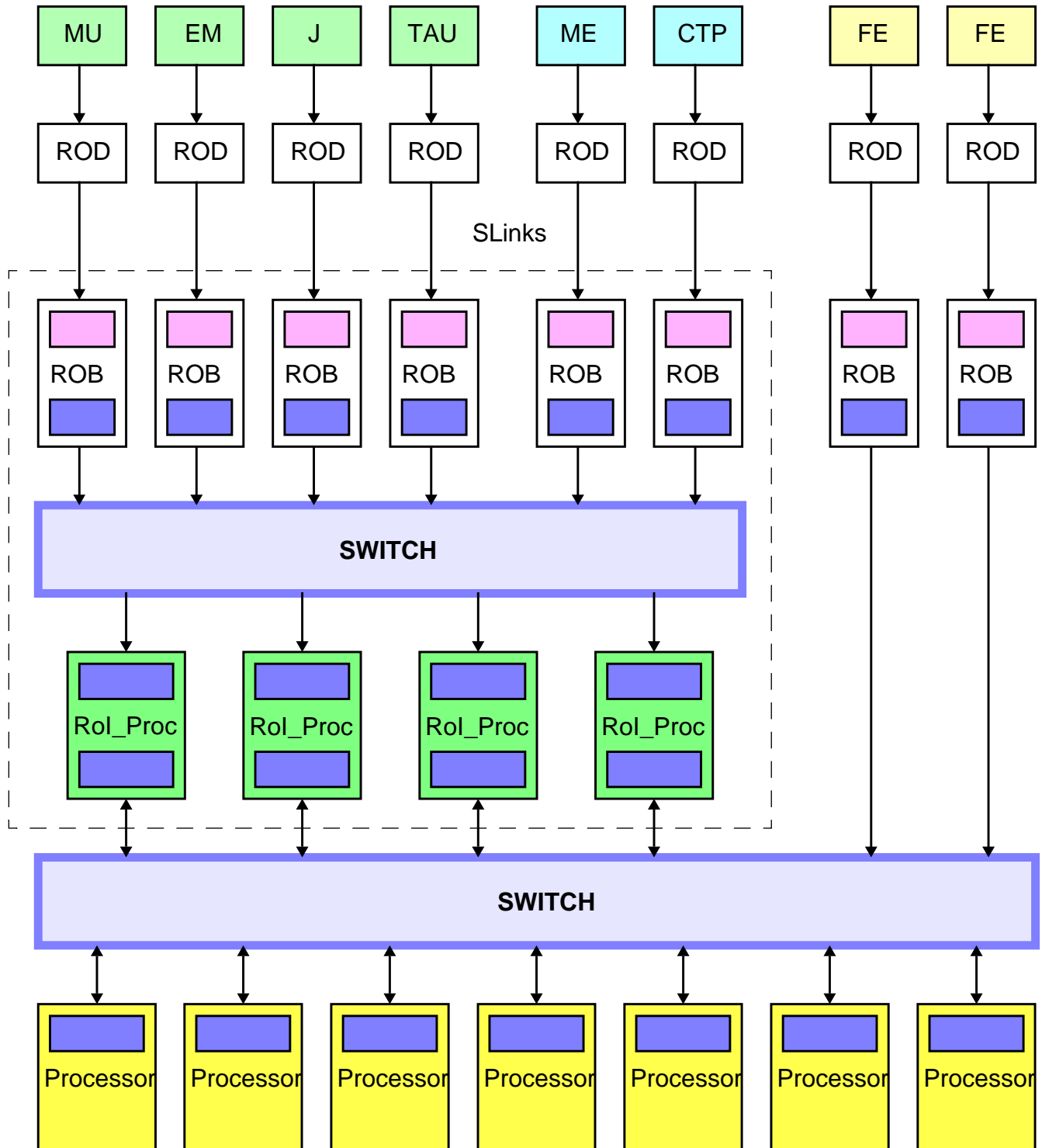
- Homogenous structure
- LVL1 data in ROBs - flexibility in Rol processing
- Merging LVL1 events to avoid 100kHz transfer from ROB
- Scalable, no “hot spot” or bottlenecks
- Changeability Rol\_Proc  $\Leftrightarrow$  Processor (software)
  
- Added traffic to the SWITCH
- Added latency

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# The Level-2 Supervisor for the Demo-C

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## STEWARD processor: a bottleneck? (2)

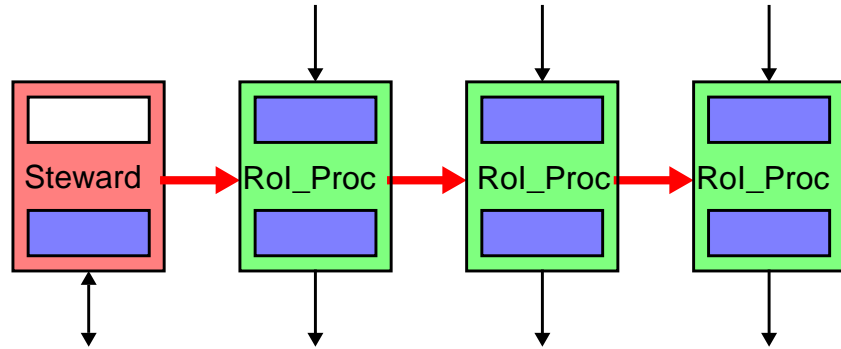


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# The Level-2 Supervisor for the Demo-C

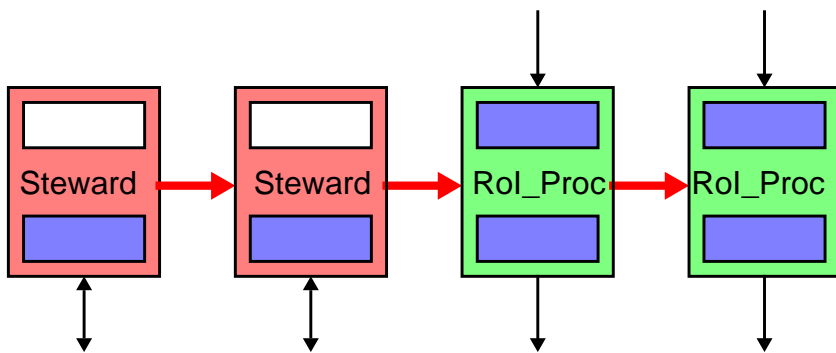
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## STEWARD processor: a bottleneck? (1)



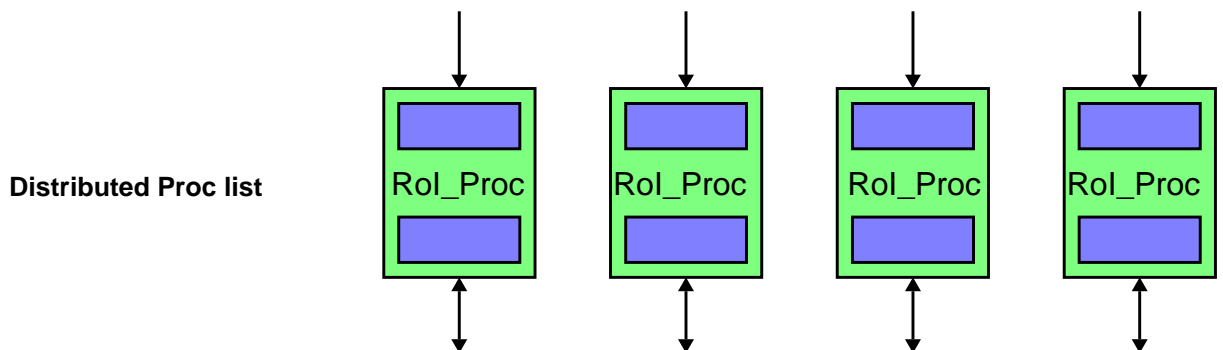
Maintain list of Proc  
Receive Proc decision  
Broadcast decision to ROBs

Distributed STEWARD processors:



Distributed Proc list  
(allocated for STEWARD-RoI\_Proc?)

Distributed Steward functions:  
(each RoI\_Proc performs STEWARD functions)

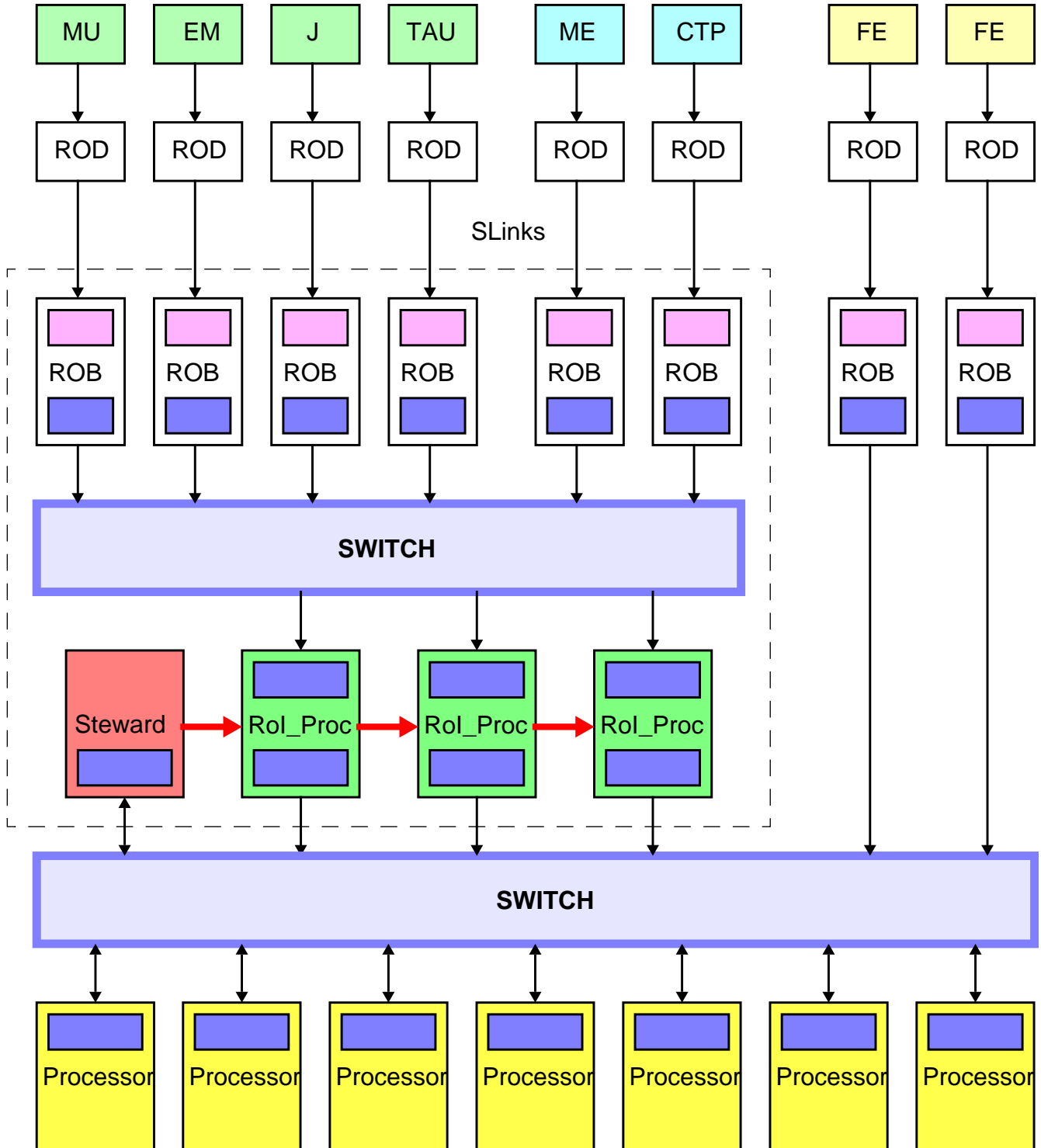


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# The Level-2 Supervisor for the Demo-C

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## LVL1 Data input to the Supervisor (2)

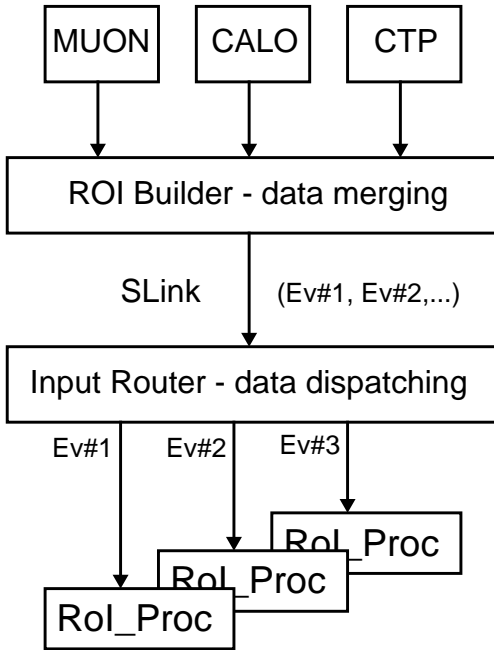


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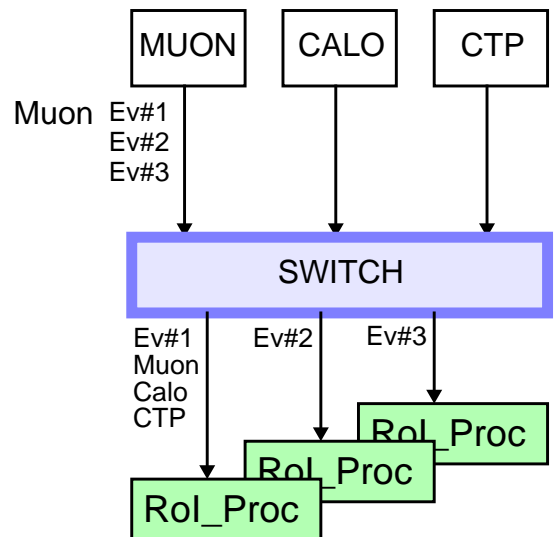
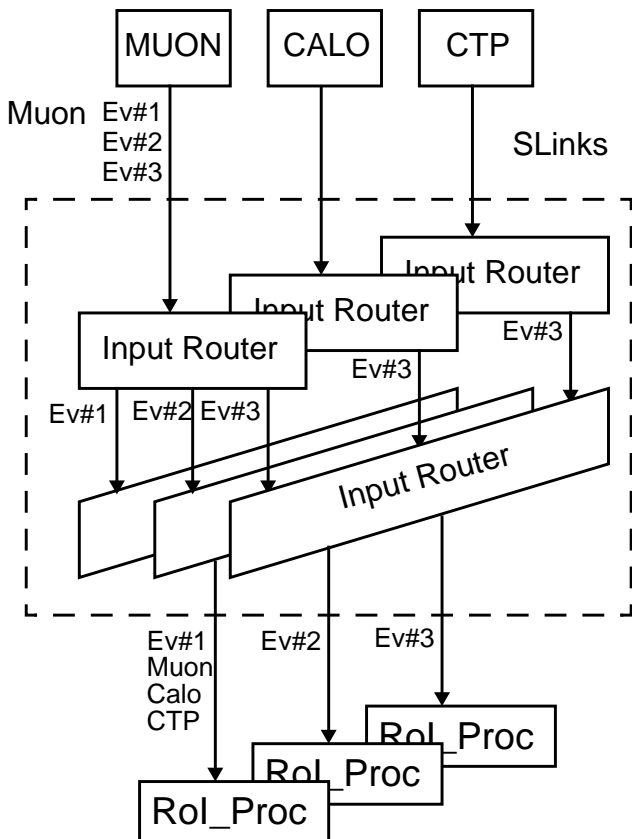
# The Level-2 Supervisor for the Demo-C

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## LVL1 Data input to the Supervisor



- Moun, Calo and CTP prepare LVL1 data
- Rol Builder merge LVL1 data in one message
- LVL1 data are sent via SLink (by ROD?)  
SLink - "hot spot"
- Input Router dispatch the LVL1 data (Ev#1, Ev#2, ...)

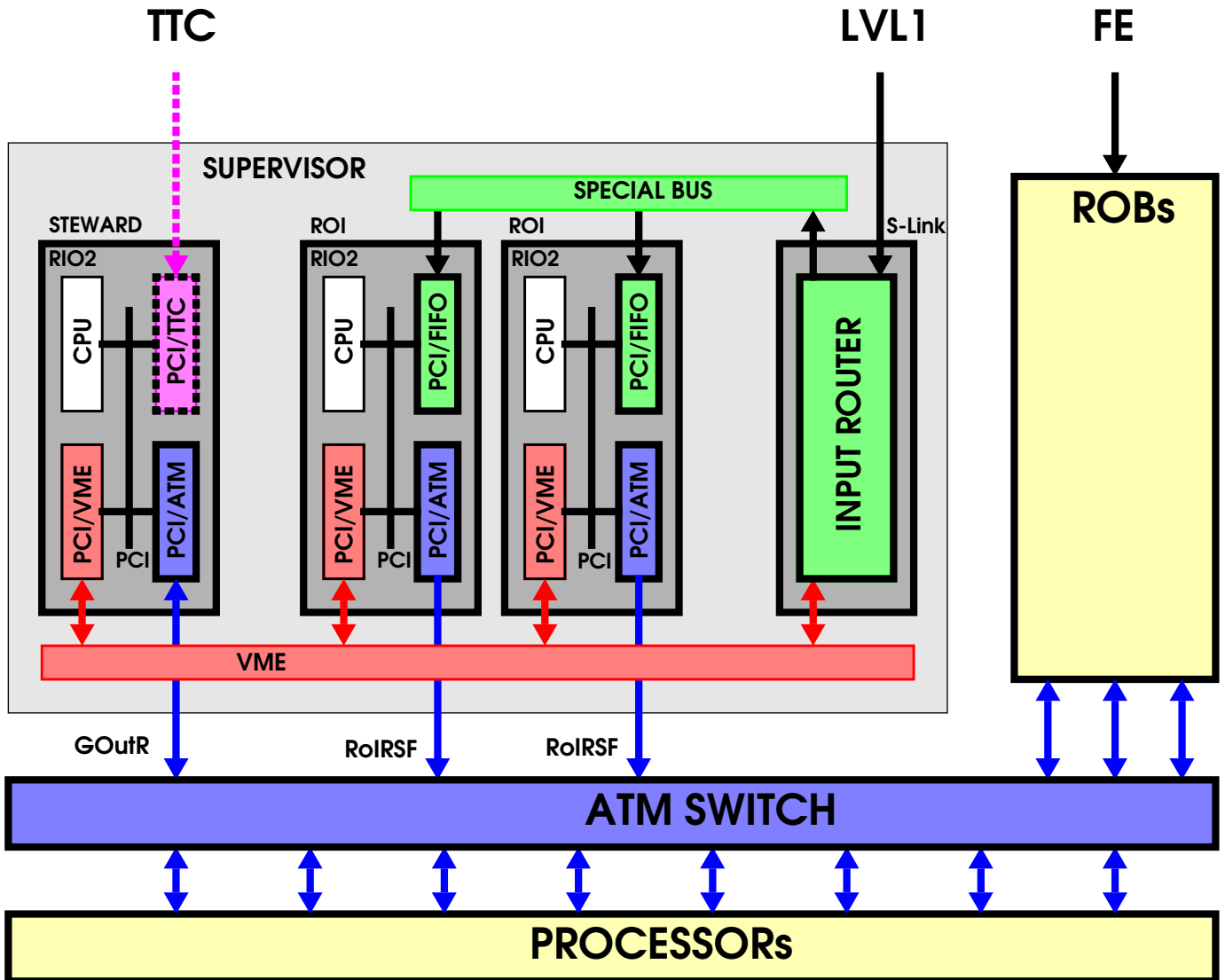


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# The Level-2 Supervisor for the Demo-C

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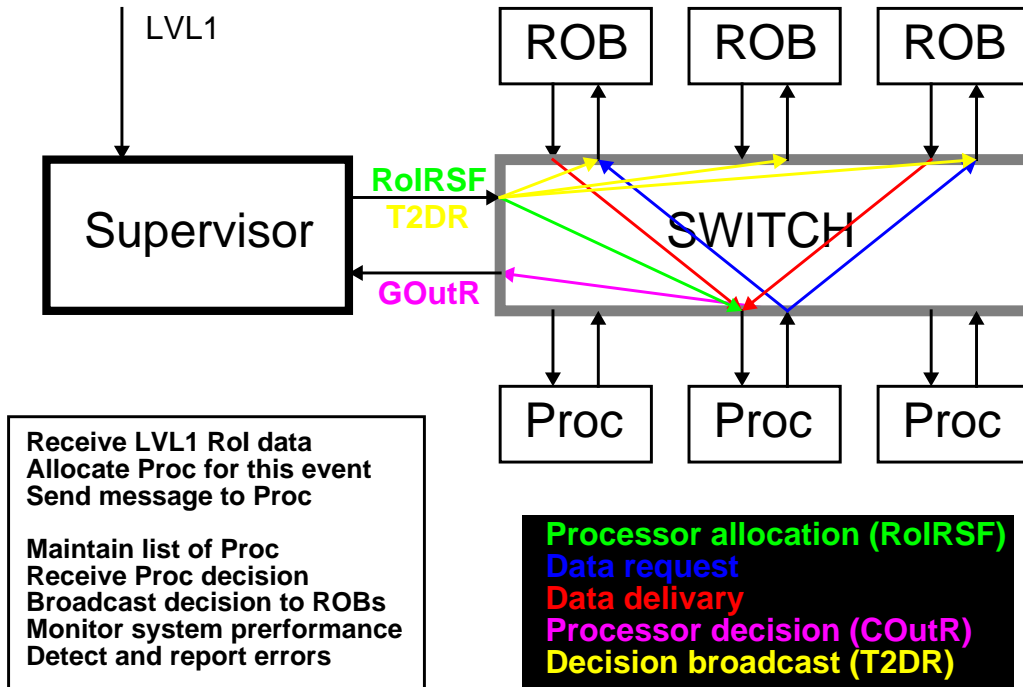
## Demonstrator for the architecture "C"





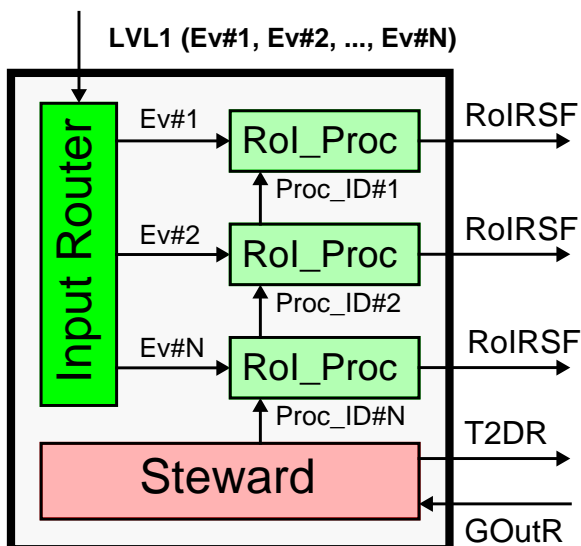
# The Level-2 Supervisor for the Demo-C

## Level-2 trigger system (Architecture C)



## Level-2 Supervisor: Conceptual design (Demo-C subset)

(<http://sgj3.hep.anl.gov:8001/l2concep.html>)



### GUIDELINES:

- Commercial Hardware (RIO2, PCI)
- Event Parallel Operations - RoI\_Proc
- "Hot spots":
  - Single input (SLink)
  - Input Router
  - Steward
- Possible bottlenecks:
  - Steward
  - Steward - RoI\_Proc path (VMEbus)