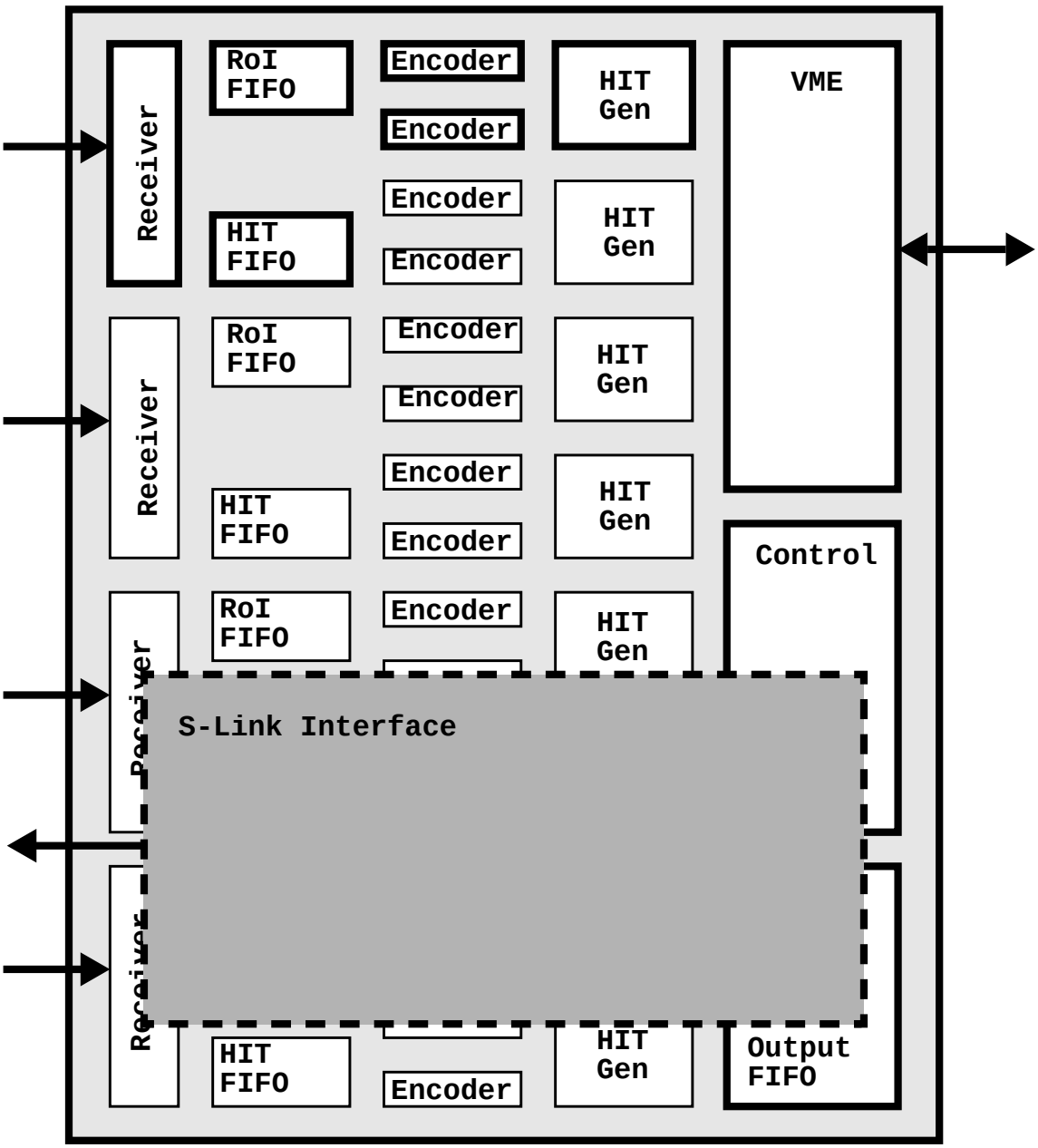
LVL1 e/γ RoI Builder Prototype

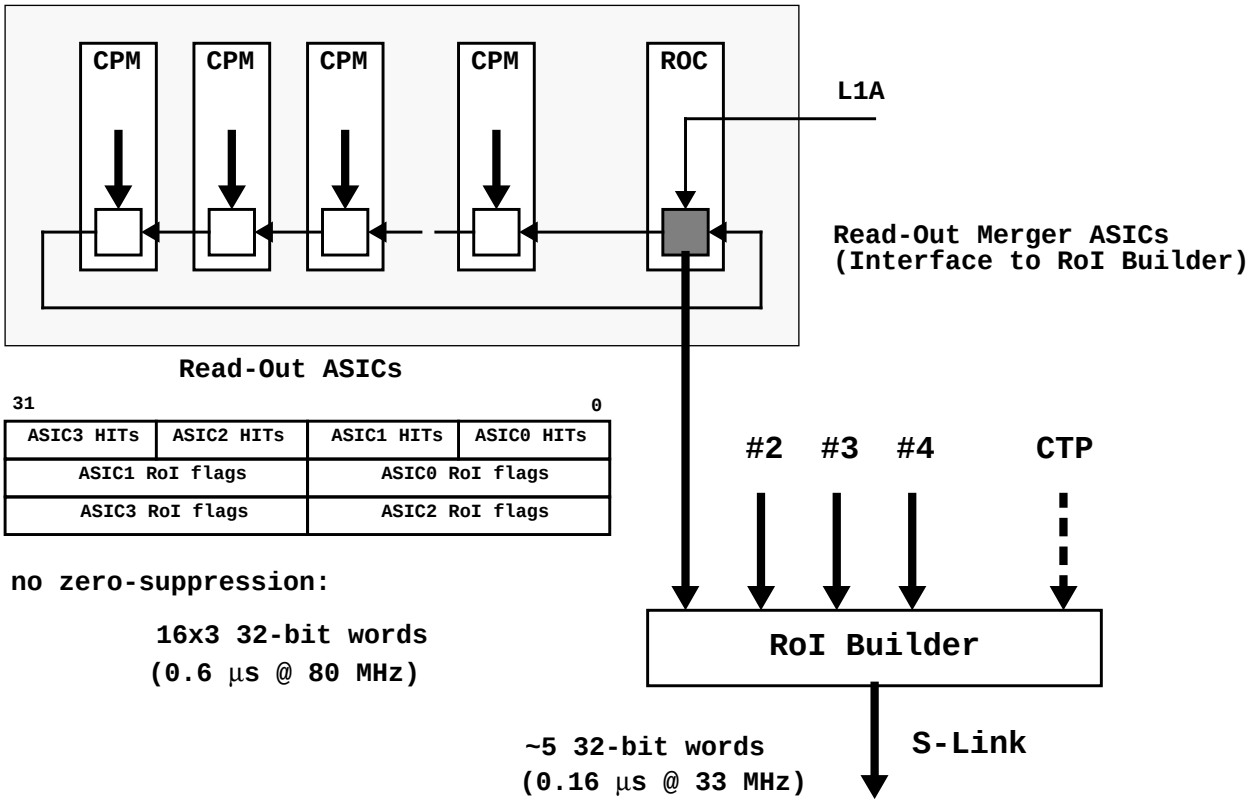
RoI / HITs matching and zero suppression



- **LVL1 / Supervisor RoI Builder discussion**
- **Verilog/VHDL model**
- **Check with existing data sets**

LVL1 e/γ RoI Data Collection

Cluster processor crate #1

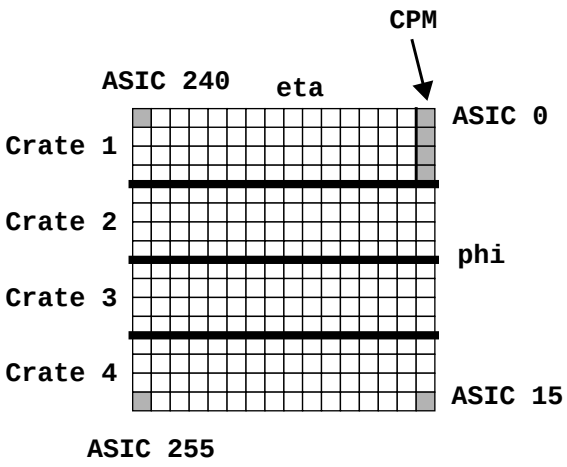


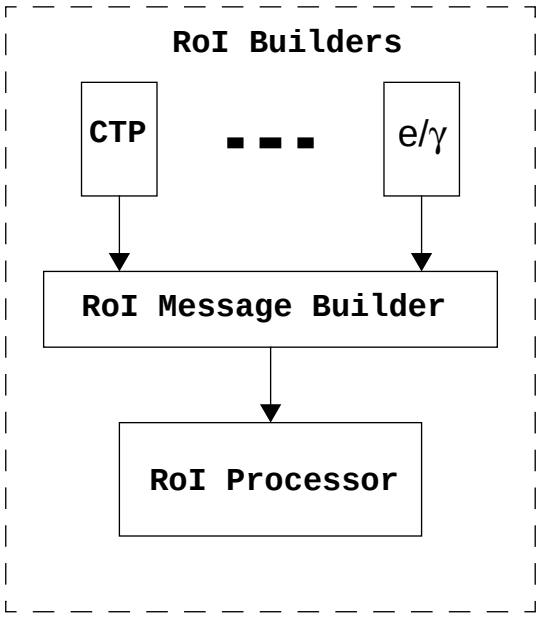
no zero-suppression:

16x3 32-bit words
(0.6 μs @ 80 MHz)

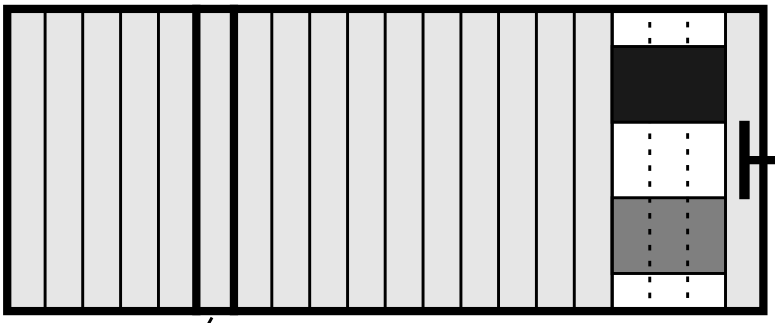
~5 32-bit words
(0.16 μs @ 33 MHz)

Crate/CPM/ASIC numbering (possible)





LVL1 e/γ Trigger Crate Layout (RoI Data)

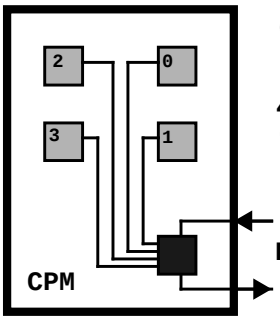


4 Cluster processor crates

RoI Data

Interface to RoI Builder

16 CP modules (CPMs) per crate



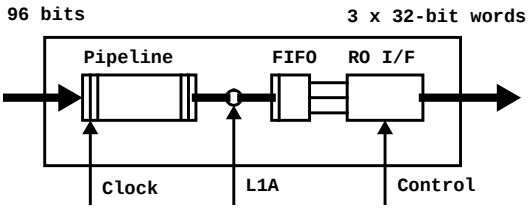
Cluster processor module (CPM, 64 in total)

4 CP ASICs
(256 in total)

4 x 8 Trigger HITs (1 32-bit word)
4 x 16-bit RoI flags (2 32-bit words)

Read-Out ASIC

Read-Out ASIC (no zero-suppression, fixed number of words)



31 24	23 16	15 8	7 0
ASIC3 HITs	ASIC2 HITs	ASIC1 HITs	ASIC0 HITs
ASIC1 RoI flags		ASIC0 RoI flags	
ASIC3 RoI flags		ASIC2 RoI flags	

(zero-suppression, variable number of words)

Possible format:

bit 31 - 0 - Trigger HIT
1 - RoI flags

31	30 16	15 8	7 0
0		ASIC HITs	ASIC Address
0		ASIC HITs	ASIC Address
1	RoI Address 2		RoI Address 1
1	RoI Address 4		RoI Address 3

11 0

Primary / Secondary RoI Algorithm

Input: 1 (12+8)-bit list (RoI coordinates + Trigger HITs)

CTP decision word after mask and prescaler

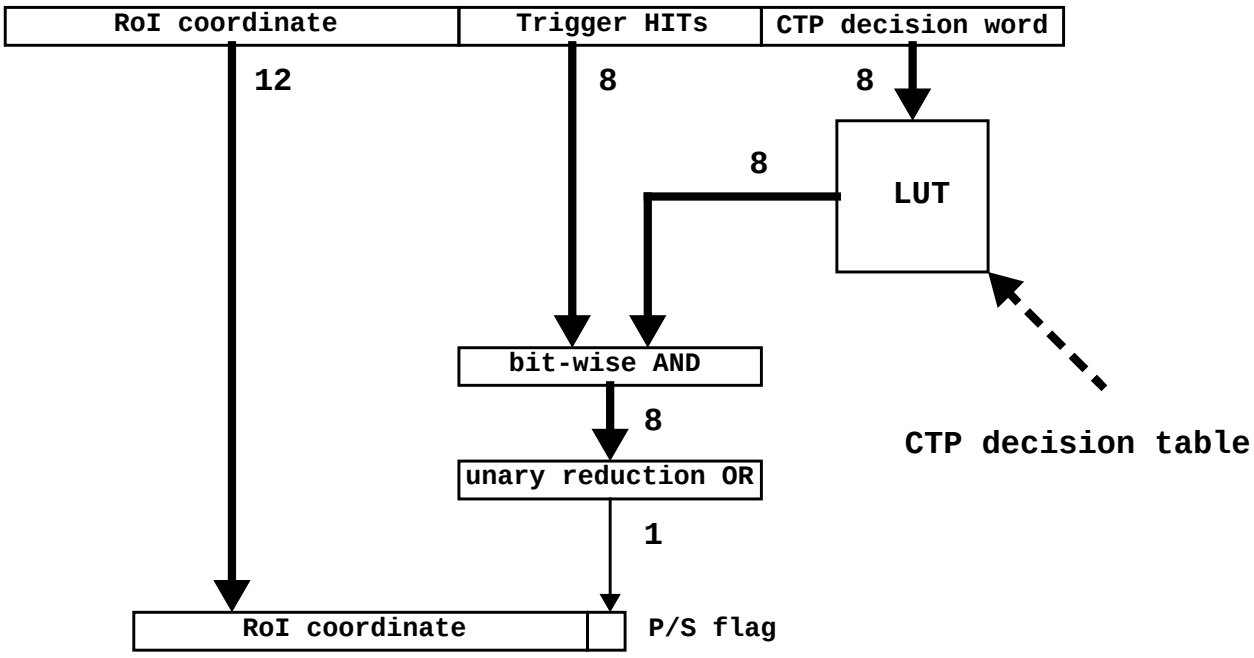
CTP decision table (thresholds and multiplicity) | **LUT**

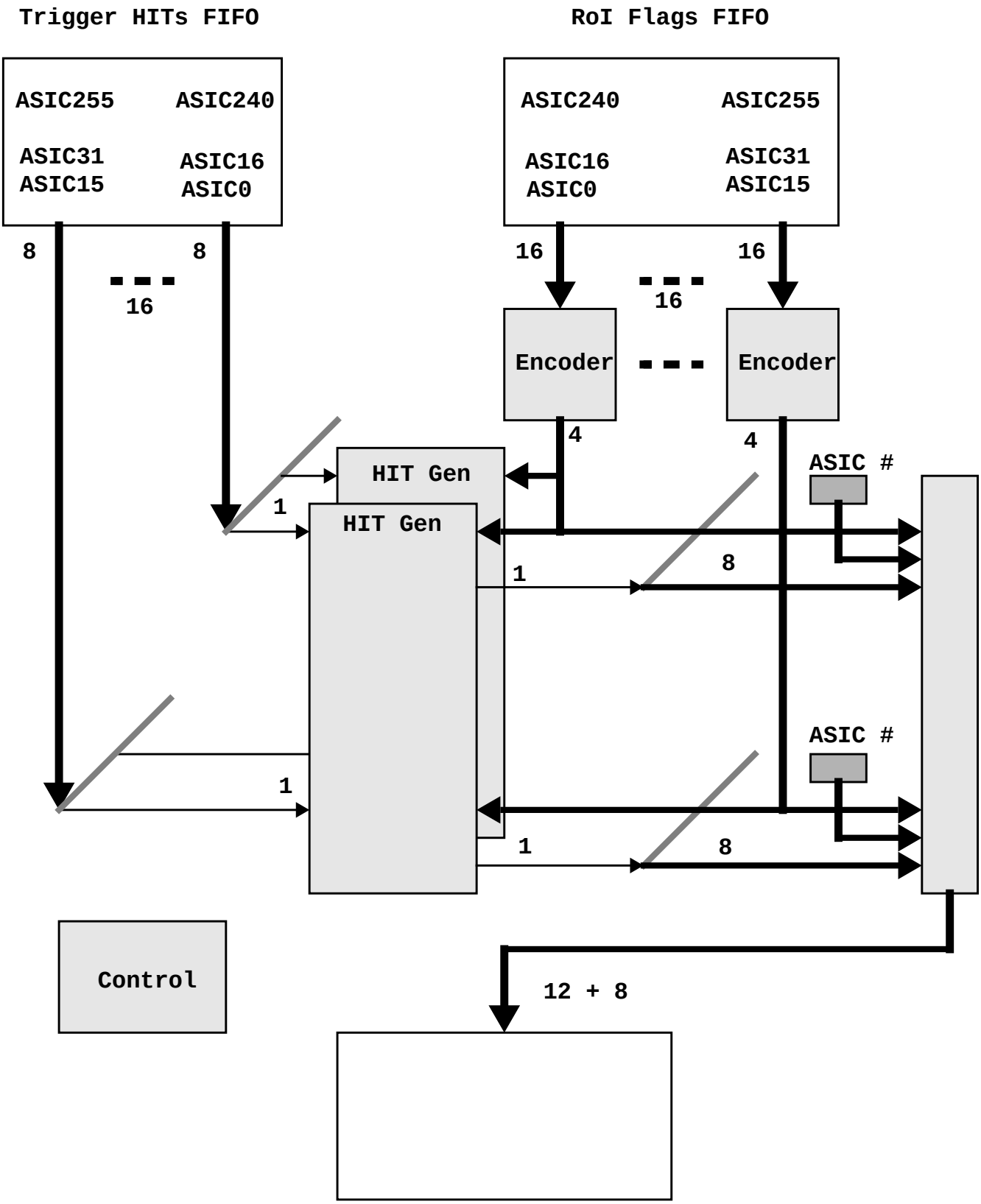
Output: 1 (12+1)-bit list (RoI coordinates + P/S flag)

Algorithm:

```
For each RoI
  For each Trigger HIT
    if LUT is “1”
      P/S flag = “1” /* Primary RoI */
```

Possible implementation:





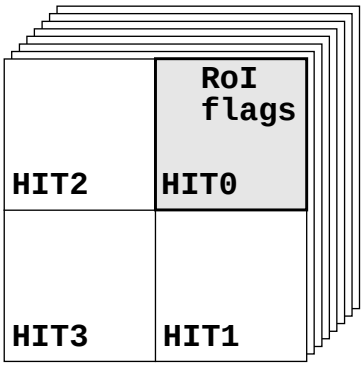
RoI coordinates + Trigger HITs FIFO

Trigger hits / RoI flags matching Algorithm

Input: 8 16x16 1-bit maps (Trigger HITs)
or 8 8-bit lists (Trigger HITs coordinates)
1 64x64 1-bit map (RoI flags)
or 1 12-bit list (RoI flags coordinates)

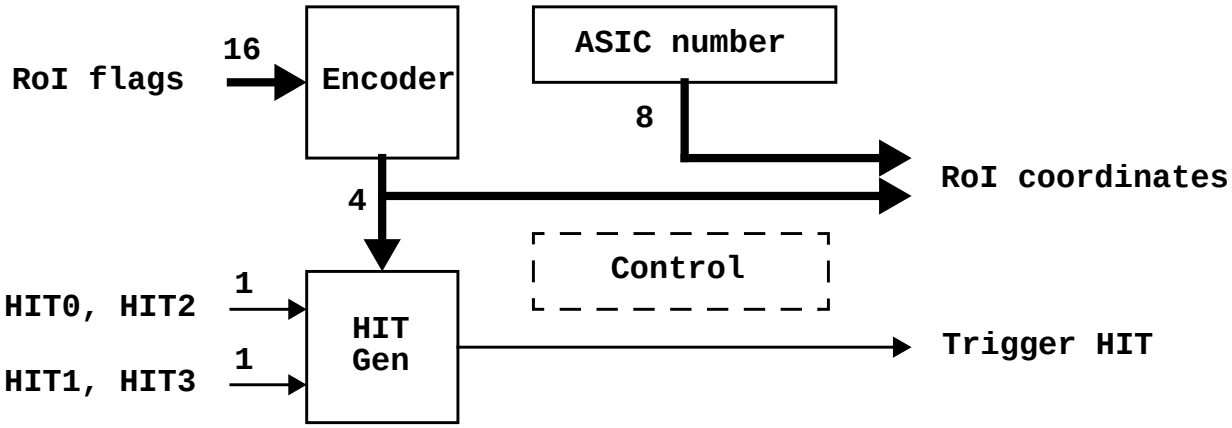
Output: 1 (12+8)-bit list (RoI coordinates + Trigger HITs)

Algorithm:




```
For each HIT-map
  For each 2x2 HITs window
    For each RoI flag
      if RoI flag within top-right 3x3
        HIT = HIT0
      else if RoI flag at the bottom edge
        HIT = HIT0 OR HIT1
      else if RoI flag at the left edge
        HIT = HIT0 OR HIT2
      else (ROI flag in the corner)
        HIT = HIT0 OR HIT1 OR HIT2 OR HIT3
```

Possible implementation:

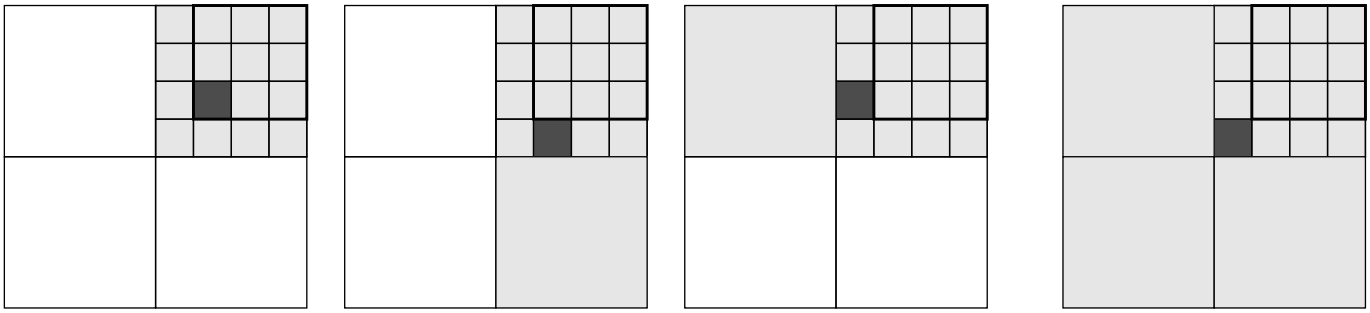


Possible parallelism:

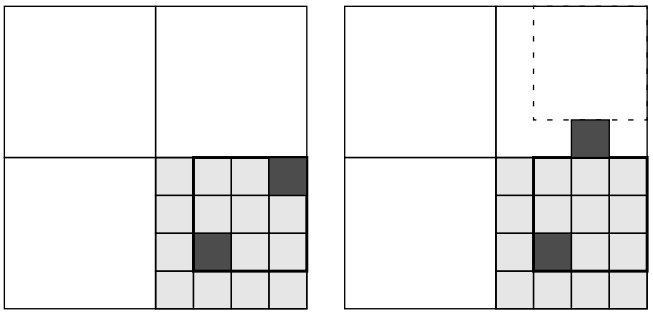
- HIT-maps
  8 Trigger HIT maps
- 2x2 HIT windows (or 16 RoI flags)
  16 2x2 HIT windows (circle in phi)

LVL1 e/γ Trigger hits / RoI flags matching

Single RoI flag - unique RoI flag - Trigger HITs assignment



Multiple RoI flags - ambiguous RoI flag - Trigger HITs assignment



RoI flag (0.1 x 0.1)

Trigger HIT (0.4 x 0.4)

=> Assign to each RoI flag all Trigger HITs

All "primary" RoI are flagged as "primary"
"Secondary" RoI may be flagged as "primary" (a few percent)

Primary / Secondary RoI classification

LVL1 Trigger Menu at L= 10^{33} (example)

LVL1	MU6
LVL1	EM80
LVL1	EM20I
LVL1	EM15I + EM15I
LVL1	TAU80
LVL1	J100
LVL1	J50 + J50 + J50
LVL1	ME100

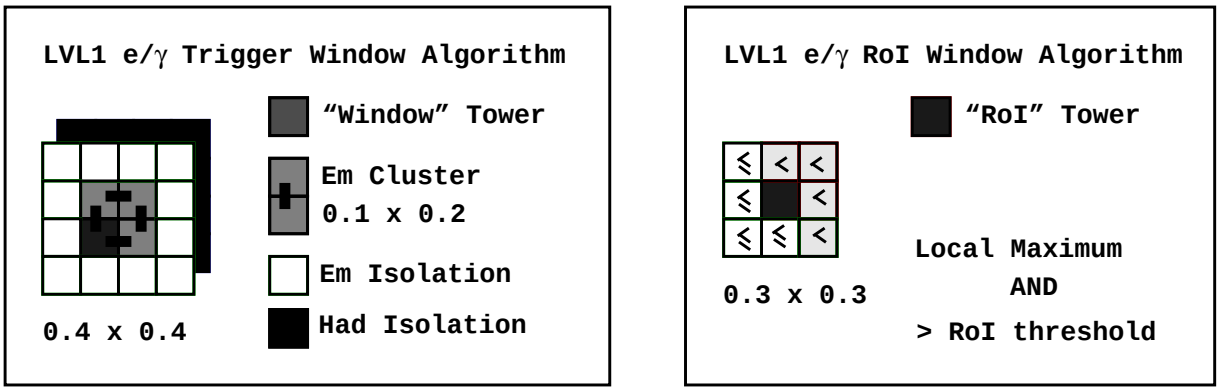
CTP information

- decision table (thresholds and multiplicity)

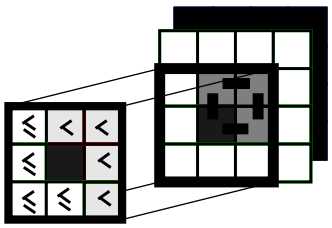
- decision (after mask and prescaler)

=> Primary/Secondary flag to RoI

LVL1 e/γ Trigger and RoI Generation



Trigger/RoI Window Coexistence

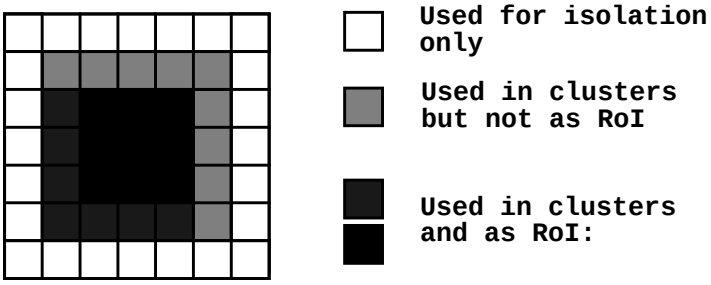


Trigger and RoI Generation Within Cluster Processor (CP) ASICs

CP ASIC processes 16 overlapping Trigger/RoI windows
Inputs from a 7x7 trigger tower region

8 sets of thresholds: cluster, em isolation, had isolation

Output: 8 Trigger HITs (one HIT per threshold's set, 16 windows logical OR)
(4 x 4) 1 bit RoI flag's map

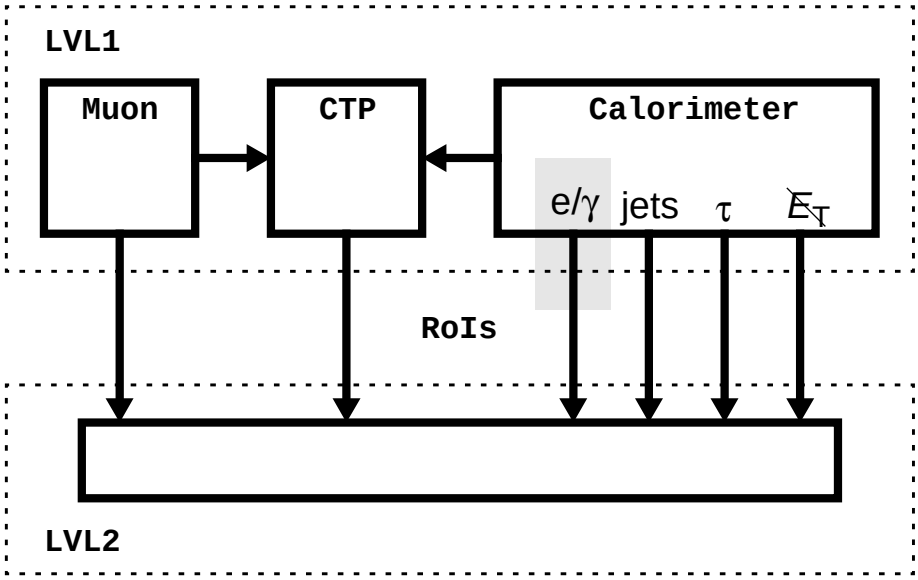


A single shower may produce Trigger HIT and ROI flag in different ASICs

Complete system (4096 towers, 256 ASICs):

256 8-bit Trigger HITs (8 16x16 1-bit maps / 1 16x16 8-bit map)
4096 1-bit RoI flags (1 64x64 1-bit map)

LVL1/LVL2 Interface



6 sources:

- **Central Trigger Processor (CTP)**
- **Muon trigger to CTP interface**
- **Electron/photon trigger** ←
- **Jets trigger**
- **Hadron trigger**
- **Missing E_T trigger**

LVL1 provides RoI information to the LVL2

Primary RoIs - contributed to the LVL1 decision
Secondary RoIs - did not contribute

Ref.: ATLAS note DAQ-No-073 (A. Watson)