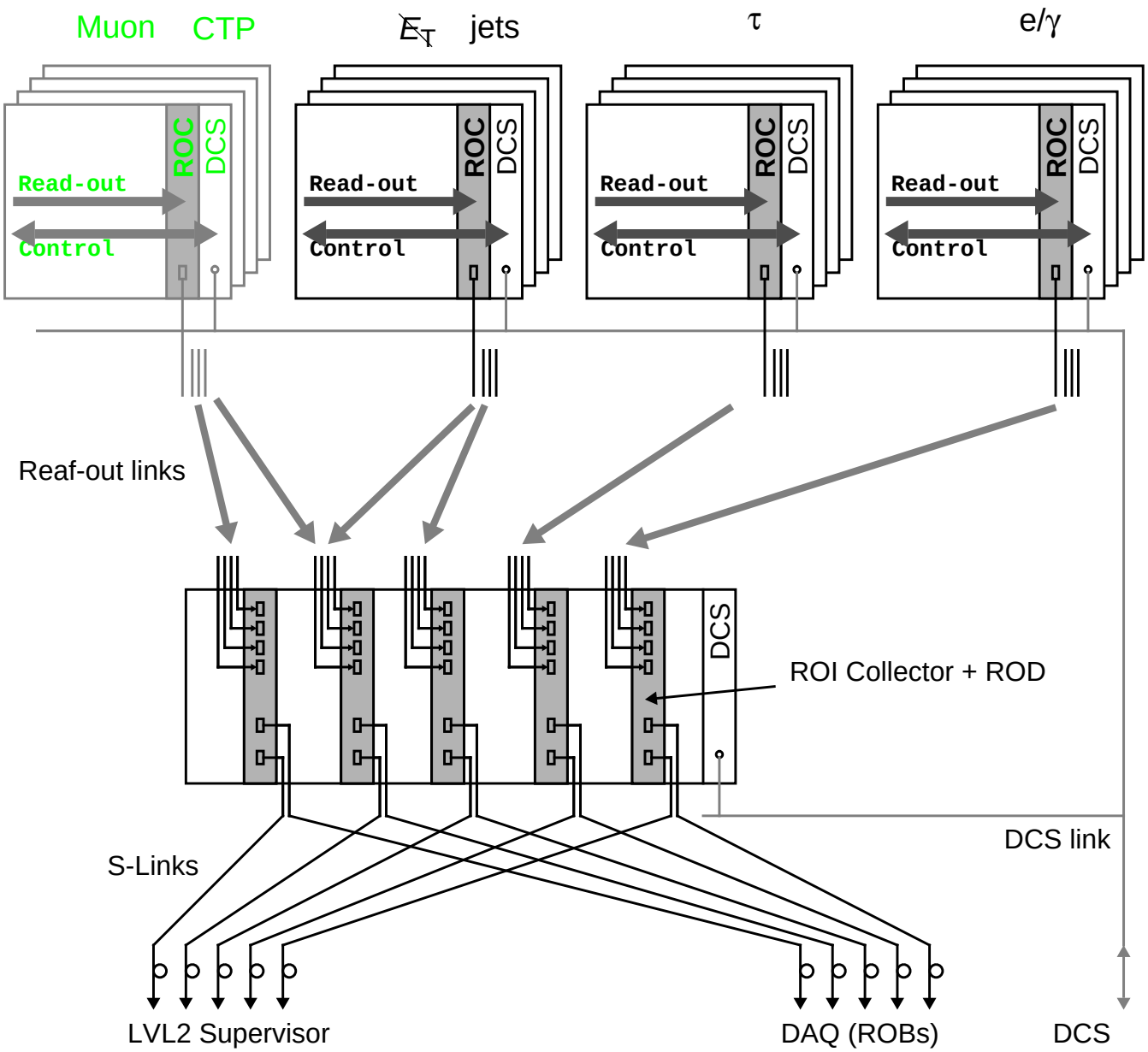
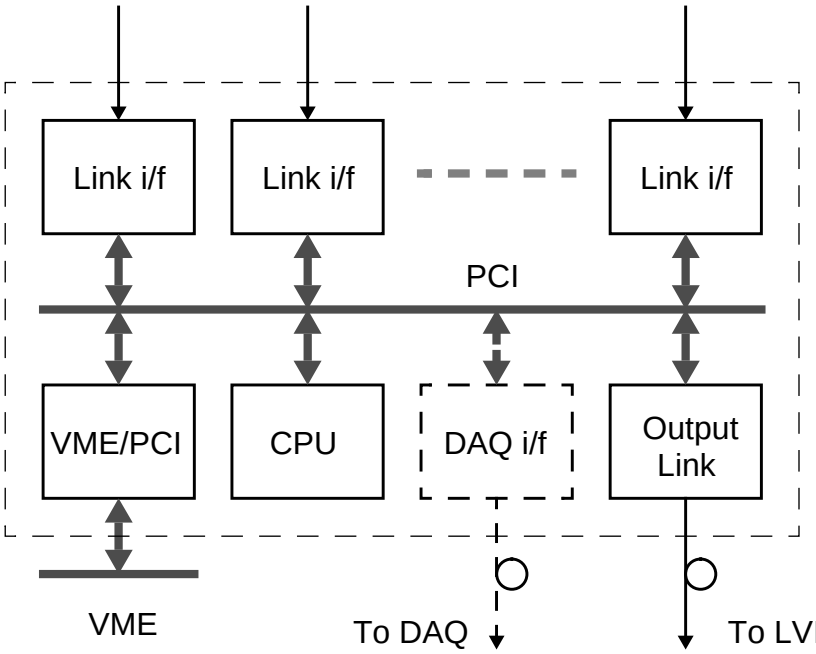
# LVL1 ROI/DAQ Read-out




- Common DAQ/ROI/DCS infrastructure
  - Crates, Read-out bus, Control bus (VME?), data links
  - ROC and DCS modules
  - ROI Collector + ROD
- Alternatively separate ROI and DAQ paths
- Look at other subsystems (subdetectors)

# RoI Collector Implementation




- Similar to ROC ?
- Link i/f - common with LVL1
- Output - optical S-Link
- Board - commercial / custom
- Commercial CPU card / commercial CPU mezzanine
- Mezzanine form-factors

- DAQ interface ?
- Common with Muon/CTP ?
- Data volume

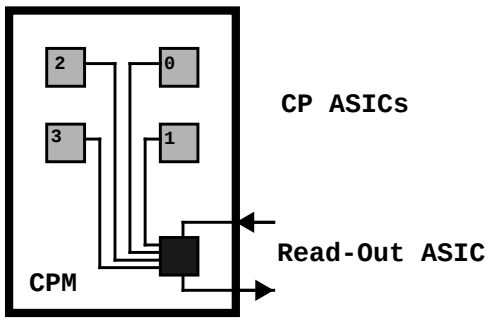
## LVL1 Data Volume

| e/γ | τ | jets | $\not{E}_T$ | CTP | Muon |
|---|---|---|---|---|---|
| 10*32 bits (10 RoIs) | 10*32 bits (10 RoIs) | 10*32 bits (10 RoIs) | 3*32 bits (const) | 7*32 bits (const) | 16*32 bits (max) |

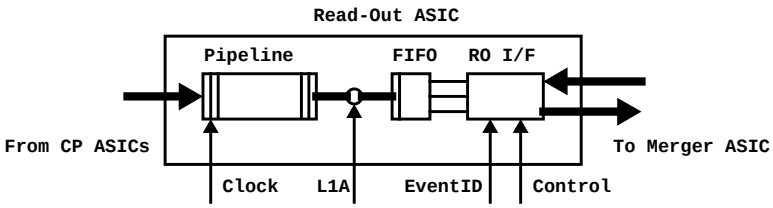
+ ~6*32 bits - message formatting & L1ID + BCID

# LVL1 e/γ RoI Data Collection

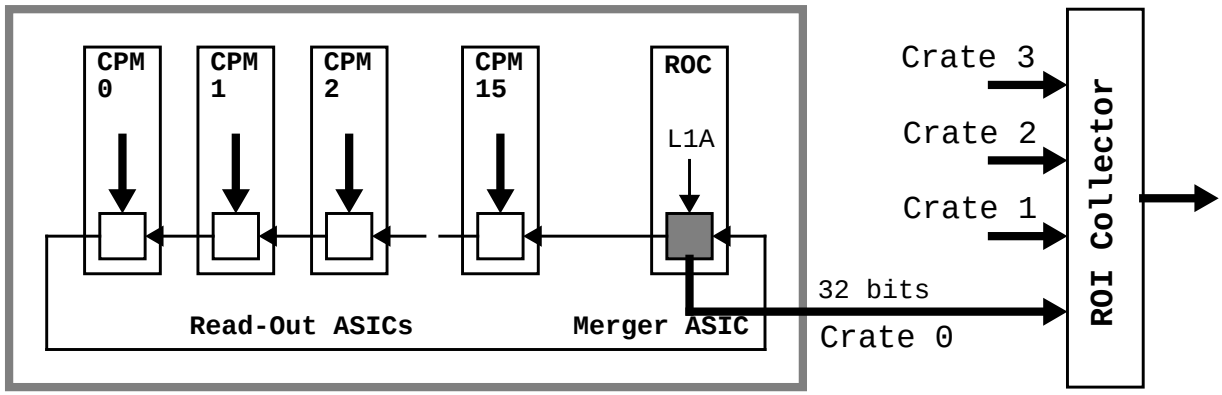
**Cluster processor module**




**Read-Out ASIC**




**Cluster processor crate (RoI read-out path)**




- ROI information read-out organisation inside the CP crate
  - ROI data path - common/separate with DAQ
- Read-out controller (DAQ/ROI read-out)
  - Contact-person
  - Participation in design?
- Link to ROI Collector (same as DAQ?)
  - Physical implementation
  - Data format
- ROI Collector
  - Implementation (same as LVL1- 9U VME)
  - Single/multiple ROI collector(s) for calorimeter trigger
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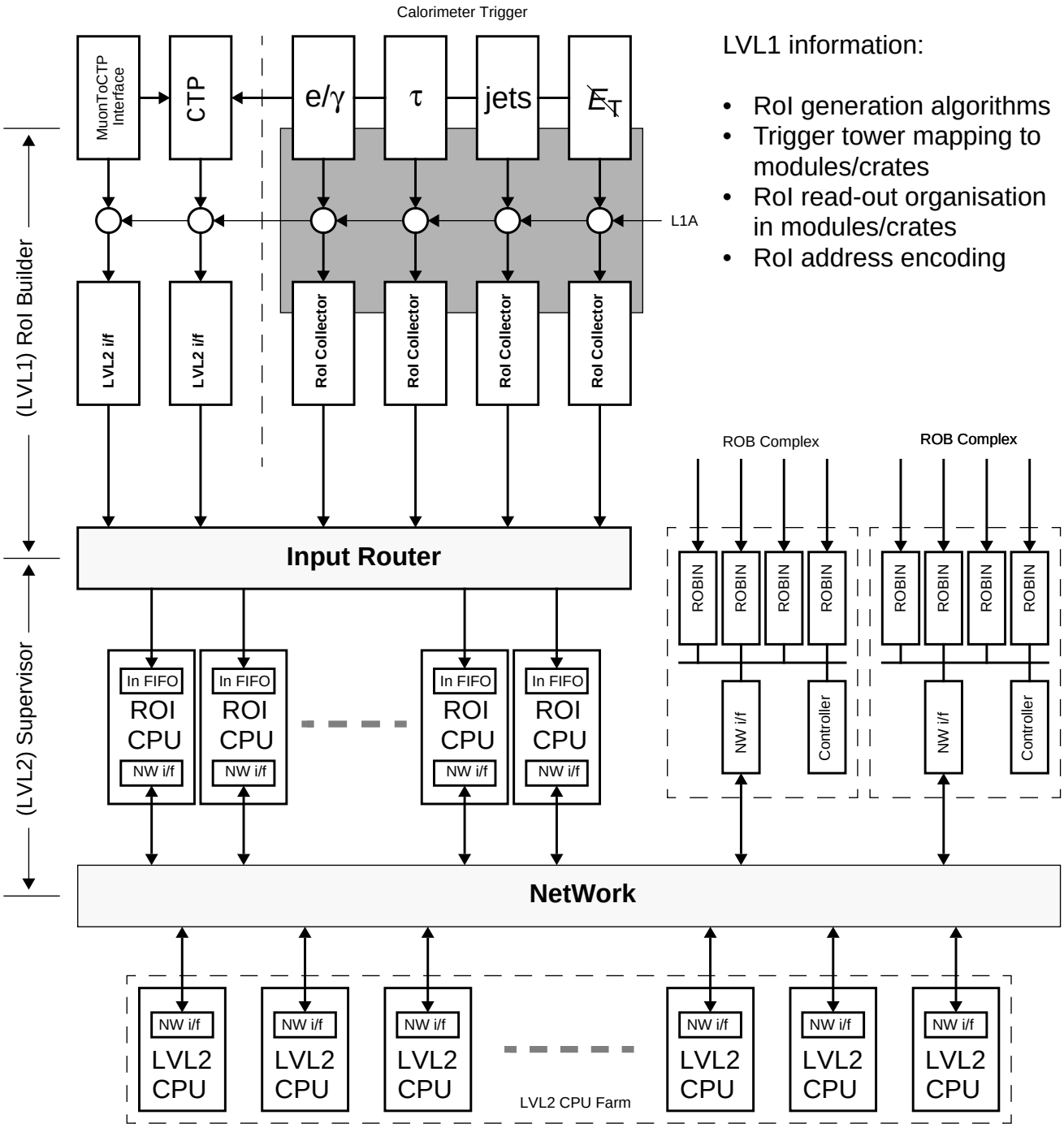
# LVL1/LVL2 Interface
# (LVL1) RoI Builder / (LVL2) Supervisor

## General Layout




LVL1 information:

- RoI generation algorithms
- Trigger tower mapping to modules/crates
- RoI read-out organisation in modules/crates
- RoI address encoding