Supervisor for Demonstrators

Supervisor tasks in the LVL2 system:

- Receive ROI fragments from the level-1, assign free level-2 processor(s) for this event and send ROI record to the ROB’s (ROIR) or to the selected processor (ROIRSF).
- Receive the level-2 decision (GOUTR), update statistics and communicate the blocked results to the ROB’s (T2DR).

“Local Global”/“Push”/“Parallel” (DemoB)  “Single Farm”/“Pull”/“Sequential” (DemoC)

Supervisor tasks in demonstrator program:

- To support DemoB and DemoC programs
- An interface from an emulated source of LVL1 data to a LVL2 vertical slice
- Custom hardware for the LVL1 interface
- Commercial processors for the for the LVL2 interface
- To demonstrate Supervisor scalability
Supervisor components

**Demo B**
- LVL1 emulator
- Input Router
- Router Bus
- Arbiter
- FIFO PMC
- RoI Processor
- Output Router
- Network server

**Demo C**
- LVL1 emulator
- Input Router
- Router Bus
- Arbiter
- FIFO PMC
- RoI Processor

Decision from Global processors

Network server

Supervisor

Supervisor

LVL1 emulator

Input Router

Router Bus

Arbiter

FIFO PMC

RoI Processor

Output Router

to ATM switch

Demo C

-Level 1 Emulator
-Input Router
-Router Bus
-Arbitrator
-FIFO PMC
-RoI Processor

Router Bus

Level 1 Emulator

Arbiter

Input Router

Level 1 Emulator

Arbiter

Input Router
Custom Hardware Performance (1)

CPU - PMC FIFO bandwidth:

![Graph showing CPU PMC FIFO bandwidth](image)

- Write: 42 Mbytes/s
- Read: 58 Mbytes/s

Router Bus: 32-Bit bus, 200 Mbytes/s raw bandwidth (50 MHz clock)

SLink to SLink:

![Graph showing SLink to SLink performance](image)

- 57 Mbytes/s
Custom Hardware Performance (2)

LVL1 Emulator - Input Router - Router Bus - FIFO PMC - CPU:

![Diagram of LVL1 Emulator - Input Router - Router Bus - FIFO PMC - CPU]

Time in Input Router

- 20 Mbytes/s

Time in Output router

- 14 Mbytes/s

CPU - FIFO PMC - Output Router - Router Bus - SLink PMC - CPU:

![Diagram of CPU - FIFO PMC - Output Router - Router Bus - SLink PMC - CPU]
Processors

General:
• PowerPC board (CES 8061) running LynxOS 2.4
• 100 and 66 MHz processors
• Two PCI PMC slots

LVL1 Emulator:
• Demonstrate the operation of the Input Router
• CERN simple PCI to S-Link interface card
• RoI fragments in a file (6 per event, different types)

Network Server (Demo B):
• Provides link between LVL2 network and RoI processor using VME bus (shared memory with a semaphore)
• Supports DS-Link, SCI (two modes)

RoI Processor:
• PCI interface to Input and Output Routers
• VMEbus memory mapped to Network Server (Demo B)
• Scalable to as many processors as router supports
### Software Organization and Measurements (1)

**Demonstrator B:**

**Network independent part (Supervisor):**
- Read/emulate LVL1 input
- Poll for Global decision (semaphore from Network Server)
- Process Global decision, if ready
- Build RoI record from RoI fragments
- Send RoI Record to RoI distributor
- Send T2 decision group record, if ready

**Network dependent part (Network Server):**
- Allocate buffer for network interface card (NIC)
- Probe/read NIC
- Forward event ID, decision and processor tags to supervisor via VMEbus (mapped shared memory)
- free buffer
- Several version of network software

**Operation:**
- Controlled variables - Nevents, Nglobals, Nevents/queue
- Monitored variables - NRoIR, NGOutR, NTimeOut, EventRate...
- Histograms - latency, events queued in LVL2

<table>
<thead>
<tr>
<th>Task</th>
<th>Percentage Time</th>
</tr>
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<tbody>
<tr>
<td>Read/RoI fragments</td>
<td>8 sec</td>
</tr>
<tr>
<td>Build RoI record</td>
<td>2 sec</td>
</tr>
<tr>
<td>Send RoI record</td>
<td>0 sec</td>
</tr>
<tr>
<td>Process T2 decision group record</td>
<td>3 sec</td>
</tr>
<tr>
<td>Forward event ID, decision and processor</td>
<td></td>
</tr>
<tr>
<td>tags to supervisor via VMEbus (mapped</td>
<td></td>
</tr>
<tr>
<td>shared memory)</td>
<td></td>
</tr>
</tbody>
</table>

![Graphs showing decision latency and events in LVL2](image-url)
Software Organization and Measurements (2)

Demonstrator C:
- Software was adapted to operate within the common framework
- Unified run control system

Common framework tasks:
- Initializing the ATM device
- Managing a table of node addresses on logical name
- Setting process priority

Supervisor tasks:
- Read and pack RoI fragments until a complete event is received
- Form a RoI record, select a destination and record a time stamp
- Transmit to destination on the ATM network
- Poll the NIC for received messages, latency calculation
- Processor returned to a pool, decision record sent

Operation:
- Controlled variables - Nevents, NRoi/event, Ndestinations
- Histograms - decision latency
Conclusions

- Supervisor for the LVL2 demonstrator programmm has been implemented which supports vertical slices of architecture B and C
- An interface between LVL1 emulator and LVL2 is provided
- Three different types of LVL2 network technologies were tested (DS-Link, SCi and ATM)
- LVL2 processing load has been balanced
- LVL2 decision latency measurements is provided
- Rates of up to 25 kHz (single RoI) have been obtained
- The model of the supervisor is scalable by adding additional commercial CPUs