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L1 Calo Firmware Overview:
Languages, Tools, Methods

- Beginners Guide to…
  - Languages
  - The Design Flow & Associated Tools
  - Version Management
- Breakdown of Languages, Tools & Methods by Institute
- Conclusions

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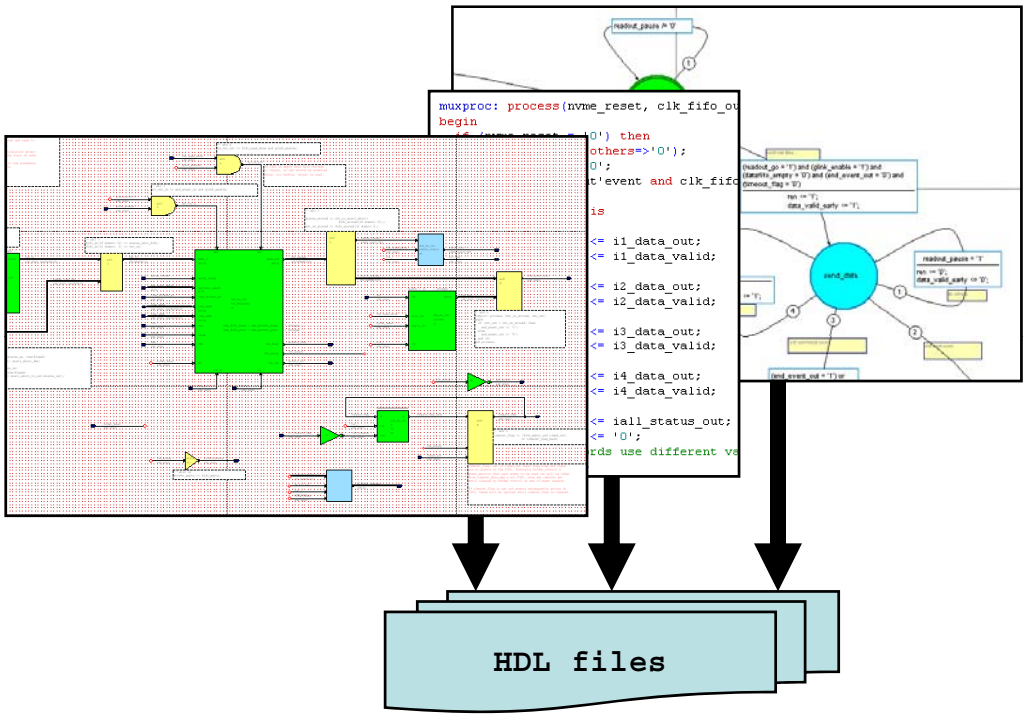
Languages

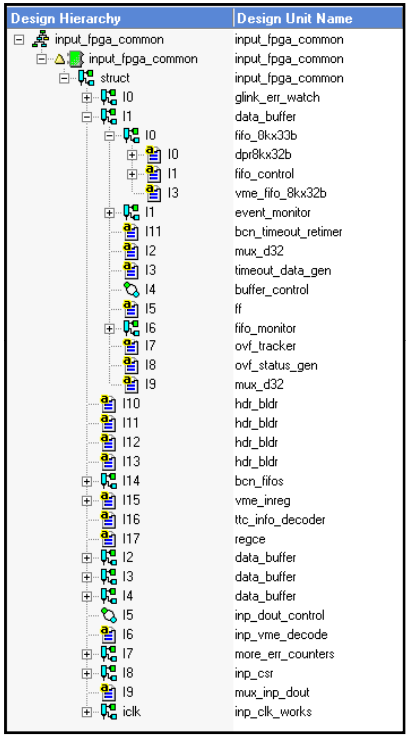
- HDL: Hardware Description Language
- VHDL, Verilog, System C….
- Comparable to computer languages, except for concurrent nature

```
sig_A <= sig_B;
sig_B <= sig_C;
```

  - sequential processes can be implemented (all processes run concurrently)
- Used for:
  - Synthesizable code (RTL = Resistor Transfer Level)
  - High-level behavioural descriptions for simulation
- Logic can be functionally correct but unsynthesizable
- VHDL: many constructs and commands exist for simulation only

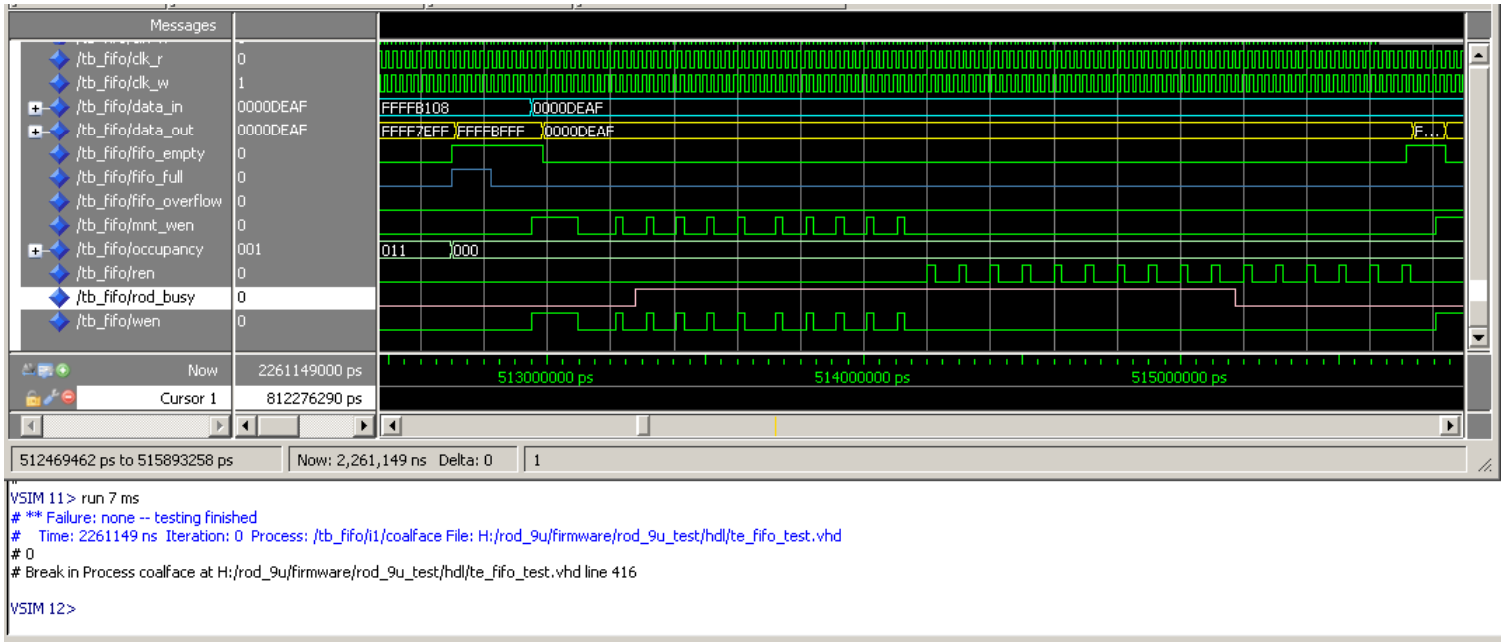
Graphical Design Entry





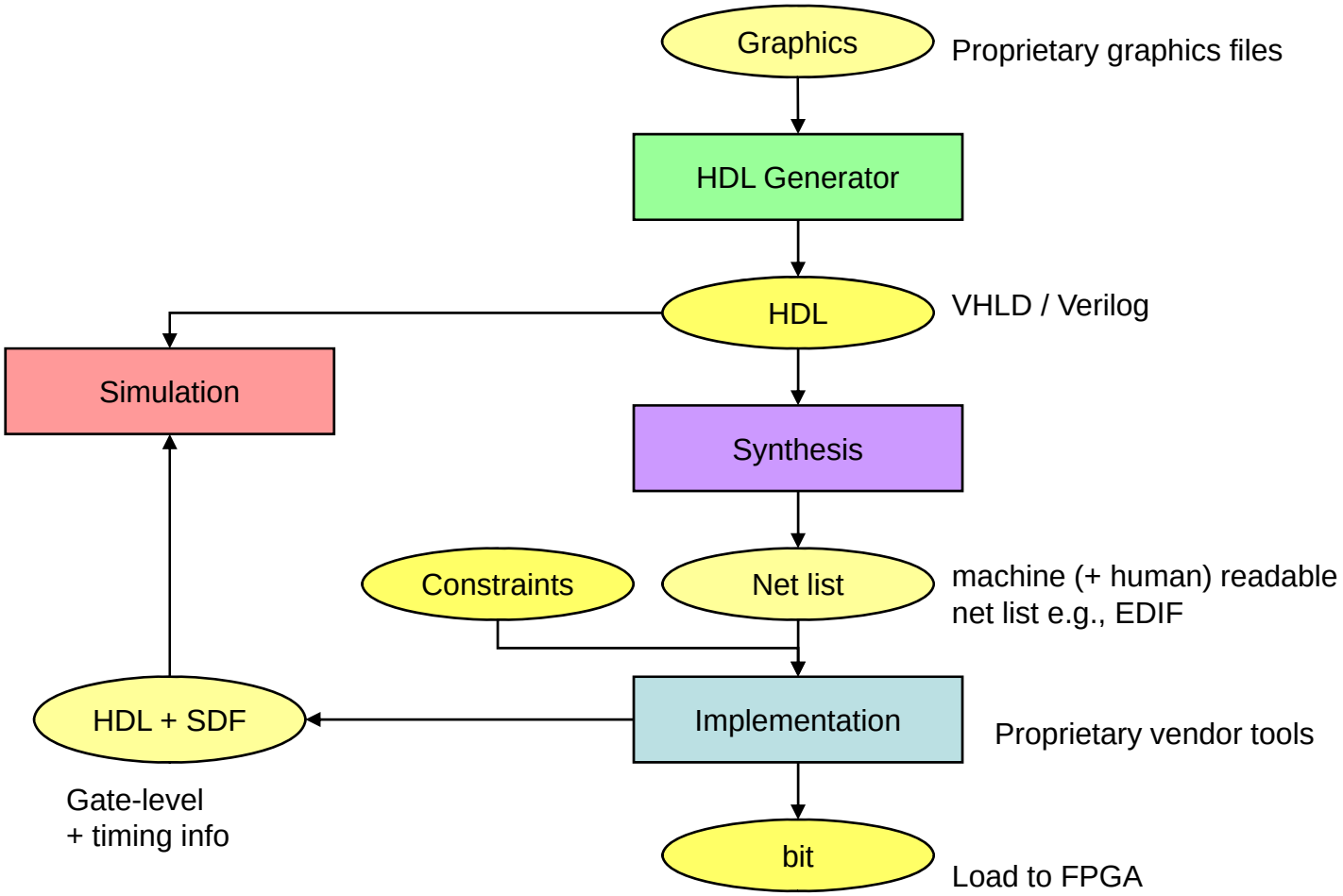
- Entirely optional
- Converts block diagrams, state machine diagrams, truth tables, flow charts → HDL
- Manage files, navigate design hierarchy
- Coupled to simulator
- Documentation

Simulation

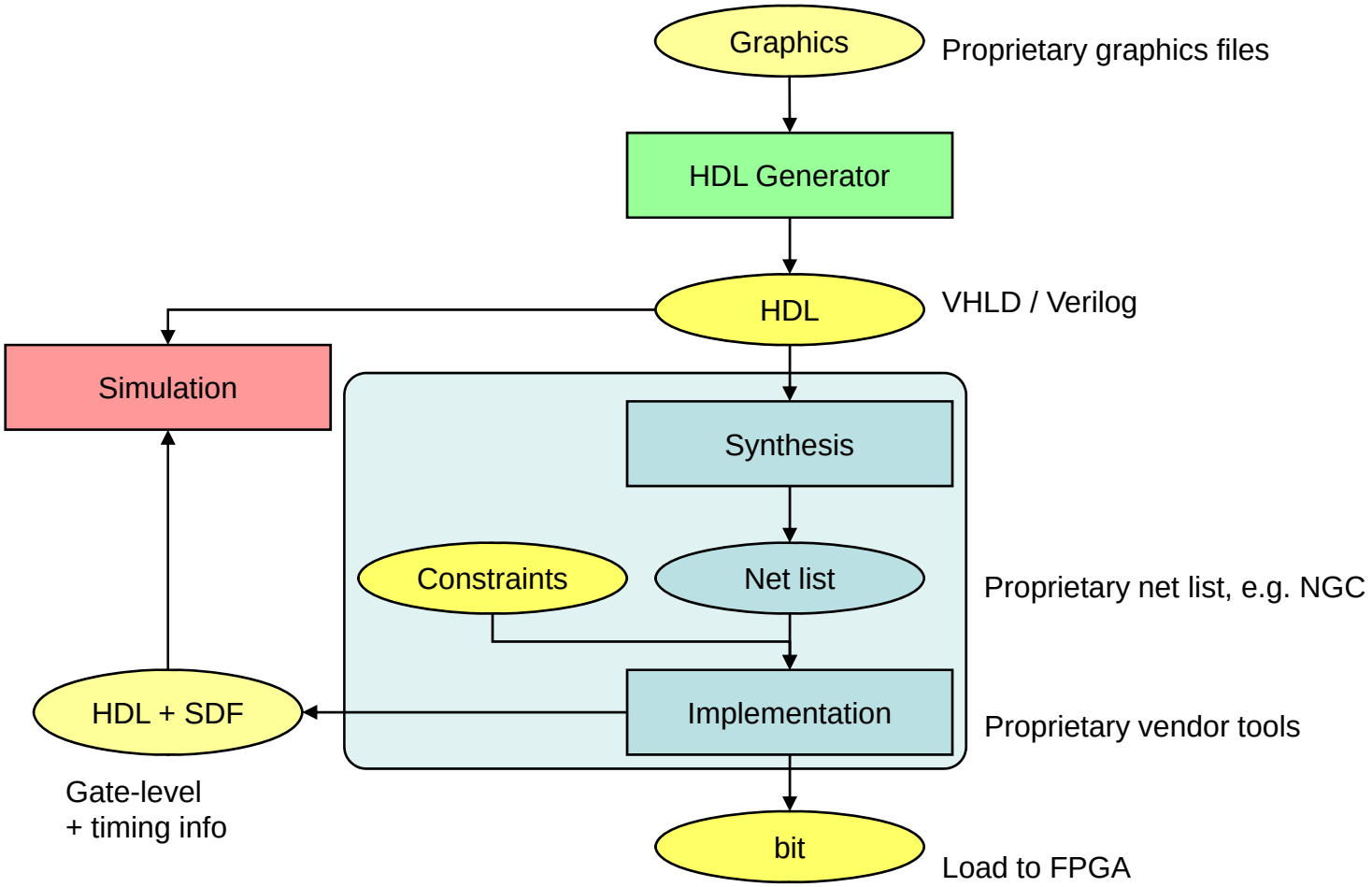


- Number of approaches to testing:
  - Input test vectors by hand, via files, or from HDL test engines…
  - Verify performance by
    - Visual waveform inspection,
    - Automated test benches – examine data and report errors
    - Write data to files (+ test by external software)

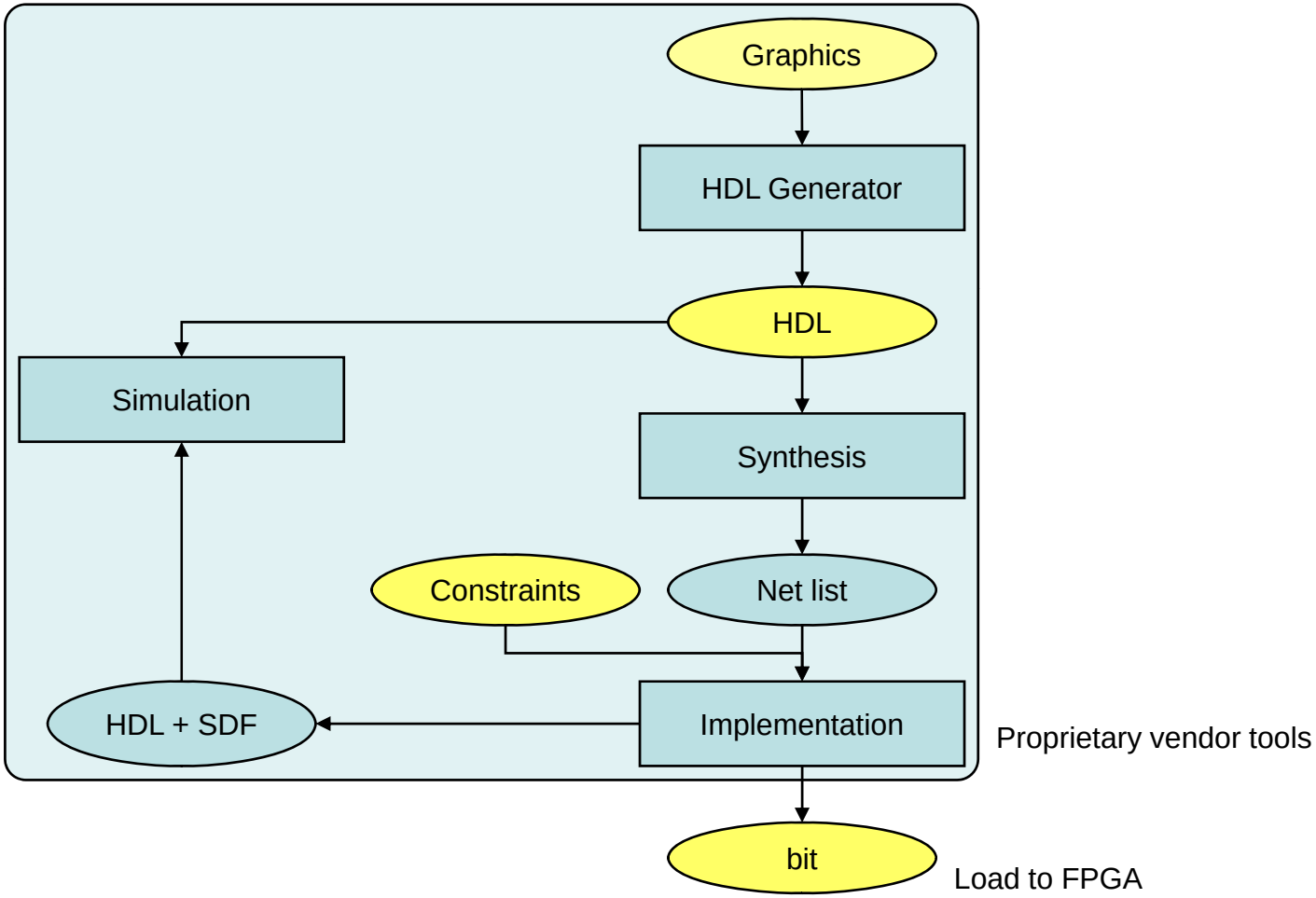
The Design Flow (1)



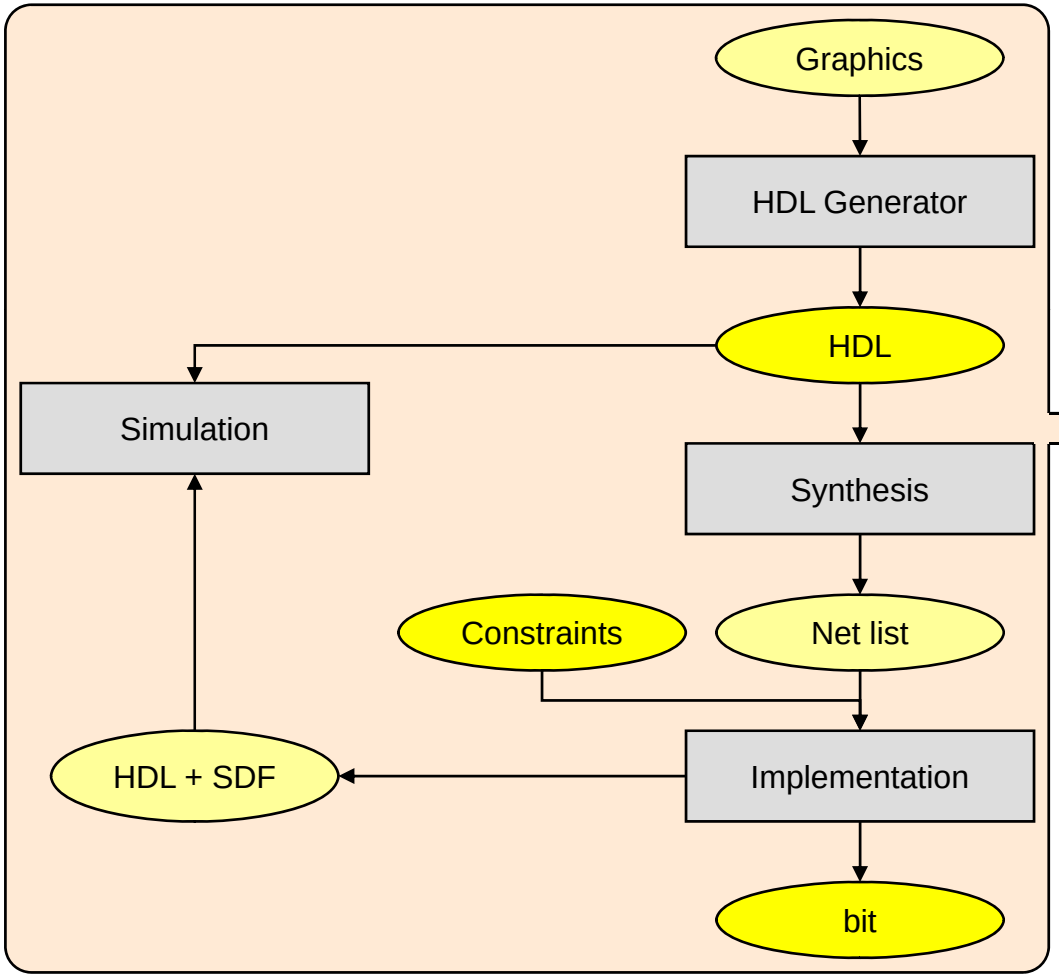
The Design Flow (2)



The Design Flow (3)



Version Management / Archiving



- Stand-alone or integrated with design tools
- Archiving
  - Back-up
- Version Management
  - Branching
  - Access control for multiple Users

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Design Tools Used in L1 Calo

	Graphical Design Entry	*Simulation*	*Synthesis*	*Implementation*
Mentor graphics FPGAdvantage	**HDL Designer**	**Modelsim**	**Precision**	
Xilinx ISE		**ISE/Modelsim**	**XST**	**ISE**
Altera Quartus II		**Altera-Modelsim**	**Quartus**	**Quartus**

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Tools & Methods Spreadsheet (1)

		B'ham	H'berg	Mainz	RAL	S'holm
Main responsibilities		**CPM**	**PPR**	**JEM**	**CMM, ROD, CPM**	**JEM**
Language	**VHDL**					
	Verilog					
Vendor	**Altera**					
	Xilinx					
Devices	**FPGA**					
	CPLD					
Entry	**HDL**					
	HDL Designer					
Synthesis	**Precision**					
	XST					
	Quartus					
Implement	**Quartus**					
	ISE					

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Tools & Methods Spreadsheet (2)

		B'ham	H'berg	Mainz	RAL	S'holm
Simulation	**Modelsim**					
	ISE					
	Behavioural					
	Gate-level					
	high-level models					
IP	**Vendor**					
	3rd Party					
Tool Use	**GUI**					
	Scripting					
Embedded						
Archiving & Version Management	**CVS**					
	Synchronicity					
	Subversion					
	TAR/zip					
Documentation	**Firmware Designs**					

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Conclusions

- Language: VHDL / Verilog:
  - tools can handle both in one design.
  - So can designers, if they have to….
- Front-end entry packages option
  - Many advantages for design entry, organisation, navigation
  - However, not portable
  - Don't rely on long-term availability of these tools for maintenance
  - (Suspect functionality will be incorporated into vendor tools)
- VHDL is the prime source for archiving and sharing
- Proprietary vendor firmware unavoidable
- Proprietary vendor IP desirable
- We should all review our archiving policy
- We should all review our documentation
- **Many thanks to all who supplied information**

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} … but not right now.

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