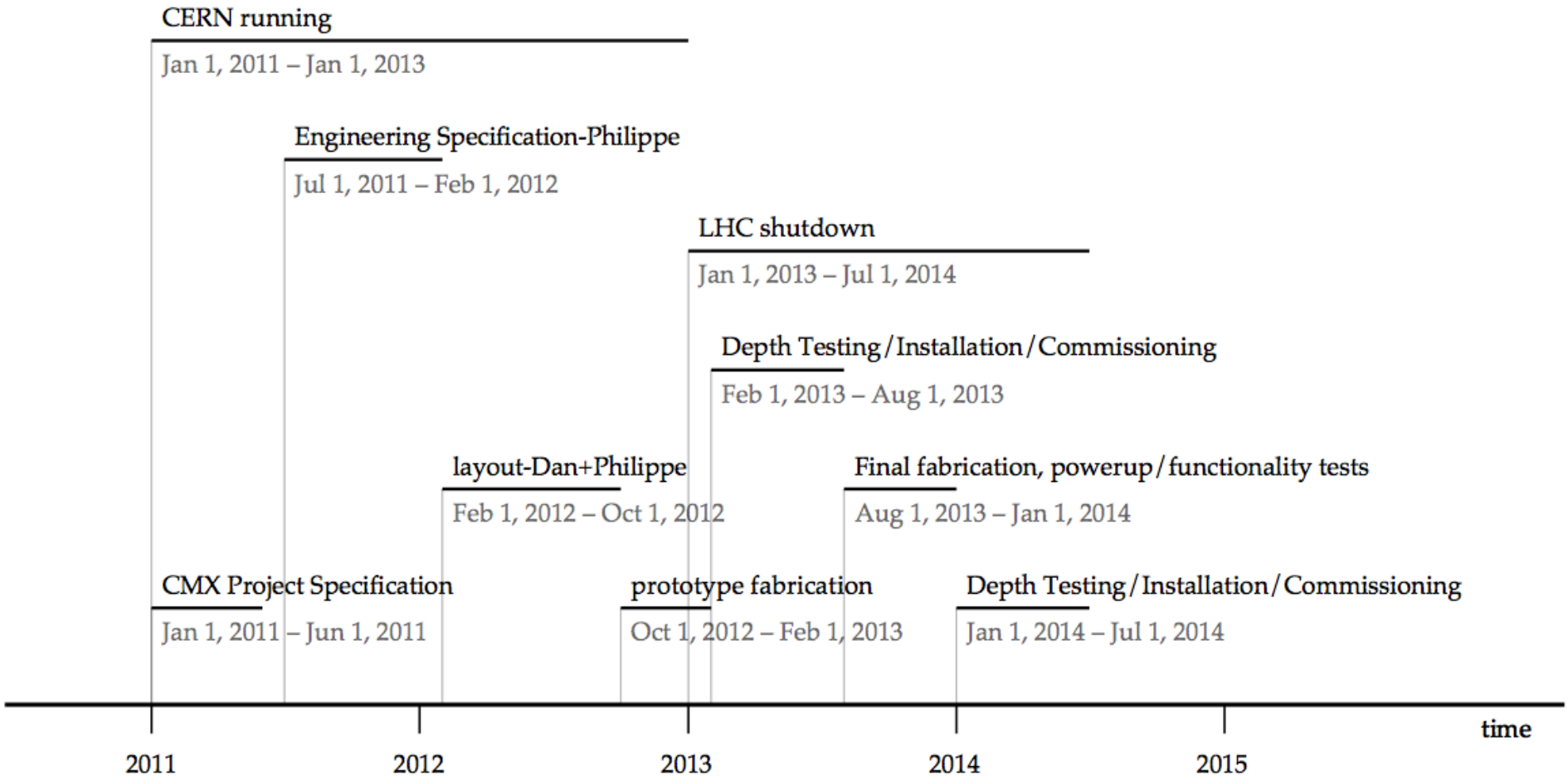
CMX:
TASKS AND SCHEDULE

Wojtek Fedorko for the MSU group

CMX development schedule as shown before (still valid)

- 2011: Project and engineering specifications
  - CMX project Preliminary Design Review (Done)
  - Preliminary design studies (Ongoing)
  - Test rig installed, checked out at MSU (postponed until 2012)
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout (ongoing)
  - CMM firmware ported on CMX
  - Prototype fabrication (fall 2012)
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review
- 2013: Prototype testing/installation/commissioning, final fabrication
  - Full prototype tests in test rig at CERN
  - CMX firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMX modules
- 2014: Final commissioning in the L1Calo trigger system in USA15

CMX development timeline: Yuri's/Dan's slide from mini-TDAQ



Hardware milestones

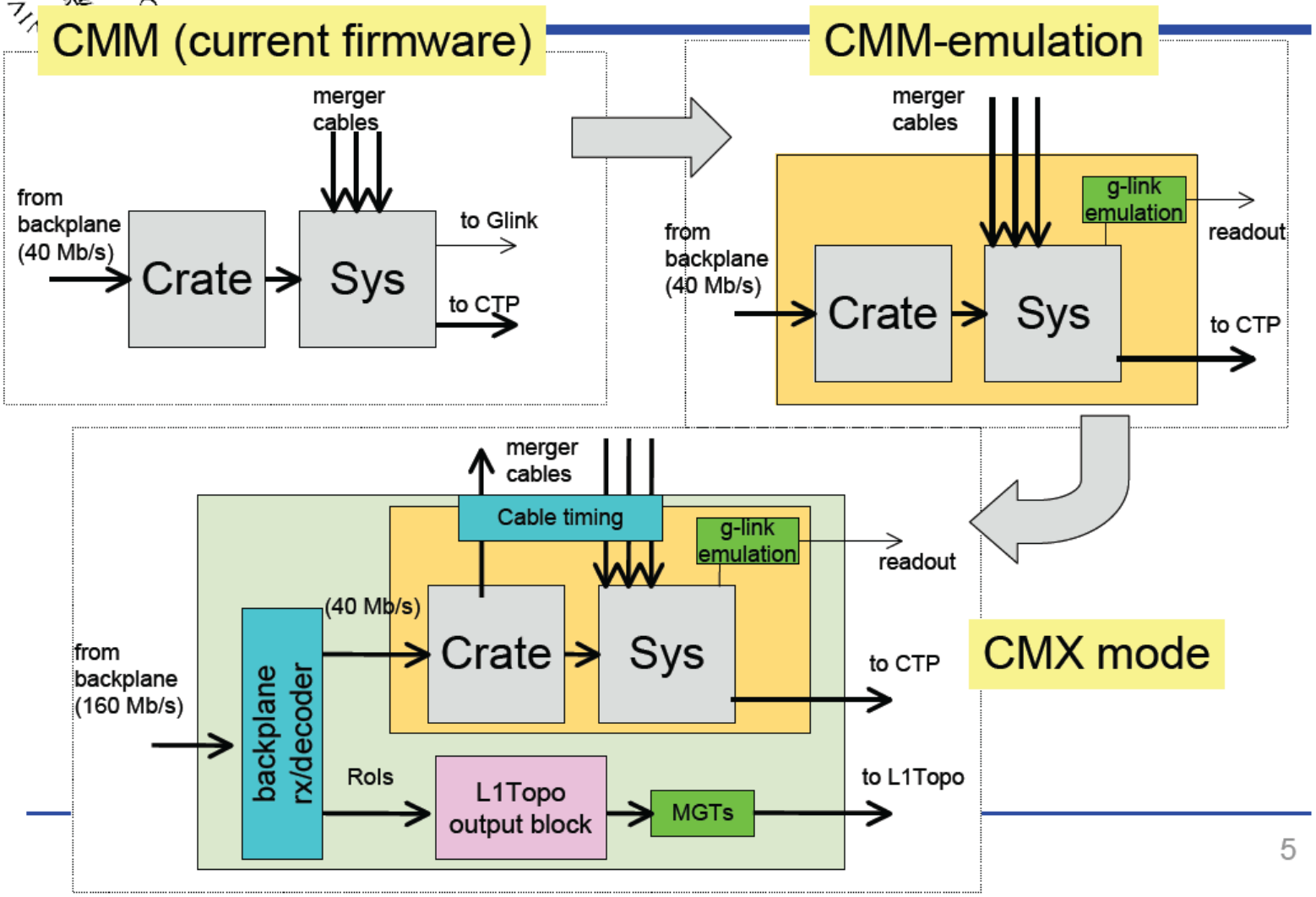
- Preliminary Design Review (PDR): - Stockholm
- Final Design Review (FDR)
  - Not included in the scheduled discussed previously
  - Required procedure?
  - If required best option would be to have FDR after design sent for fabrication
- prototype: 2013.01.31
- Production Readiness Review (PRR):
  - After prototype received and tested
- production: ~fall 2013
- installation: ~spring 2014

Firmware development planning

Slide from Sam's May 24th talk

"MSU will develop format-independent boundaries to the FPGAs on the CMX, and coordinate subsystem-specific code development with other institutes."

Base-CMX FPGA



Base CMX Firmware versions: from Sam's May 24th talk

Areas of responsibility:

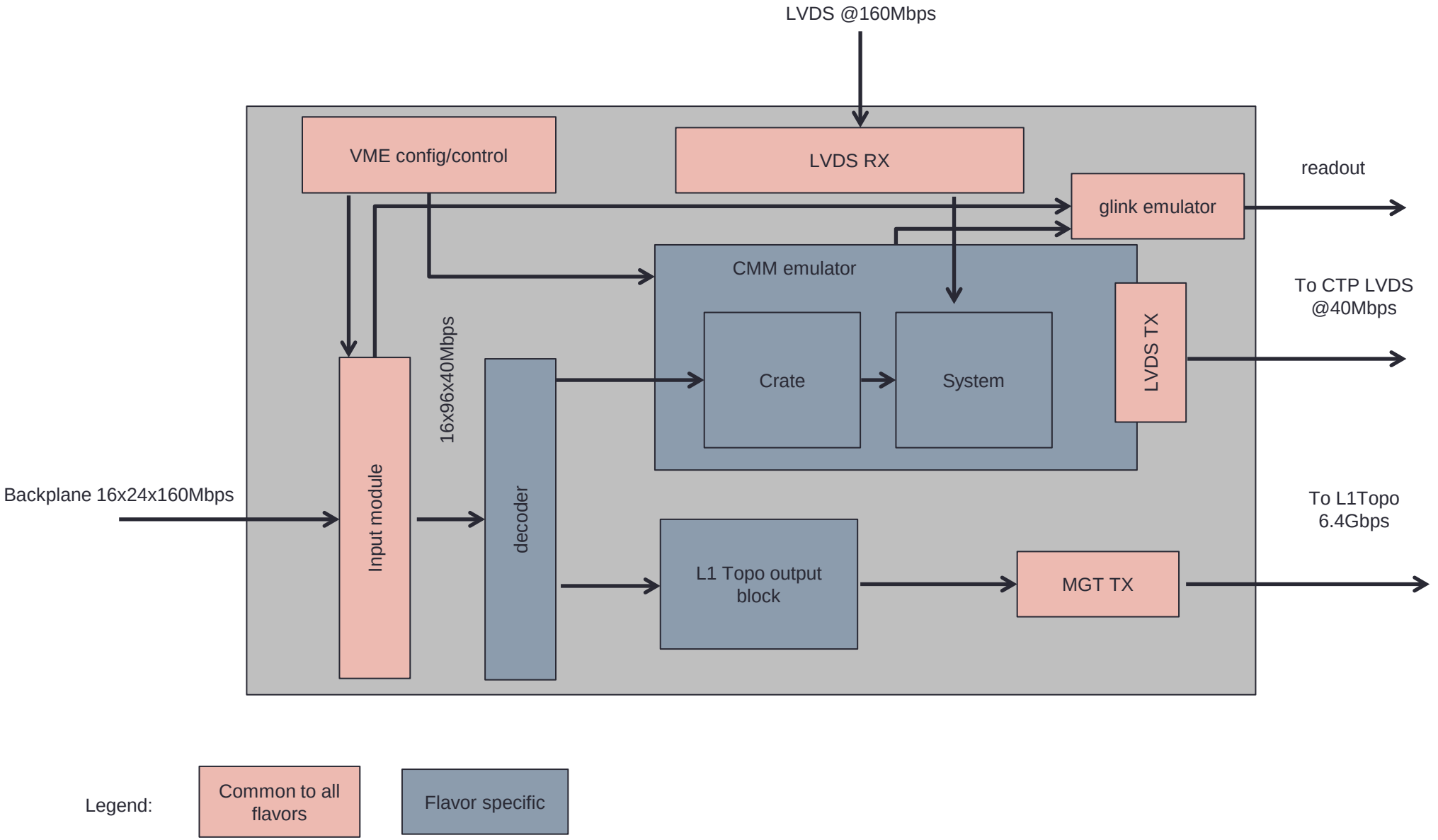
Version	CMM-emulation	CMX mode	TP-CMX
Test/diagnostic	MSU	MSU	MSU
e/γ, τ	MSU**	MSU**	MSU provides base/common functionality Others contribute specific algos
Jet	Stockholm	Stockholm	
Energy-sum	MSU**	MSU**	

* with support from RAL and Stockholm

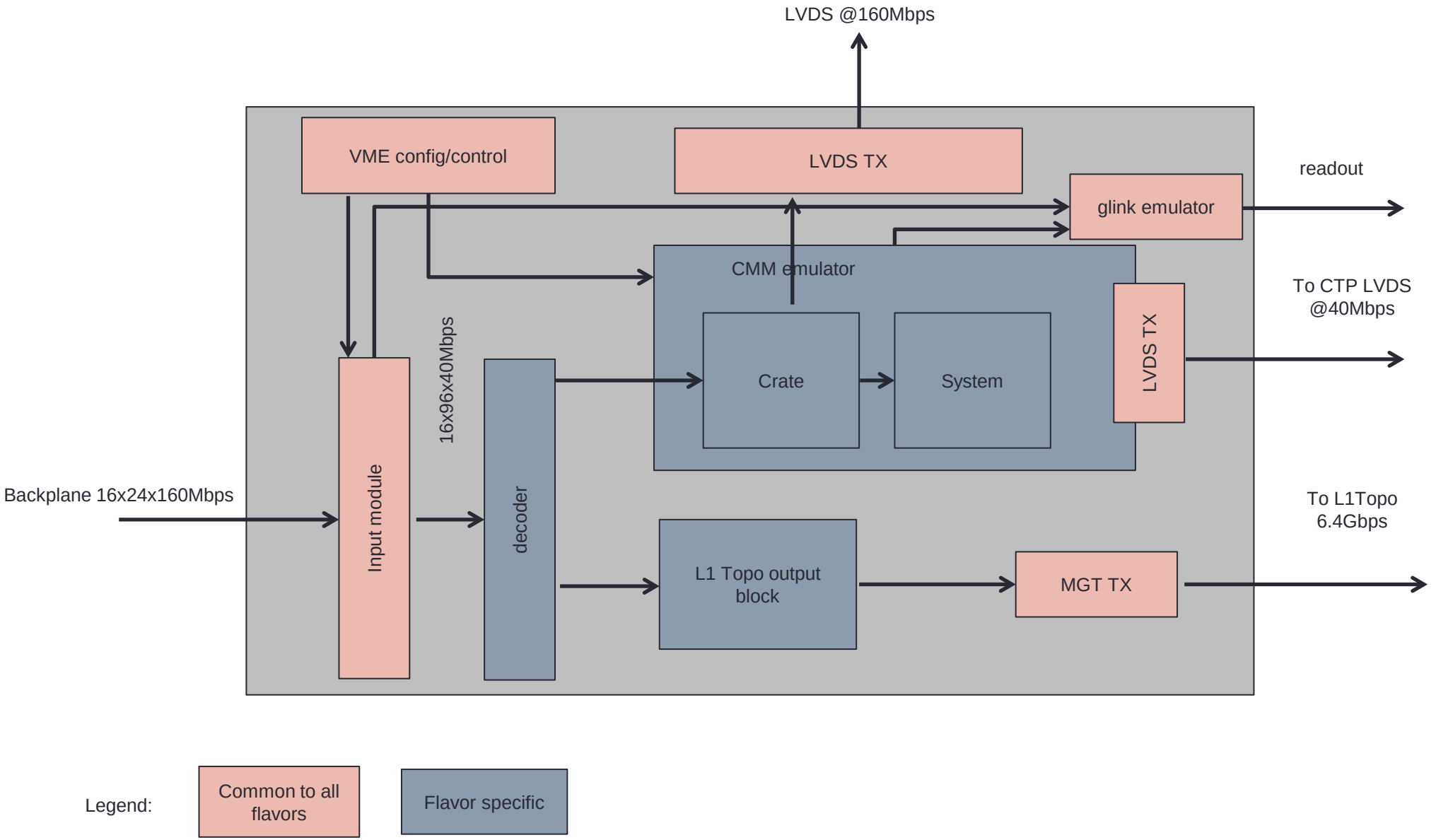
** continued development by Wojtek at UBC

** no firm commitment from MSU (except for coordination)

Base CMX Firmware – filling in the boxes (system)



Base CMX Firmware – filling in the boxes (crate)



Input Module

- Was needed urgently to guide layout
- Implemented with the clk/parity encoding scheme
  - Will be tested in eval kit
- First implementation with 80 MHz DDR scheme
  - Needs verification and eval kit test
- In both cases ‘toy’ interface
  - Full projected functionality
    - e.g. IDELAY, IDDR
    - details of how this would be configured will change
  - Capture data into registers and ‘deserialization’ into 96 bit word
  - No synchronization between channels
- Parity calculation and error flag

Other Firmware Modules

- Need to define functionality and interfaces between firmware ‘modules’
- Resource sharing (e.g. MMCM – clock generation and buffering)
- ‘Take out’ some functionality from the CMM emulator module
- Start work from the ‘Jet’ version of CMX
  - Expect that common module interfaces will work for other versions
  - Manpower (Pawel) available to work on this version outside of MSU
    - Experience with CMM
  - Will be able to use this or stripped down version of this firmware for board tests
  - Need complete firmware before prototype arrives early next year. Hope ready sooner.
  - Part of firmware testable in Yuri’s TTC/VME/ACE test card.
  - Expect duty cycle between Pawel and myself to decrease in the coming weeks.
  - Other firmware versions will follow after prototype tests.

Questions that need clarification to guide the firmware design

- 80MHz DDR on bit 24 decided?
  - Do we have an agreement on data formats for all flavors?
  - Circulation of documentation?
- Location of parity bit
  - Constant in the payload between the flavors?
- Synchronization of processor inputs
  - At which stage this needs to happen? Input module?
- Efficient use of the data format
  - What data can be made available early to minimize latency?
- Behavior on error?
  - Include information in the real time data?
  - Special L1A to force readout?
- …

CMX Topo FPGA

- Plans for firmware development need to be discussed
- Hope for common firmware architecture with L1Topo
- Test version needs to be ready for prototype testing.
  - Link tests

Software development (Seth Caughron)

- Goals:
  - Ability to test the VME/TTC/ACE test card and CMX within L1Calo software framework
  - Develop expertise now using the 6U crate in bldg. 32 and Yuri's test card
  - When prototype arrives we must be ready to test it.
- Status:
  - We need and are getting help
  - Murrough and Seth have cloned the software objects modeling the CMM into CMX
    - Assumes CMX register model will be an evolution of the CMM
  - Working on setting up a small partition in the 6U crate
  - Will be 'playing' with Yuri's card on completion of the inspection and smoke test (mid August)

Conclusions

- Hardware schedule well defined
  - Procedural question about FDR
- Base CMX firmware goals set
  - Most urgent tasks guiding hardware design complete
  - Need finer planning of further development and more intermediate goals
- TP-CMX firmware needs more thinking
- Software work just starting
  - Discussion in this forum very welcome
  - We are grateful for the expertise provided so far (and we'll need more)