CMX

testing, installation and integration plans

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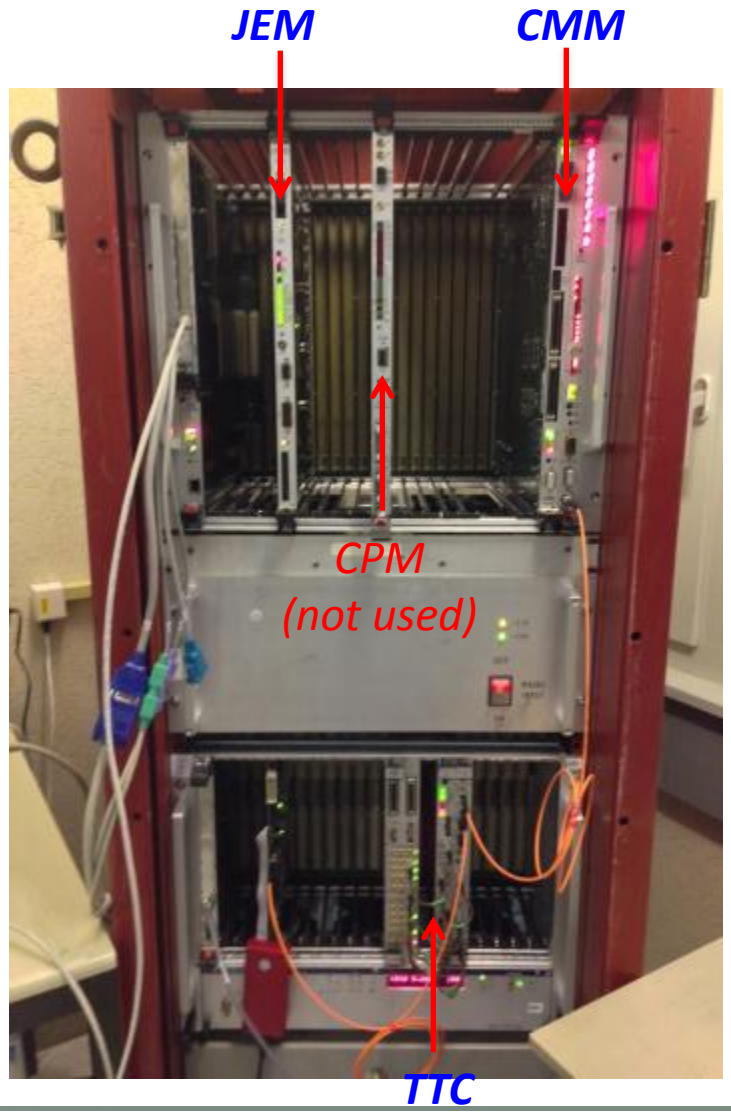
Introduction

- General Plan:
  - CMX prototype expected end of November/early December
  - Initial board checkout @ MSU
  - Board interface tests @ MSU / CERN
  - System tests at CERN starting mid December/Jan
    - Lab 104
    - Full rack tests in USA15
- Current and future activities:
  - MSU test rig preparation
    - Needed for initial tests @ MSU
  - CAN bus controller tests
    - Decision on purchase of full batch of microcontrollers
  - Preparation for the interface tests

MSU test rig

- MSU test rig
  - Processor crate on loan to MSU
  - Prototype custom backplane
  - Hardware setup in good state: SBCs, TTC, one JEM, one CMM
  - Software support
  - Currently in B32 lab
  - To be shipped to MSU next week



MSU test rig

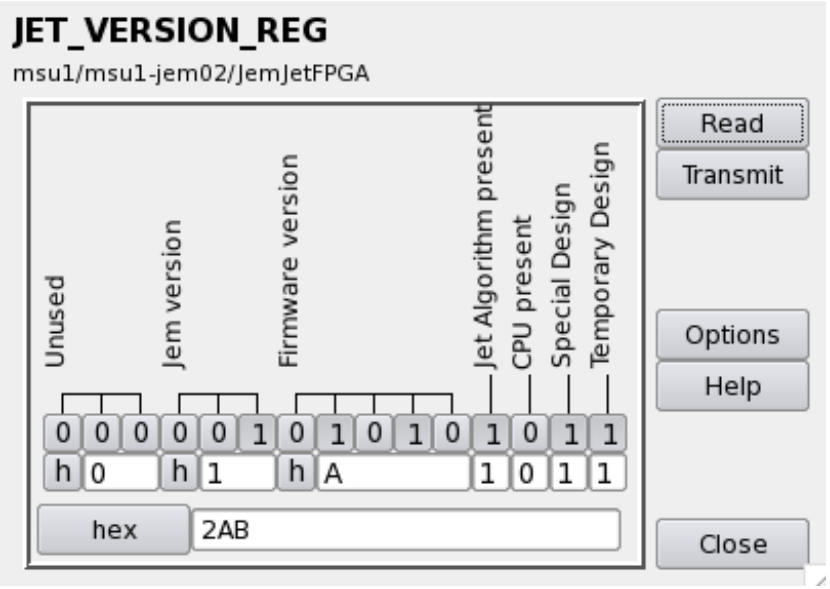
- Software and databases updated to accommodate the hardware in the test rig
  - Officially in SVN now under partition “MSUtest”
- System running with JEM and CMM
  - Able to send test vectors for CMM and for JEM->CMM chain
  - Able to change test vectors for CMM/JEM
  - Some quirks with the setup being not officially in the CERN TDAQ environment, e.g. not common disk space between computer running the partition and SBCs, but under control
- *Thanks to Murrough and Bruce!*

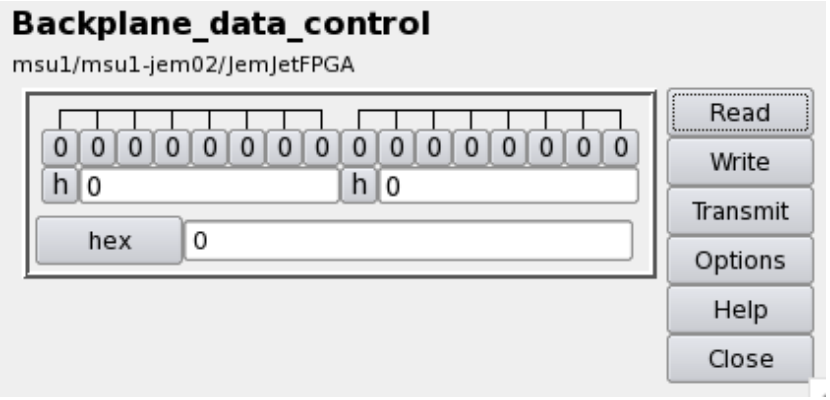
MSU test rig

- MSU test rig in preparation for testing at MSU: Duc
  - Preparation to run the test rig “standalone” at MSU
    - Netboot of the SBCs, setup of TDAQ software
- New firmware for JEM: Pawel
  - 160 Mbps backplane rate
  - Output spy memory support
- Software support for the new Firmware: Jan Schäffer
  - First version prepared
  - Support for extended firmware features

MSU test rig

- Tests in B32:
  - First versions of the new firmware and software
  - Firmware version not recognized by software, yet (manual override check for now)
  - Backplane output spy memory loaded via command line
  - Debugging the firmware and software on-going





L1Calo DCS interface to CMX: background

- DCS CANbus interface to CMX is based on the CMM microcontroller
  - for compatibility with L1Calo DCS software
- Fujitsu MB90F594 microcontroller is obsolete
  - Not available from Fujitsu supply chain anymore
  - Absence of a backward compatible devices for F2MC-16LX family
  - Parts available from resellers for 20-50 times higher price
- Possible solution:
  - Find a "reliable" re-seller, buy a few chips and test them in the L1Calo
    - 5pcs x 48.00 EUR acquired from Club Electronics
    - CANbus card, designed for PPM, used as a test card
    - L1Calo DCS environment
  - Add connectors for a (possible) daughter card with DCS functionalities
    - Done by Dan on the CMX

CANbus microcontroller testing: Paul Thompson, Bruce, Yuri

- PPM CANbus card used as a test board
  - 2 bare PCBs, connectors, docs from Paul Hanke
  - Card mounted at CERN
  - PPM in the L1Calo test rig (Bld.104)
  - Hardware program adaptor from Klaus Schmitt
- Testing in the L1Calo test rig
  - L1Calo test rig DCS environment used for the tests
    - Softune software to develop and compile the CANbus code
      - same version of the CAN code on all CAN chips in all L1Calo modules
    - Accemic software to program the CANbus microcontroller via serial interface
    - PVSS system on DCS control PC (CANbus interface to TCM)
      - CANbus controller on TCM to interact with CANbus controllers on L1Calo modules
  - CANbus card programmed stand alone using serial interface
  - Test on the PPM module in the L1Calo DCS environment
    - In parallel with the L1Calo DCS environment update and move to W7
    - in progress: investigating HW and SW issues

Courtesy of Heidelberg University.

Initial test Plan at MSU

- Basic Tests (est 2 weeks):
  - Board Inspection
  - Installation of variety of jumpers and components not included in the assembly
  - Grounding and Power verification
  - Clocking tests and characterization
  - FPGA programming, JTAG/CF

Interface test Plan

- Performed utilizing the MSU rig and later in parallel
- Special Test firmware versions for BF and Topo FPGAs
  - Utilize FW components from Target FW
  - Embed Chipscope cores for control and monitoring minimizing SW support necessary
  - FW in preparation (Wojtek, Pawel)
- Target (or close to target) FW for Board Support FPGA (Yuri)
  - Control of the AVAGO TXRXs
  - LVDS buffer control
  - TTC control
  - In preparation

Interface test Plan: shopping list

1. Establish the system clocking for Base and Topo FPGAs: 0.5 day
    1. Lock on 40.08 MHZ clocks DSKW_1 and 2, as well as 320, propagate MMCMs lock and recovered clocks on the debug pins. measure jitter properties.
    2. Capture the TTCdec signals on Base and Topo FPGA's
2. Backplane connectivity and timing measurement: 3 days
    1. Static pattern capture
    2. Measure relative time delays between signals P0-23 and 24 from a single JEM.
    3. Test data transfer at 160Mbps from a single JEM, moving the JEM periodically from slot to slot.
    4. Variety of patterns, including stress patterns
    5. Detect parity error
3. Low speed serial TX connectivity test; 1 day
    1. establish reference 120.00MHz clock lock for the PLLs on the two GTX's
    2. use the G-Link emulation firmware module to send out a pre-defined or predictable data pattern on 4 fibers and use a test receiver to flag errors.
4. High speed serial Base RX/ Topo TX connectivity: 3 days.
    1. establish PLL lock for the reference clocks on BASE and Topo Function
    2. send out a test PRNG test pattern from the Base FPGA and capture on Topo FPGA
        1. Pattern conforming to CMX->Topo protocol
        2. 8b/10b and CRC monitoring to flag errors
        3. Test all (2 ribbons) outputs and (3 ribbons) inputs
5. LVDS RTM (crate ->system) communication at 80 Mbps: 1 day
    1. loopback tests each of the 3 rear 27 pair connectors tested in both directions (A->B, A->C, B->A, C->A)
        1. PRNG patterns, stress patterns
        2. Detect Parity error
6. LVDS frontpanel (CTP) communication at 40 Mbps: 1 day
    1. Base-> Topo and Topo->Base test pattern transmission from one connector to the other when either of the connector is driven or receiving from Base or Topo.
7. BASE->TOPO GPIO link: 0.5 day
    1. Test LVDS and direct connectivity
    2. Push rate

B104 and Full crate tests (CERN)

- Needed before Production Review
- Fully loaded crate of JEMs @ 160Mbps
  - CMX in left and right slots
  - CPMs also if possible
- Needs to be done in the cavern
- We would like to schedule it for mid Jan.
- Preparation for the tests in December if possible in B104

Further tests and installation and commissioning

- Jan-Feb: Full-crate test (USA15), patterns for L1Topo (104), Production RR
- Feb-Mar: Final fabrication & QC of production boards @MSU
- Apr-Jul: Installation and commissioning @CERN (M4: July 7-11)
- Aug-Sep: Test in the USA15 L1Calo system (M5: Sept 8-12)
- Oct-Dec: Integration with L1Topo (M6: Oct 13-17)