SFX-424G Synchronous Clock Generators

CONNOR WINFIELD

PLL

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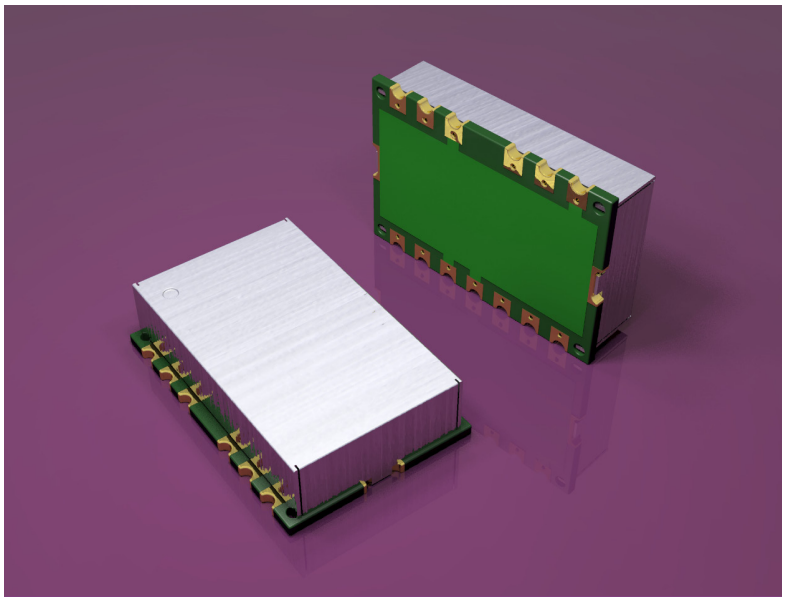


Applications

SONET / SDH / ATM
DWDM / FDM
FEC (Forward Error Correction)

Features

- 3.3V High Precision PLL
- Jitter Generation OC-192 Compliant
- Surface Mount
- Accepts up to 4 Inputs from an External MUX
- Inputs Compatible with CMOS/LVDS/LVPECL
- Frequency Translation up to 800 MHz
- Alarm detection for Loss of Lock/ Loss of Reference condition
- ROHS Compliant

RoHS COMPLIANT

Bulletin	**SG124**
Revision	**03**
Date	**10 May 2011**

General Description

The SFX-424G is a high precision frequency translator that translates up to four inputs from 8 kHz to 100MHz, to output frequencies between 8 MHz and 800 MHz. The SFX-424G supports all major FEC rates such as 15/14, 255/237 etc.

SFX-424G is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment. The SFX-424G provides a jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SFX-424G includes a lock detect alarm output. The PLL control voltage is brought out through a 470 kΩ resistor and can be used to determine when the pull range limits are reached. The LVPECL outputs may be put into the tri-state high impedance condition for external testing purposes by asserting a high signal to the Enable/Disable pin.

Parts are assembled using high temperature solder to withstand surface mount reflow process. This product is compliant with all required ROHS specifications.

Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage (OptionD)	-0.3	-	4.0	Volts	
VI	Input Voltage	-0.2	-	Vcc +0.3V	Volts	
Ts	Storage Temperature (OptionF)	-55	-	125	°C	
	Storage Temperature (OptionA)	-40	-	85	°C	

Specifications

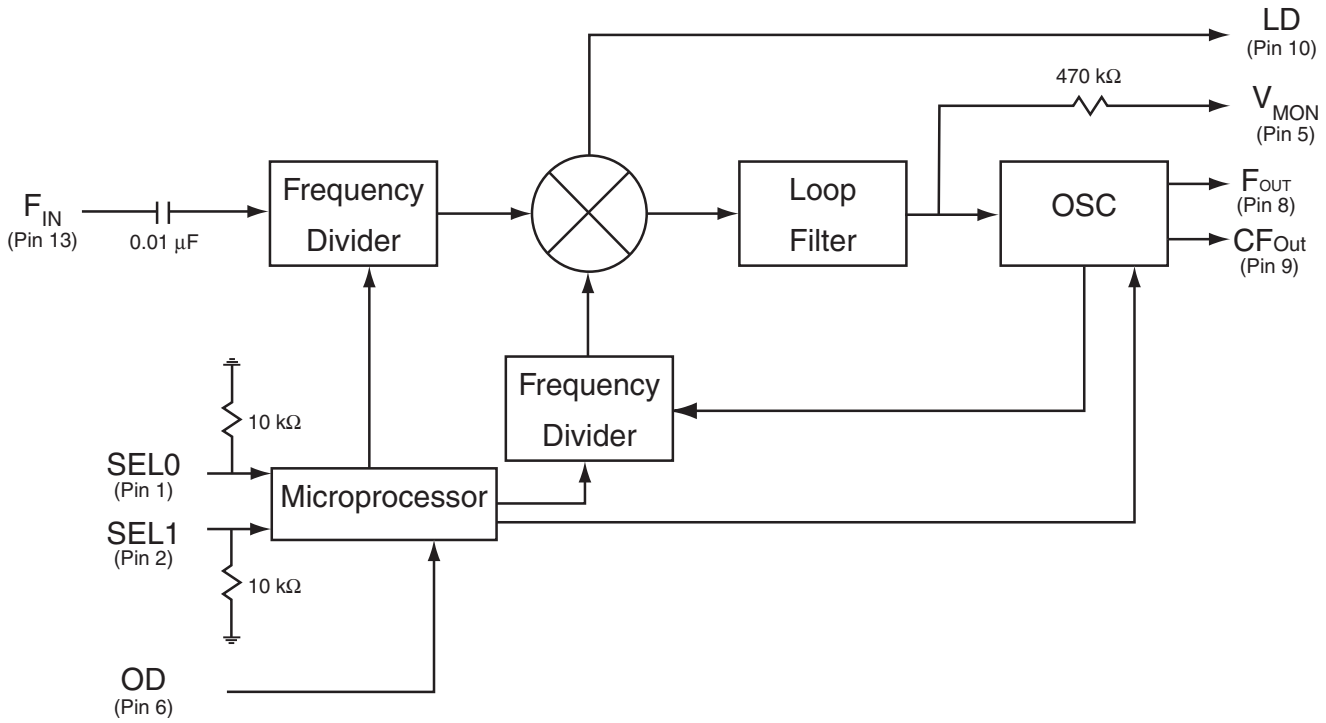
Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
f_{IN}	Input Frequencies	8 k	-	100 M	Hz	
f_{OUT}	Output Frequencies (LVPECL) 19.44 M	-	800 M	Hz		
	Output Frequencies (LVCMOS)	8 M	-	130 M	Hz	
Vcc	Supply Voltage (3.3 VDC)	3.13	3.3	3.46	Volts	
I_{CC}	Supply Current -	60	-	mA		
LVCMOS INPUT						
V_{IH}		2	-	VCC	Volts	
V_{IL}		-0.3	-	0.8	Volts	
LVPECL INPUT						
V_{IH}		1.49	-	2.72	Volts	
V_{IL}		0.86	-	2.125	Volts	
LVCMOS OUTPUT (Option A)			TYP. LVCMOS			
LVPECL OUTPUT (Option F)						
V_{OH}		2.275	-		V	
V_{OL}		-	-	1.68	V	
T_R/T_F	Rise/Fall Time @20% to 80%	-	0.6	1.5	ns	
SYM	Output Symmetry	45		55	%	
J_{GEN1}	Jitter Generation RMS (12 kHz - 20 MHz)	-	0.35	-	ps	1.0
J_{GEN2}	Jitter Generation RMS (12 kHz - 20 MHz)	-	0.50	-	ps	2.0
J_{TRAN}	Jitter Transfer	-	-	0.1	dB	3.0
APR	Input Frequency Tracking	±40	-		ppm	
T_{OP}	Operating Temperature **F** =	-40	-	85	°C	
	C =	0	-	70	°C	
SSB Phase Noise (for SFX-424G-DFF-A10Z only)						4.0
	at 10Hz offset	-	-57	-45	dBc/Hz	
	at 100Hz offset	-	-92	-80	dBc/Hz	
	at 1kHz offset	-	-120	-110	dBc/Hz	
	at 10kHz offset	-	-138	-135	dBc/Hz	
	at 100kHz offset	-	-150	-145	dBc/Hz	
	at 1MHz offset	-	-157	-147	dBc/Hz	
	at 10MHz offset	-	-160	-150	dBc/Hz	
$\emptyset_{OFF}$	Phase Offset	-	5	15	ns	

NOTES: *1.0 155.52 MHz* *2.0 156.25 MHz* *3.0 GR-253-CORE, Sec. 5.6.2.1.2* *4.0 For other models and frequencies, consult factory.*

Functional Block Diagram

Figure 1



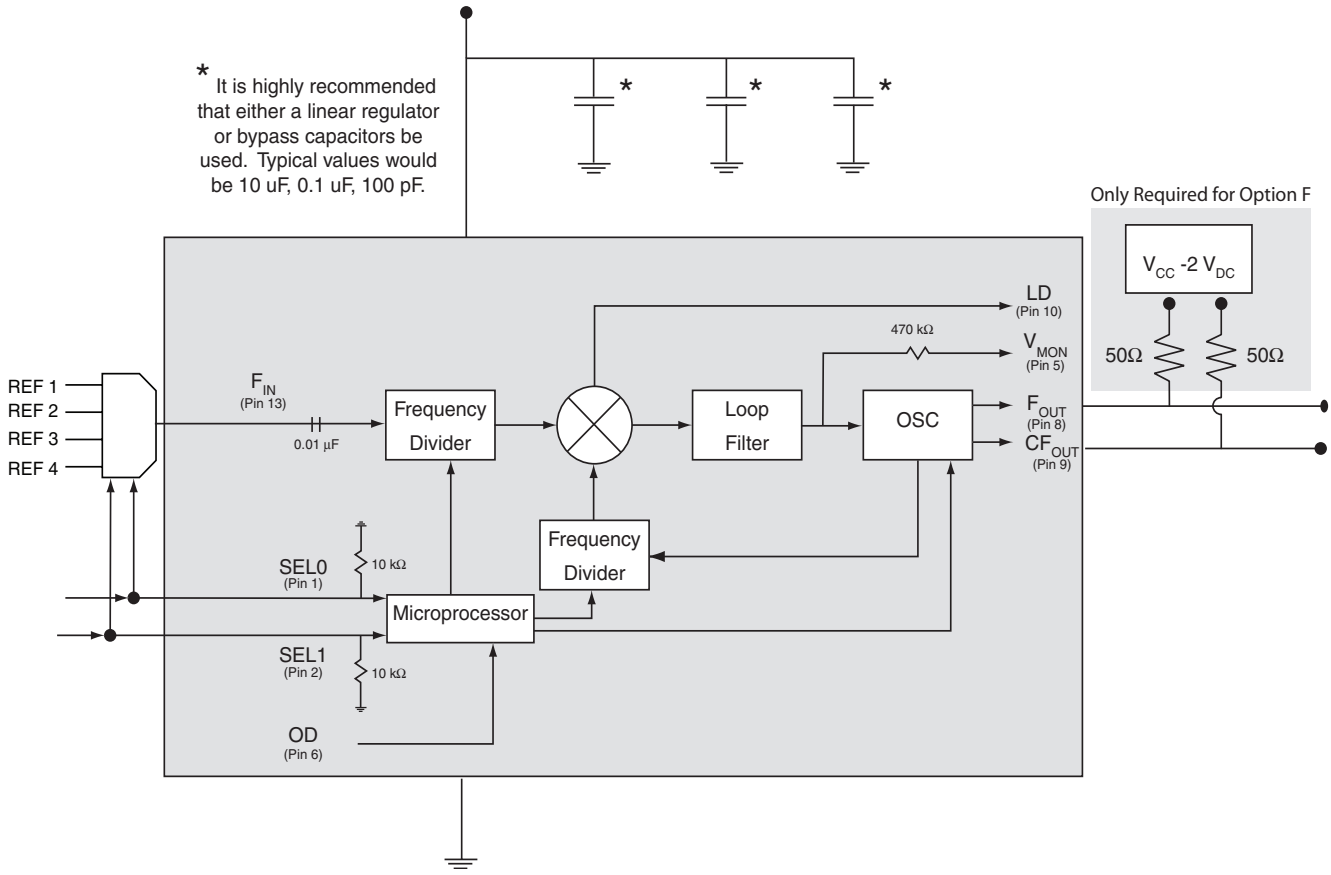
Pin Description

Table 3

PIN #	SYMBOL	I/O	Level	Function
1	SEL0	I	LVTTL	Input Frequency Select .* 10kΩ Pull down resistor
2	SEL1	I	LVTTL	Input Frequency Select .* 10kΩ Pull down resistor
3	GND	GND	Supply	Ground
4				Missing
5	VMON	O	Analog	VCXO Control VoltageUnder locked conditions VMON should be > 0.3V and <3.0V. The Input Frequency may be out of range if the voltage is outside of this voltage range.
6	OD	I	LVCMOS	Output Disable Disable = Logic 1 Enable = Logic 0 or No Connect
7	GND	GND	Supply	Ground
8	FOUT	O	LVPECL or LVCMOS	Frequency Output
9	CFOUT	O	LVPECL or GND	Complementary Frequency Output Note: For the LVCMOS Option, this connection is tied to GND
10	LD	O	LVCMOS	Lock Detect Locked = Logic 1 Loss of Signal = Logic 0
11	GND	GND	Supply	Ground
12	GND	GND	Supply	Ground
13	FIN	I	LVPECL or LVCMOS	Input FrequencyNote: Input is AC coupled for handling either LVCMOS or LVPECL input signals
14	VCC	VCC	Supply	Power Supply Voltage (3.3V ±5%)

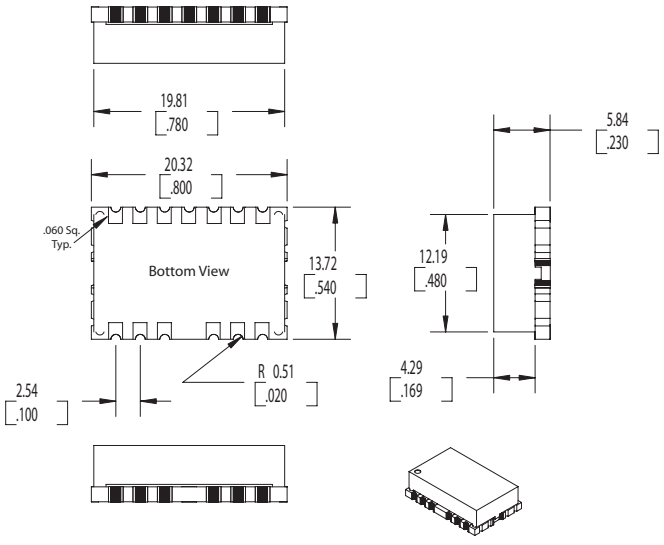
Output Load and Power Supply Filtering Recommendations

Figure 2



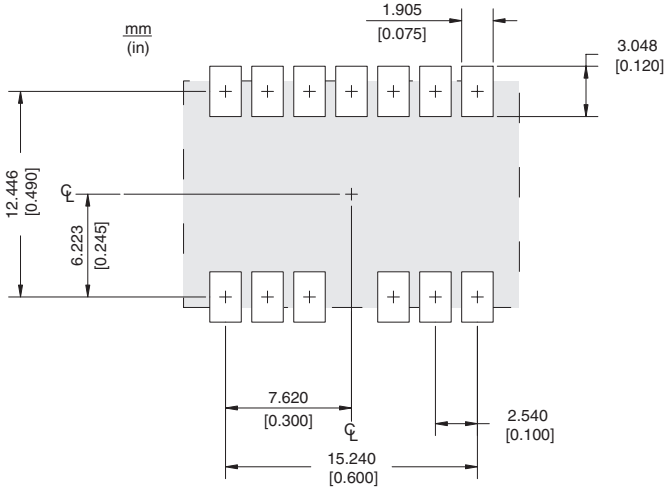
Package Dimensions

Figure 3



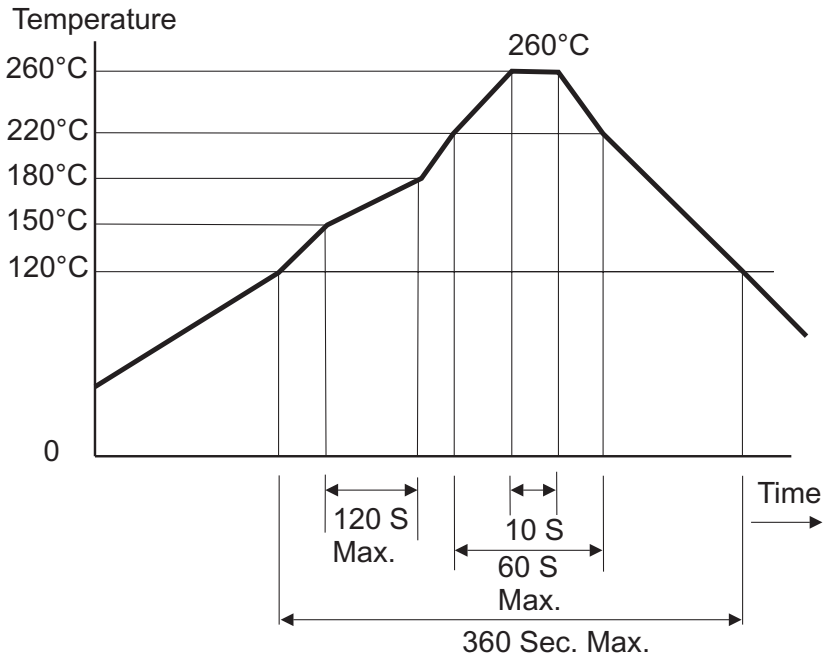
Recommended Footprint Dimensions

Figure 4



Solder Profile

Figure 5



Meets IPC/JEDEC J-STD-020C

Standard Frequencies

8 kHz	C	38.8800 MHz	X
16 kHz	D	44.7360 MHz	Y
64 kHz	E	204.80 MHz	Z
1.024 MHz	F	51.84 MHz	0
1.544 MHz	H	61.44 MHz	1
2.048 MHz	J	77.76 MHz	2
4.096 MHz	K	82.944 MHz	3
8.192 MHz	L	112.00 MHz	4
13.0000 MHz	M	139.2640 MHz	5
16.3840 MHz	N	155.5200 MHz	6
10.24 MHz	O	166.6286 MHz	7
19.4400 MHz	P	622.0800 MHz	8
20.4800 MHz	R	666.5143 MHz	9
26.0000 MHz	T	156.25 MHz	A
27.0000 MHz	W	Input Freq not listed	S
		Output Freq not listed	S

Ordering Information

SFX-424G- X X X - X X X X

Supply Voltage
D = 3.3 V_{DC} ±5%

Output Logic
A = LVCMOS
F = Comp. LVPECL

Temperature Range
C = 0˚C to 70˚C
F = **-4**0˚C to 85˚C
D = 0˚C to 85˚C

Input Logic
A = LVCMOS
F = LVPECL

Output Frequency (Options L - A)
See standard frequencies chart above.
* If the desired frequency is not listed, Please Consult a sales representative for availabilty of additional frequencies.

Input Frequency (Options C - 3)
See standard frequencies chart above.
* If the desired frequency is not listed, Please Consult a sales representative for availabilty of additional frequencies.

Number of Input Frequencies
1: 1 Input Frequency
2: 2 Input Frequencies
3: 3 Input Frequencies
4: 4 Input Frequencies

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Revision	Revision Date	Note
P00	6/30/06	Preliminary Release
P01	2/6/07	Added Solder Profile
P02	3/1/07	Added Mechanical Drawing
P03	6/7/07	Updated Solder Profile
P04	1/22/08	Updated Output Frequency Range
P05	9/19/08	Added Input Frequency Range to Tbl. 2
00	12/09/08	Change from Preliminary to Release
01	06/17/09	Jitter Change
02	04/06/11	Standard Frequency Updates & Temp Range & Solder Profile update
03	05/10/11	Added phase noise example spec & edited Package Dimensions