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## Description

The FX-400 is a precision quartz-based frequency translator used to translate an input frequency such as 8 kHz, 1.544 MHz, 2.048 MHz, 19.44 MHz etc. to any specific frequency from 1.544 MHz to 1.0 GHz. The FX-400 can perform either up or down frequency conversion. The FX-400's superior jitter performance is achieved through the use of a precision VCXO or VCSO. With the use of an external multiplexer, up to 4 different input clocks can be translated to a common output frequency.

## Features

- Quartz-based PLL for Ultra-Low Jitter
- Frequency Translation up to 1 GHz
- Accepts up to 4 ext.-muxed clock inputs
- LVCMOS / LVDS / LVPECL Inputs compatible
- Differential LVPECL /LVDS or LVCMOS Output
- Lock Detect / Loss of Signal Alarms
- Output Disable
- 20.3 x 13.7 x 5.1 mm SMT package
- RoHS/Lead Free Compliant

## Applications

- Wireless Infrastructure
- 10 Gigabit FC
- 10GbE LAN / WAN
- OADM and IP Routers
- Test Equipment
- Military Communications

## Block Diagram

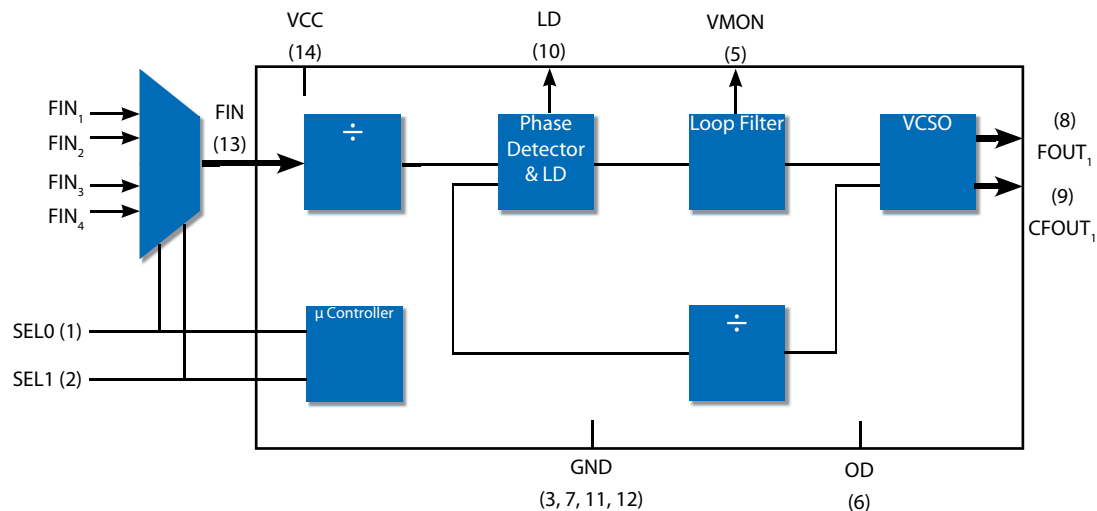


Figure 1. Functional block diagram

## Performance Specifications

Table 1. Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Frequency <sup>1,2,3</sup>					
Input Frequency	$F_{IN}$	0.008		800	MHz
Capture Range	APR	±40			ppm
Output Frequency	$F_{OUT}$	1.544		1000	MHz
Supply					
Voltage <sup>2,3</sup>	$V_{CC}$	3.13	3.3	3.46	V
Current (No Load) <sup>3</sup>	$I_{CC}$		60	100	mA
Input Signal <sup>2,3</sup>					
LVC MOS	$F_{IN}$		CMOS		
LVDS	$F_{IN}$		LVDS		
LVPECL	$F_{IN}$		LVPECL		
LVC MOS Output (Option A) <sup>2,3</sup>			LVC MOS		
Differential Output (Options C and D) <sup>2,3,4,5</sup>					
Mid Level - LVPECL		$V_{CC}-1.4$	$V_{CC}-1.25$	$V_{CC}-1.0$	V
Swing - LVPECL		450	600	950	mV p-p
Mid Level - LVDS		$V_{CC}-2.4$	$V_{CC}-2.3$	$V_{CC}-2.5$	V
Swing - LVDS		250	410	450	mV p-p
Rise Time	$t_R$		0.5		ns
Fall Time	$t_F$		0.5		ns
Symmetry	SYM	45	50	55	%
SSB Phase Noise, $F_{out} = 155.52/622.08$ <sup>5,6</sup>					
10Hz Offset	$\Phi_n$		-64/-27		dBc/Hz
100Hz Offset	$\Phi_n$		-95/-55		dBc/Hz
1kHz Offset	$\Phi_n$		-123/-123		dBc/Hz
10kHz Offset	$\Phi_n$		-143/-110		dBc/Hz
100kHz Offset	$\Phi_n$		-146/-130		dBc/Hz
1 MHz Offset	$\Phi_n$		-146/-146		dBc/Hz
10 MHz Offset	$\Phi_n$		-146/-146		dBc/Hz
Jitter Generation <sup>5,6</sup>					
155.52 MHz (12kHz - 20MHz BW)	$\Phi_J$		0.30		ps RMS
622.08 MHz (12kHz - 20 MHz BW)	$\Phi_J$		0.12		ps RMS
Operating Temperature (Options T of E) <sup>1,3</sup>	$T_{OP}$	0 to 70 or -40 to 85			°C

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 2).
3. Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 3).
5. Not tested in production, guaranteed by design, verified at qualification.
6. The FX-400 phase noise and jitter performance can be optimized for specific applications. Please consult with Vectron's Application Engineers for more information.

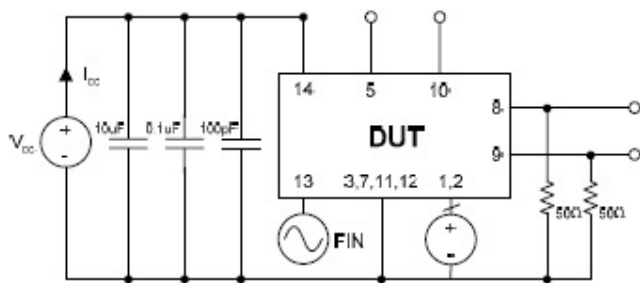


Figure 2. Test Circuit

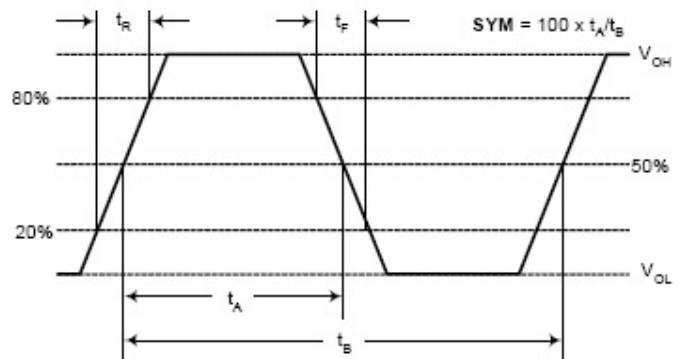


Figure 3. LVPECL Waveform

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

**Table 2. Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
Power Supply	$V_{DD}$	6	V
Storage Temperature	$T_{STR}$	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260/40	°C/sec

## Reliability

The FX-400 is capable of meeting the following qualification tests

**Table 3. Environmental Compliance**

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

## Handling Precautions

Although ESD protection circuitry has been designed into the the FX-400, proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance=1.5Kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes

**Table 4. Predicted ESD Ratings**

Model	Minimum	Conditions
Human Body Model	500 V	MIL-STD 883, Method 3015
Charged Device Model	500 V	JEDEC, JESD22-C101

## Reflow Profile

**Table 5. Reflow Profile (IPC/JEDEC J-STD-020C)**

Parameter	Symbol	Value
PreHeat Time	$t_s$	60 sec Min, 180 sec Max
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$t_{AMB-P}$	480 sec Max
Time At 260 °C	$t_p$	20 sec Min, 40 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

The FX-400 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-400 should not be subjected to a wash process that will immerse it in solvents. NO CLEAN is the recommended procedure. The FX-400 has been designed for pick and place reflow soldering. The FX-400 may be reflowed once and should not be reflowed in the inverted position.

Terminal Plating: ENIG per IPC-4552  
 Electroless Ni = 3 - 6  $\mu$ m  
 Immersion Au = 0.05  $\mu$ m Min

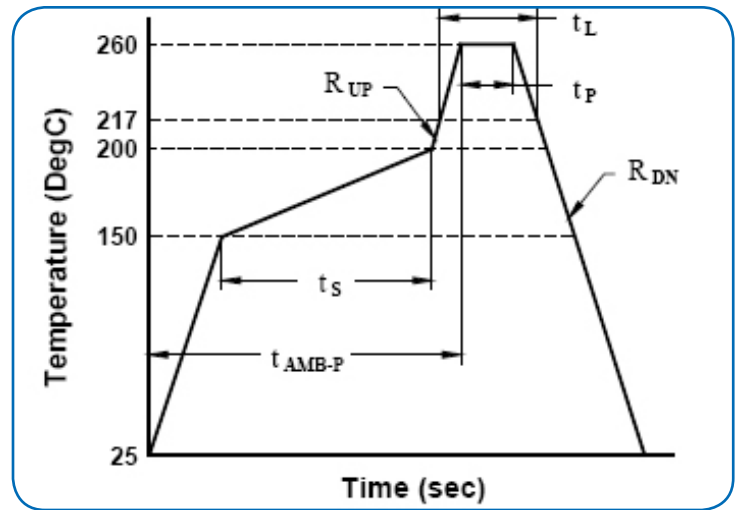


Figure 4. Suggested IR Profile

## Tape and Reel

**Table 6. Tape and Reel Information**

Tape Dimensions (mm)					Reel Dimensions (mm)							
W	F	Do	Po	P1	A	B	C	D	N	W1	W2	#/Reel
44	20.2	1.5	4	20	330	1.5	13	20.2	100	44.4	50.4	200

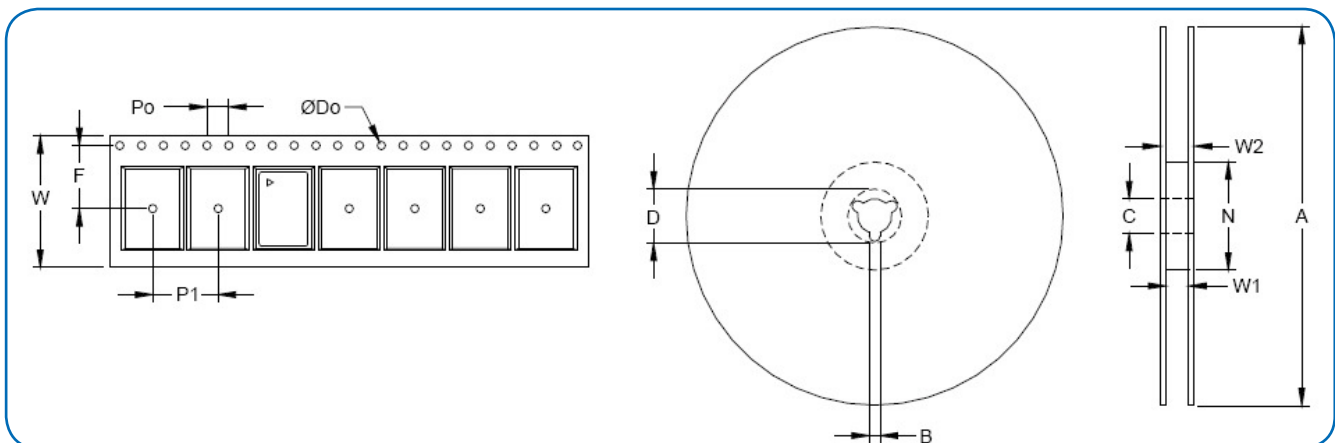


Figure 5. Tape and Reel

# FX-400 Low Jitter Frequency Translator

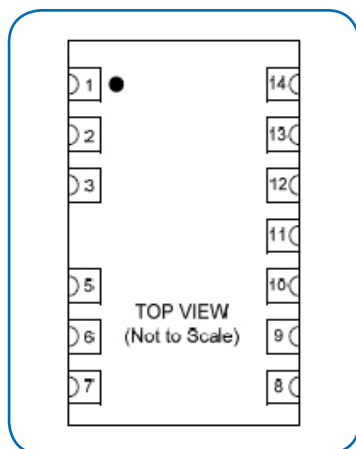


Figure 6. Pin Configuration

Table 7. Pin Functions				
Pin #	Symbol	I/O	Level	Function
1	SEL0	I	LVC MOS	Frequency Select * (See Table 8)
2	SEL1	I	LVC MOS	Frequency Select * (See Table 8)
3	GND	GND	Supply	Case and Electrical Ground
4				Not present
5	VMON	O		VCXO Control Voltage Monitor Under locked conditions VMON should be > 0.3V and < 3.0V. The input frequency may be out of range if the voltage exceeds these levels
6	OD	I	LVC MOS	Output Disable Disabled = Logic "1" Enabled = Logic "0" or no connect
7	GND	GND	Supply	Case and Electrical Ground
8	FOUT	O	LCPECL, LVDS or LVC MOS	Frequency Output
9	CFOUT	O	LVPECL, LVDS or LVC MOS	Complementary Frequency Output – Note for LVC MOS option this pad will be tied to GND.
10	LD	O	LVC MOS	Lock Detect Locked = Logic "1" Loss of Signal = Logic "0"
11	GND	GND	Supply	Case and Electrical Ground
12	GND	GND	Supply	Case and Electrical Ground
13	FIN	I	LVC MOS or LVPECL	Input Frequency – AC Coupled
14	VCC	VCC	Supply	Power Supply Voltage (3.3 V ±5%)

\*For applications requiring two to four input frequencies, Vectron will assign a unique part number and the Input Frequency versus SEL[1:0] settings will be provided in a Specification Control Drawing. For single input configurations it is recommended that SEL0 and SEL1 are tied to ground.

Table 8. Control Logic (LVC MOS)		
SEL0	SEL1	Reference Clock Input
0	0	F <sub>1</sub>
0	1	F <sub>2</sub>
1	0	F <sub>3</sub>
1	1	F <sub>4</sub>

FX-400 Outline Diagram and Pad Layout

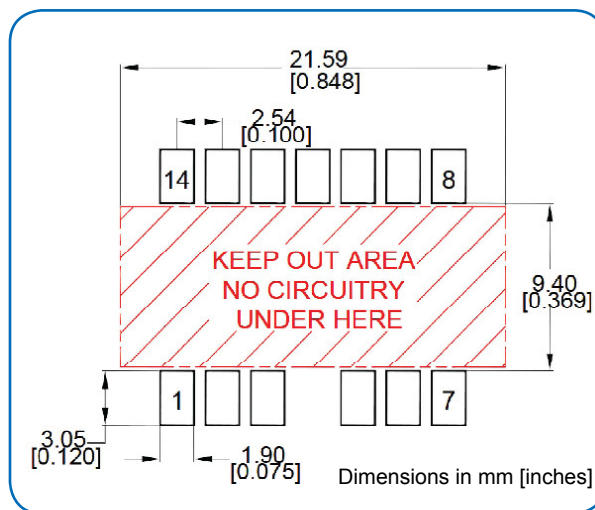
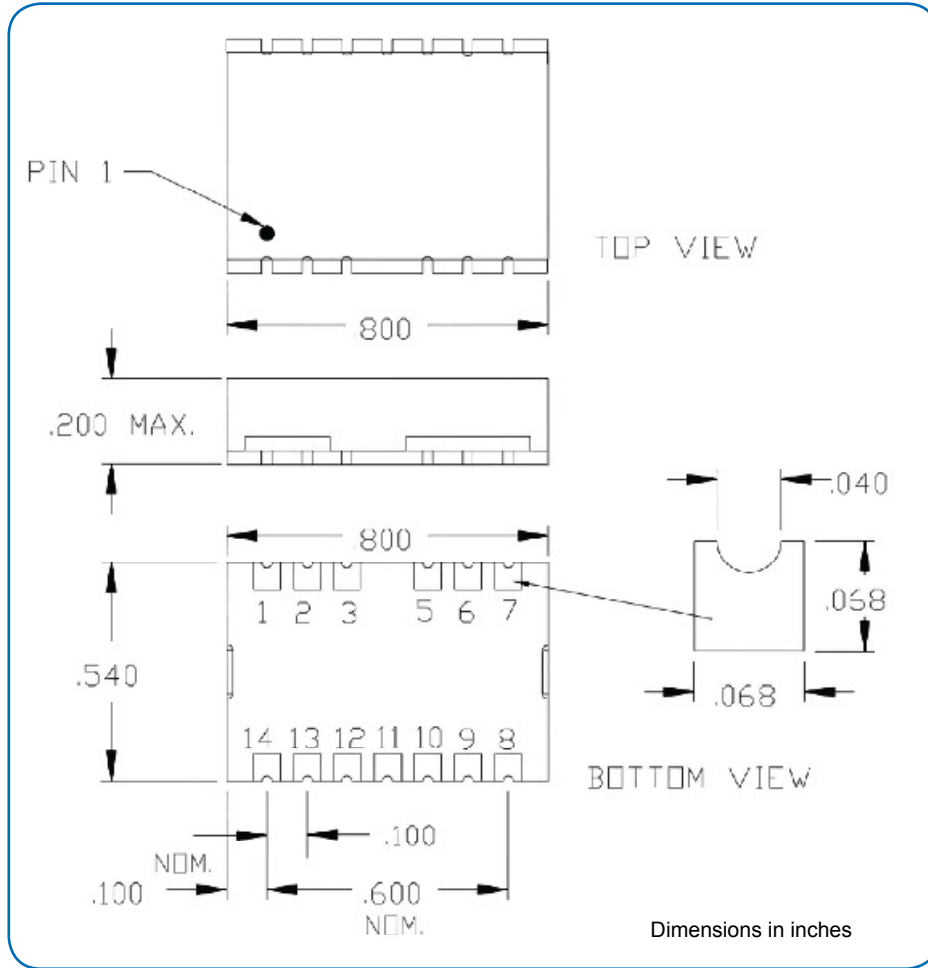


Figure 7. Outline and Pad Layout

Suggested Output Load Configurations

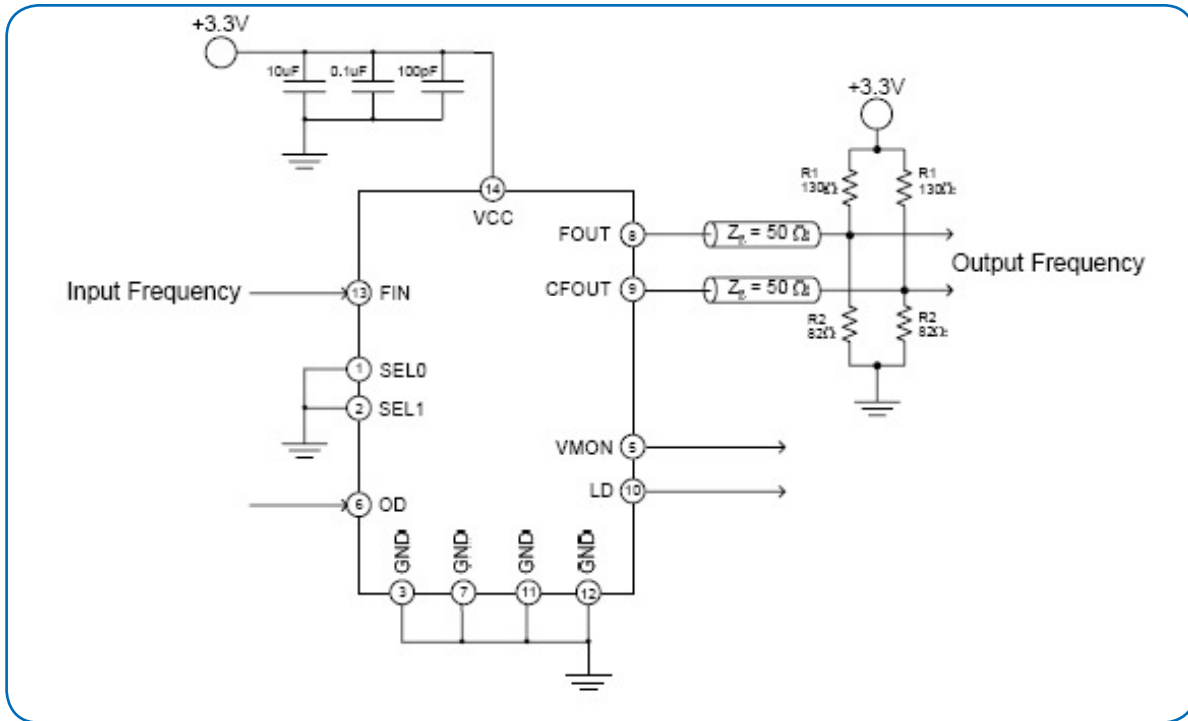


Figure 8. Single Input Frequency Translation - LVPECL Termination

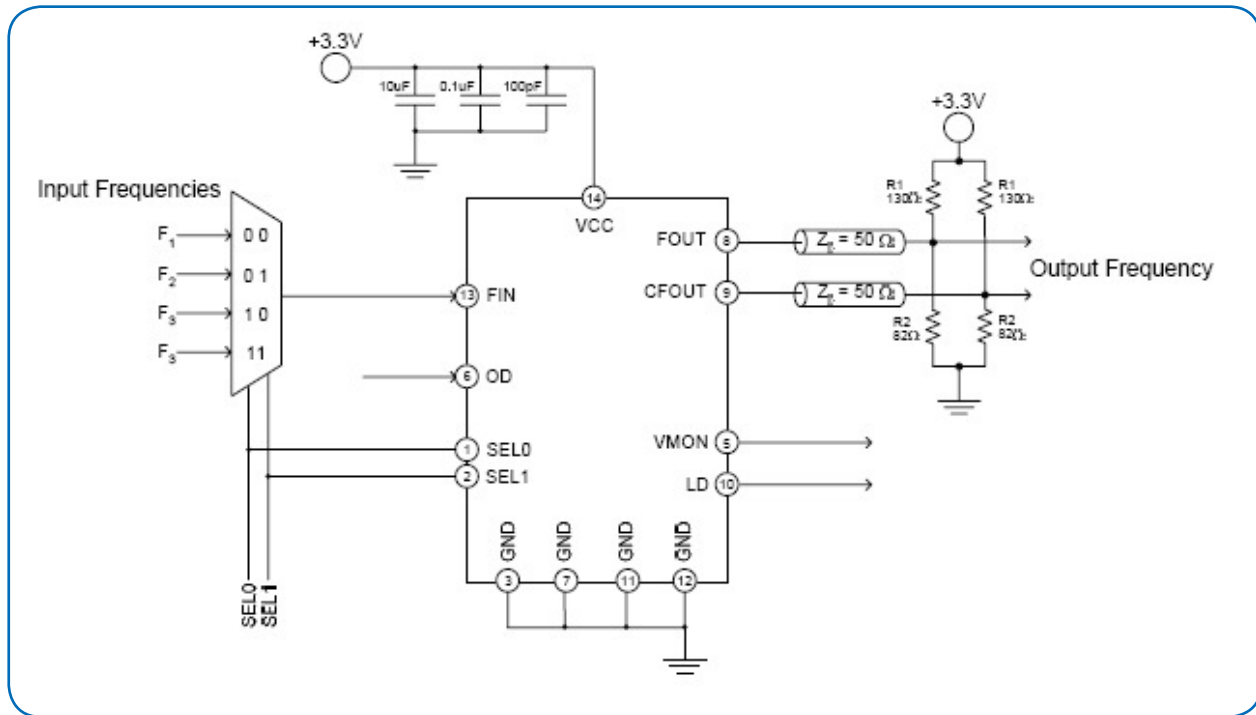


Figure 9. Four Input Frequencies Translated to Common Output Frequency - LVPECL Termination

# FX-400 Low Jitter Frequency Translator

0.08000000	A9	6.31200000	C7	20.00000000	E2	39.84375000	HJ	65.53600000	J6	153.60000000	MA	334.66330000	RB	673.45660000	RA
0.10000000	AH	6.48000000	C2	20.14160000	E3	40.00000000	JF	66.00000000	JA	155.52000000	M2	336.08135000	RC	684.25540000	R9
0.12800000	AX	6.75000000	CB	20.48000000	E4	40.28306300	KK	70.00000000	KB	156.25000000	M3	351.90000000	W1	687.70000000	TV
0.24300000	A8	7.68000000	C9	20.54443400	EF	40.96000000	J1	70.65600000	KC	159.37500000	M7	353.67635000	RD	690.56919600	R4
0.25600000	AM	7.77600000	C5	20.71350000	E1	41.08888700	KM	71.61000000	KF	160.00000000	M1	368.64000000	RY	693.46875000	RV
0.32000000	AW	8.19200000	C3	20.82857200	EG	41.65714400	KP	73.72800000	K8	161.13281300	M4	375.00000000	RF	693.48299100	R6
0.38400000	AY	9.21600000	CH	20.82860000	EB	41.66000000	LM	74.12500000	K1	164.35547500	M9	382.80000000	RU	693.75000000	R8
0.40000000	AF	9.72000000	C8	20.91654600	EH	41.83291300	KT	74.17580000	KA	166.62857200	M5	400.00000000	RR	696.39062500	RW
0.48000000	AK	9.75000000	CE	21.00508400	EJ	42.00000000	JB	74.25000000	K7	167.33164600	N2	409.60000000	RE	696.42147800	V1
0.50000000	BP	9.83040000	C1	22.00000000	E9	42.01016900	KV	75.00000000	KH	168.04067800	N3	491.52000000	PM	696.42187500	TY
0.51200000	AJ	10.00000000	C4	22.10477200	EK	42.50000000	JC	76.80000000	K4	170.00000000	N4	500.00000000	RK	704.38060000	TG
0.65545000	AE	10.23000000	DP	22.21710000	E5	42.66000000	JZ	77.76000000	K2	172.50000000	NU	505.00000000	V3	707.35270000	TC
0.77200000	AT	10.24000000	DM	22.57920000	E8	44.20954400	KX	78.00000000	LH	173.37074800	ND	531.00000000	PH	707.50000000	V2
0.96000000	A7	10.41428500	DV	24.00000000	EC	44.43430000	LF	78.12500000	K3	173.43750000	NP	531.25000000	P8	710.94860000	T2
1.00000000	BB	10.45822600	DU	24.57600000	E6	44.62180000	JW	78.20000000	LP	176.83817500	NA	568.92860000	PJ	712.52000000	TW
1.02400000	B2	10.48720000	DN	24.70400000	E7	44.73600000	J3	78.64320000	K5	182.01600000	N8	569.19640000	P9	716.57320000	T1
1.21500000	BU	10.94900000	DG	25.00000000	F7	44.92800000	JE	79.68750000	KG	182.85714200	NM	588.00000000	RH	718.75000000	T5
1.22880000	BK	10.95000000	DJ	25.16580000	F8	45.15840000	JG	80.00000000	K9	184.00000000	NG	595.05600000	PL	719.73440000	T3
1.25000000	BG	11.18400000	DF	25.60000000	F6	45.82400000	JM	80.56641300	KJ	184.32000000	NH	600.00000000	PR	737.28000000	TL
1.33330000	BF	12.28800000	D8	25.92000000	F2	46.03794600	LG	82.17773800	KL	187.50000000	N5	614.40000000	RG	739.20000000	TT
1.50000000	BE	12.30768600	DY	26.00000000	F3	46.72000000	JK	82.94400000	K6	195.00000000	N7	622.08000000	P2	742.50000000	V4
1.53600000	BV	12.35200000	D1	27.00000000	F4	46.87500000	JY	83.31428800	KN	200.00000000	NE	624.69380000	PD	748.07090000	T6
1.54400000	B3	12.80000000	D2	27.64800000	FB	48.00000000	JV	83.66582500	KR	200.19200000	N6	624.70480000	P6	750.00000000	T7
1.92000000	B1	13.00000000	D3	28.70400000	F1	49.15200000	J7	84.02033800	KU	201.41602000	N1	625.00000000	P3	768.00000000	TN
2.00000000	B8	13.50000000	DT	29.49120000	F5	49.40800000	J2	86.68537400	LJ	212.50000000	NF	627.32960000	P7	777.60000000	T4
2.04800000	B4	14.83516000	DL	29.50000000	F9	50.00000000	JD	88.41908800	KW	219.42957100	NL	629.98780000	PA	779.56860000	T8
2.30400000	BD	15.00000000	D4	30.00000000	HE	50.04800000	KD	95.70000000	LK	240.00000000	NR	637.50000000	PG	780.88100000	TD
2.45760000	BJ	15.03360000	DR	30.72000000	H1	51.20000000	LL	97.50000000	KE	243.00000000	NC	640.00000000	PN	781.25000000	T9
2.50000000	BM	15.36000000	DW	30.88000000	HF	51.84000000	J4	100.00000000	L8	245.76000000	N9	644.53125000	P4	796.87500000	TB
2.55750000	B9	16.00000000	D9	31.25000000	H8	52.00000000	JP	105.00000000	L6	250.00000000	NT	645.12000000	RJ	800.00000000	TK
3.08800000	B6	16.38400000	D5	32.00000000	H2	53.33000000	JU	106.25000000	L9	252.57142800	NJ	647.23940000	PE	805.66410000	TA
3.24000000	BL	17.18400000	DE	32.76800000	H3	54.74600000	JL	108.00000000	LA	256.00000000	NK	647.25080000	PK	809.06350000	TE
3.25000000	BC	18.43200000	D7	33.00000000	H7	55.00000000	JX	110.00000000	L1	262.14400000	NB	649.97030000	PF	819.20000000	TH
3.37500000	BH	18.52800000	DC	33.33300000	HC	60.00000000	JR	112.00000000	L2	292.57142900	NN	657.42187500	PB	821.77730000	TF
3.84000000	B7	18.75000000	EE	34.36800000	H6	61.38000000	KY	114.00000000	L3	300.00000000	PT	665.62560000	PC	850.00000000	TJ
4.00000000	BN	19.20000000	DD	34.56000000	HB	61.44000000	J5	120.00000000	LC	307.20000000	RX	666.51428600	P5	983.40000000	TU
4.09600000	B5	19.39265800	DX	36.86400000	HG	62.20800000	J8	122.88000000	LB	311.04000000	P1	669.12810000	R2	1,000.00000000	TM
4.19430400	CJ	19.44000000	D6	37.05600000	H4	62.50000000	J9	124.41600000	L7	312.50000000	PU	669.32658200	R3		
5.00000000	C6	19.53125000	DZ	37.12500000	H9	62.91450000	LE	125.00000000	L4	318.75000000	PV	669.64290000	R1		
5.12000000	CD	19.66080000	DB	37.50000000	HK	63.36000000	JJ	130.00000000	LD	320.00000000	PP	670.83860000	R7		
6.14400000	CG	19.69896800	DK	38.88000000	H5	63.89760000	JN	139.26400000	L5	322.26565000	PW	672.00000000	RT		
6.29140000	CC	19.71900000	DH	39.06250000	HH	64.00000000	JT	150.00000000	M8	328.71095000	PX	672.15625000	TX		
6.29145600	CF	19.92187500	ED	39.32160000	HD	64.15200000	JH	150.14400000	M6	333.25715000	PY	672.16271200	R5		



## Ordering Information

# FX-400-EAE-KNNN-XX-XX

**Product Family**

FX: Frequency Translator

**Package**

400: 20.3 13.0 5.1mm

**Input**

E: 3.3 Vdc ±10%

**Output**

A: LVCMOS

C: LVPECL

D: LVDS

**Operating Temperature**

E: -40 to 85 °C

T: 0 to 70 °C

**Output Frequency**  
(See Above)

**Input Frequency**  
(See Above)

Factory Use

Factory Use

Factory Use

**Absolute Pull Range**

K: ± 50 ppm

S: ± 100 ppm

- For non-listed frequencies and/or multiple input frequencies a unique part number will be assigned with the following format FX-400-XXX-SNNNN. "SNNNN" is the SCD number.

## For Additional Information, Please Contact

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# FX-400 Low Jitter Frequency Translator

Revision History		
Date	Approved	Description
15Jun2011	CH	Updated frequency code table
10Jun2011	BW	Updated frequency code table
18Feb2011	BW	Terminal Plating thickness added to page 4