Please review the following regarding your two PLL's SFX-524-CRNx

SFX-524-CRN1 Exact frequency is 40.0787 MHz in and out. PLL BW is 50 Hz.

System	
Min Freq	40.0MHz
Max Freq	40.0MHz
Channel Spc.	160.0kHz
PD Freq.	160kHz
Design Freq	40.0MHz
Reference	custom
Frequency	40.0MHz
Phase Noise	None
VCO	custom
Tuning Law	Kv (ideal)
Input Cap.	0F
Phase Noise	None
Chip	ADF4111
Mode	Normal
Main Divider	
Ref Divider	
Phase Detector	Charge Pump
Lock Detect	Dig. Filter
Speedup Mode	None
Loop Filter	CPP_3C
Specify:	Phase Margin
Loop Bandwidth	50.0 Hz
Phase Margin	70.0 deg
Zero Loc.	6.27 Hz
Pole Loc.	399 Hz
Last Pole	500 Hz
C1	67.7nF
R1	5.34k
C2	4.76uF
R2	406k
C3	877pF
Lock Detect	Dig. Filter
FreqDomain	
Min Freq	1.00 Hz
Max Freq	10.0kHz
Pts per Decade	10
Analysis at	40.0MHz
TimeDomain	
Type	Power On
Frequency	40.0MHz
Stop Time	300ms
Max Time Step	200ns

ADF4111 design for 40M ref 40M out 50Hz Bw 70deg mrgn 160kPFD.pll analysed at 08/26/13 14:35:48

PLL Chip is ADF4111
VCO is custom
Reference is custom

Loop Filter designed at a VCO frequency of 40.0MHz with a Kv of 3.00kHz/V

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 40MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-112.9	--	--	-118.2	-114.3
1.00k	-142.8	--	--	-154.5	-143.1
10.0k	-182.3	--	--	-213.0	-182.3
100k	-222.3	--	--	-273.0	-222.3
1.00M	-262.3	--	--	-300.0	-262.3

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Fractional-N Spur Estimate (worst case)

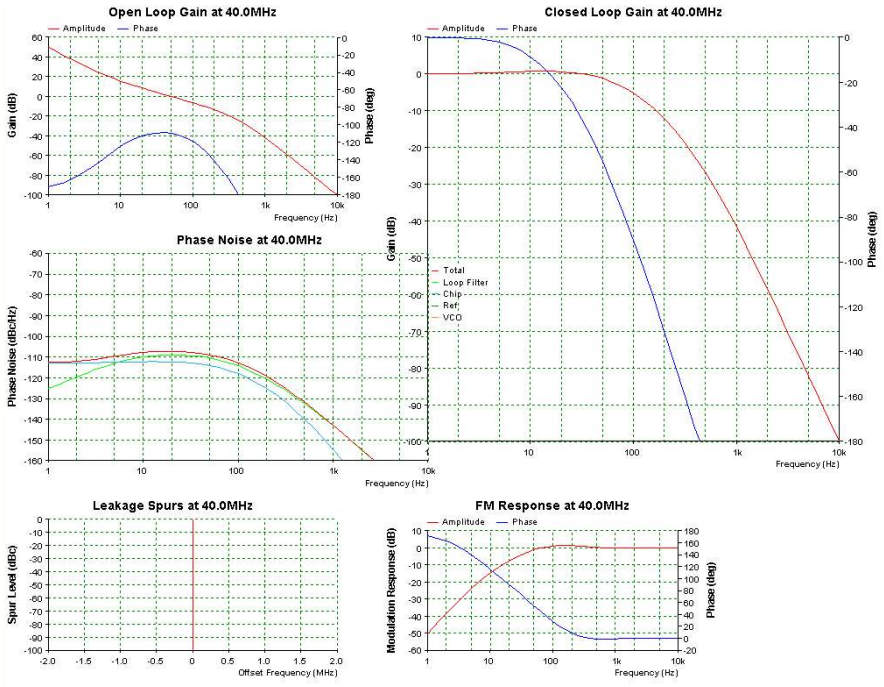
---- End of Frequency Domain Results ----

Transient Analysis of PLL
Power up transient to frequency of 40MHz
Simulation run for 300ms

Frequency Locking
Time to lock to 1.00kHz is 4.01ms
Time to lock to 10.0 Hz is 97.5ms

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 143ms
Time to lock to 1.00 deg is 193ms

Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 75.5ms



SFX-524-CRN2 Exact frequency is 320.6296 MHz in and out. PLL BW is 200 Hz.

System	
Min Freq	320MHz
Max Freq	320MHz
Channel Spc.	320.0kHz
PD Freq.	320kHz
Design Freq.	320MHz
Reference	custom
Frequency	40.0MHz
Phase Noise	None
VCO	custom
Tuning Law	Kv (ideal)
Input Cap.	0F
Phase Noise	None
Chip	ADF4111
Mode	Normal
Main Divider	
Ref Divider	
Phase Detector	Charge Pump
Lock Detect	Dig. Filter
Speedup Mode	None
Loop Filter	CPP_3C
Specify:	Phase Margin
Loop Bandwidth	200 Hz
Phase Margin	67.0 deg
Zero Loc.	30.4 Hz
Pole Loc.	1.32kHz
Last Pole	2.00kHz
C1	9.32nF
R1	10.7k
C2	488nF
R2	235k
C3	418pF
Lock Detect	Dig. Filter

ADF4111 design for 40M ref 320M out 200Hz Bw 67deg mrgn 320kPFD.pll analysed at 08/26/13 14:52:24

PLL Chip is ADF4111
VCO is custom
Reference is custom

Loop Filter designed at a VCO frequency of 320MHz with a Kv of 24.0kHz/V

Frequency Domain Analysis of PLL
Analysis at PLL output frequency of 320MHz

Phase Noise Table

Freq	Total	VCO	Ref	Chip	Filter
100	-96.54	--	--	-97.18	-105.1
1.00k	-112.7	--	--	-113.6	-119.9
10.0k	-155.0	--	--	-163.7	-155.6
100k	-195.5	--	--	-223.5	-195.5
1.00M	-235.5	--	--	-283.4	-235.5

Reference Spurious
Noise and Jitter Calculations include the first 10 ref spurs
First three spurs: -300 dBc -300 dBc -300 dBc

Fractional-N Spur Estimate (worst case)

---- End of Frequency Domain Results ----

Transient Analysis of PLL
Power up transient to frequency of 320MHz
Simulation run for 50.0ms

Frequency Locking
Time to lock to 1.00kHz is 9.75ms
Time to lock to 10.0 Hz is 29.6ms

Phase Locking (VCO Output Phase)
Time to lock to 10.0 deg is 31.5ms
Time to lock to 1.00 deg is 41.5ms

Lock Detect Threshold
Time to lock detect exceeds 2.50 V is 9.30ms