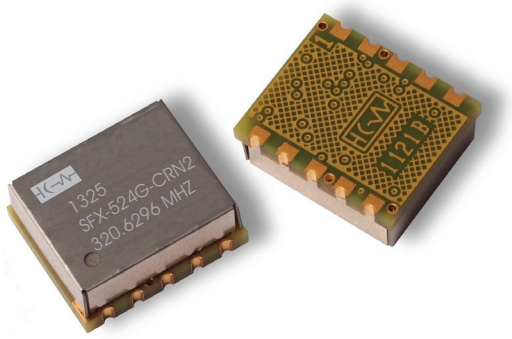
ADVANCED

SFX-524G-CRN1
SFX-524G-CRN2
Synchronous Clock Generators

CONNOR WINFIELD

PLL

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
www.conwin.com



Applications

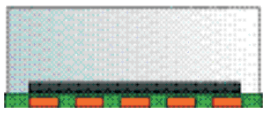
SONET / SDH / ATM
DWDM / FDM
FEC (Forward Error Correction)

Features

- 3.3V High Precision PLL
- Jitter Generation OC-192 Compliant
- Surface Mount
- Inputs Compatible with CMOS or LVPECL Logic
- Inputs Frequency: 40.0787 MHz
- Frequency Translation 40.0787 MHz to 320.6296 MHz
- Alarm detection for Loss of Lock/ Loss of Reference condition
- Space-Saving 12x14mm Leadless Package
- ROHS Compliant / Lead Free

ADVANCED

RoHS COMPLIANT



Bulletin	SG193
Revision	A01
Date	27 Jun 2013

General Description

The SFX-524G-CRN1 and SFX-524G-CRN2 are high precision frequency translator that translates an input 40.0787 MHz, to output frequency of 40.0787 MHz or 320.6296 MHz. The SFX-524G supports all major FEC rates such as 15/14, 255/237 etc.

SFX-524G-CRNx is well suited for use in line cards, service termination cards and similar functions to provide reliable reference, phase locked, synchronization for TDM, PDH, SONET and SDH network equipment. The SFX-524G-CRNx provides a jitter filtered, wander following output signal synchronized to a superior Stratum or peer input reference signal.

The SFX-524G-CRNx includes a lock detect alarm output.

Parts are assembled using high temperature solder to withstand surface mount reflow process. This product is compliant with all required ROHS specifications.

Absolute Maximum Rating

Table 1

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vcc	Power Supply Voltage	-0.3	-	4.0	Volts	
VI	Input Voltage	-0.2	-	Vcc +0.3V	Volts	
Ts	Storage Temperature	-55	-	125	°C	

Absolute Ratings: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only. The functional operation of the device at those or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to conditions outside the "recommended operating conditions" for any extended period of time may adversely impact device reliability and result in failures not covered by warranty.

Specifications

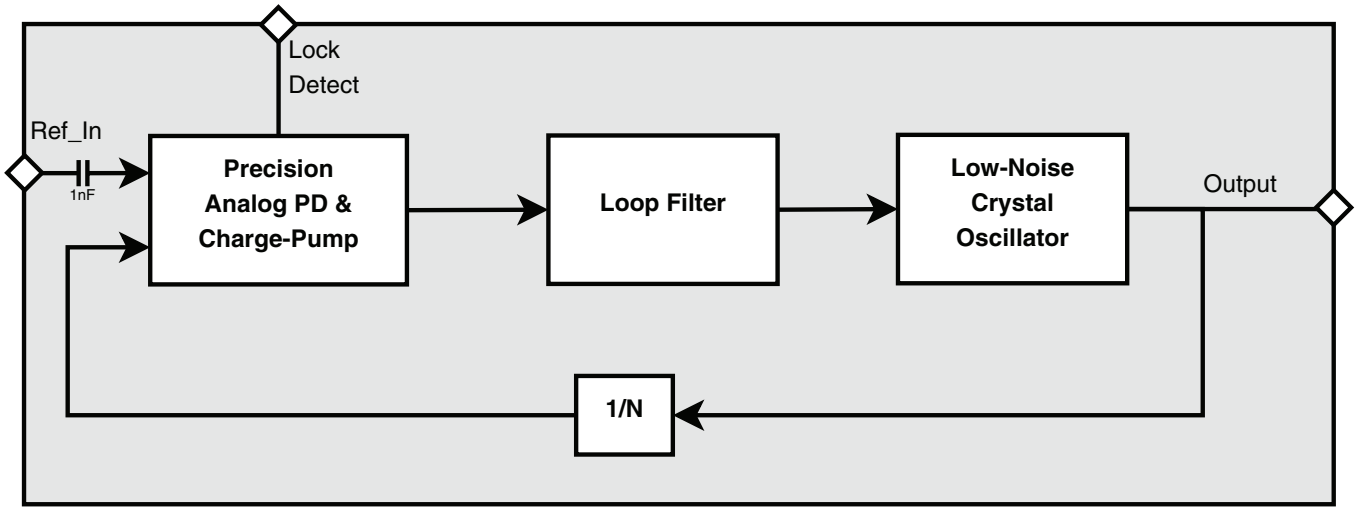
Table 2

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
f_{IN}	Input Frequency	-	40.0787	-	MHz	
f_{OUT}	SFX-524G-CRN1 Output Frequencies (LVPECL)	-	40.0787	-	MHz	
	SFX-524G-CRN2 Output Frequencies (LVPECL)	-	320.6296	-	MHz	
Vcc	Supply Voltage (3.3 V_{DC})	3.13	3.3	3.46	Volts	
I_{CC}	Supply Current	-	80	-	mA	
F_{IN} Input Characteristics						
V_{FIN}	Input Voltage	0.8	-	3.3	Vpp	1.0
F_{OUT} SFX-524G-CRNx LVPECL OUTPUT						
V_{FOUT}	Differential Output Voltage	-	0.65	-	Volts	2.0, 3.0
T_R/T_F	Rise/Fall Time @20% to 80%	-	0.6	1.5	ns	
SYM	Output Symmetry	45		55	%	
J_{GEN2}	Jitter Generation RMS (12 kHz - 20 MHz)	-	0.60	1.0	ps	4.0
J_{TRAN}	Jitter Transfer Function	-	-	0.1	dB	5.0
TF	Input Frequency Tracking	±40	-		ppm	
T_{OP}	Operating Temperature	0	-	85	°C	
SSB Phase Noise (for SFX-524G-CRN2-320.6296M)						
	@ 10Hz offset	-	-57	-45	dBc/Hz	
	@ 100Hz offset	-	-92	-80	dBc/Hz	
	@ 1kHz offset	-	-110	-100	dBc/Hz	
	@ 10kHz offset	-	-118	-115	dBc/Hz	
	@ 100kHz offset	-	-122	-118	dBc/Hz	
	@ 1MHz offset	-	-128	-125	dBc/Hz	
	@ 10MHz offset	-	-146	-143	dBc/Hz	
	@ 20MHz offset	-	-147	-145	dBc/Hz	
$\emptyset_{OFF}$	Phase Offset	-	5	15	ns	6.0
$\emptyset_{DYN}$	Dynamic Phase Offset	-	-	1	ns	7.0

NOTES:
1.0: F_{IN} is internally AC-coupled
2.0: Internally biased. External AC-coupling capacitor recommended. Please see Figure 2 for recommended connection diagram.
3.0: V_{FOUT} is the voltage difference between F_{OUT} and CF_{OUT}
4.0: Based on the VCXO used.
5.0: GR-253-CORE, Sec. 5.6.2.1.2
6.0: $\emptyset_{OFF}$ must be <15ns for >3 consecutive cycles for Lock Detect to be set high. One high, any cycle with $\emptyset_{OFF}$ >25ns will reset Lock Detect.
7.0: Change in phase offset over temperature, relative to 25°C

Functional Block Diagram

Figure 1



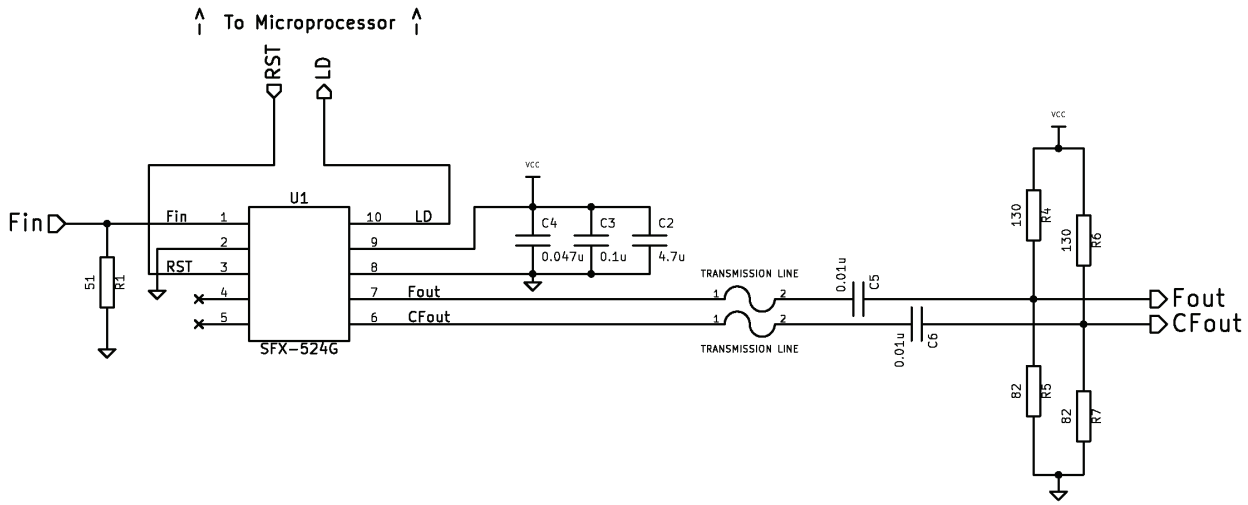
Pin Description

Table 3

PIN #	SYMBOL	I/O	Level	Function
1	FIN	I	LVPECL or LVCMOS	Input Frequency Note: Input is AC coupled for handling either LVCMOS or LVPECL input signals
2	GND	GND	Supply	Ground
3	RST	I	LVCMOS	Active Low Reset
4		N/C	N/A	Do Not Connect
5		N/C	N/A	Do Not Connect
6	FOUT	O	LVPECL	Frequency Output
7	CFOUT	O	LVPECL	Complementary Frequency Output
8	GND	GND	Supply	Ground
9	VCC	VCC	Supply	Power Supply Voltage (3.3V ±5%)
10	LD	O	LVCMOS	Lock Detect Locked = Logic 1 Loss of Signal = Logic 0

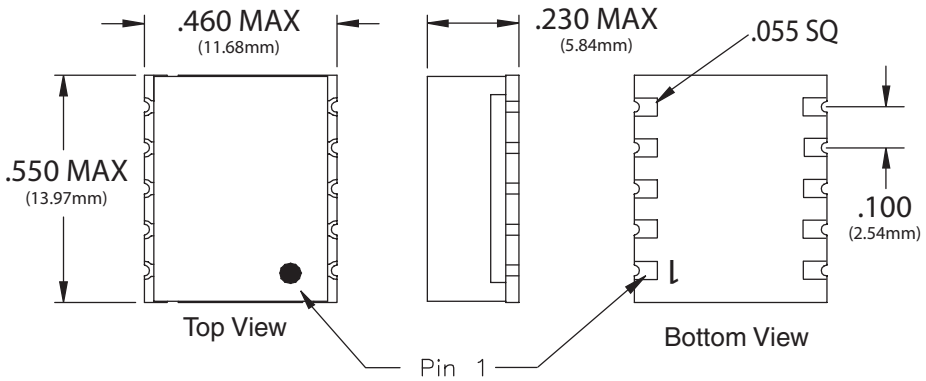
Output Load and Power Supply Filtering Recommendations

Figure 2



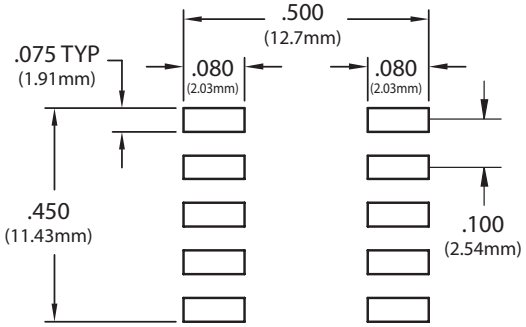
Package Dimensions

Figure 3



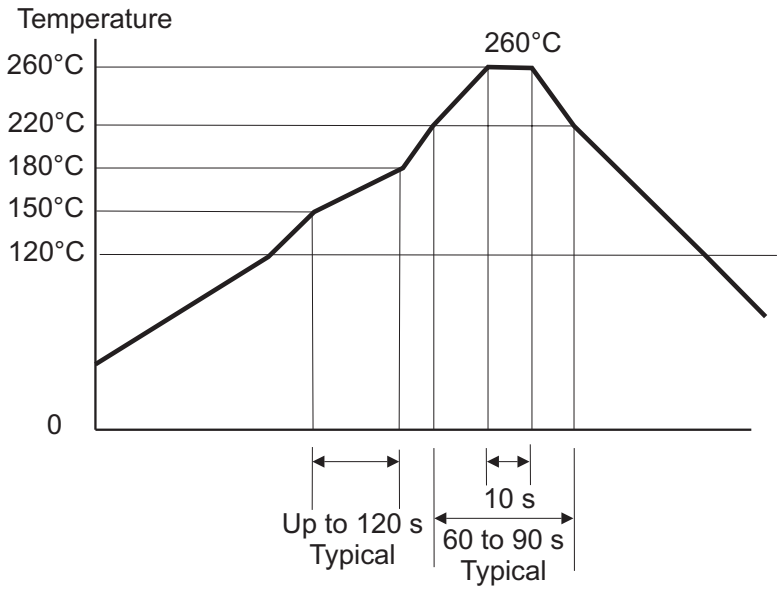
Recommended Footprint Dimensions

Figure 4



Solder Profile

Figure 5



Meets IPC/JEDEC J-STD-020C

Standard Frequencies

Table 4

Model	Input F_{IN}	Output F_{OUT}	Bandwidth
SFX-524G-CRN1	40.0787 MHz	40.0787 MHz	45 - 50 Hz
SFX-524G-CRN2	40.0787 MHz	320.6296 MHz	150 - 200 Hz

Ordering Information

SFX-524G-CRN1-040.0787M or SFX-524G-CRN2-320.6296M

Revision	Date	Note
A00	06/11/13	Advanced Released.
A01	06/27/13	Data sheet corrections.