Emulating the GLink Chip Set With FPGA Serial Transceivers in the ATLAS Level-1 Muon Trigger

Alberto Aloisio, Francesco Cevenini, Raffaele Giordano, and Vincenzo Izzo

***Abstract*—Many high energy physics experiments based their serial links on the Agilent HDMP-1032/34A serializer/deserializer chip-set (or GLink). This success was mainly due to the fact that this pair of chips was able to transfer data at $\sim$ 1 Gb/s with a deterministic latency, fixed after each power up or reset of the link. Despite this unique timing feature, Agilent discontinued the production and no compatible commercial off-the-shelf chip-sets are available. The ATLAS Level-1 Muon trigger includes some serial links based on GLink in order to transfer data from the detector to the counting room. The transmission side of the links will not be upgraded, however a replacement for the receivers in the counting room in case of failures is needed. In this paper, we present a solution to replace GLink transmitters and/or receivers. Our design is based on the gigabit serial IO (GTP) embedded in a Xilinx Virtex 5 Field Programmable Gate Array (FPGA). We present the architecture and we discuss parameters of the implementation such as latency and resource occupation. We compare the GLink chip-set and the GTP-based emulator in terms of latency, eye diagram and power dissipation.**

***Index Terms*—Fixed latency, FPGAs, serial links.**

I. Introduction

TRIGGER systems of high energy physics (HEP) experiments need data transfers to be executed with fixed latency, in order to preserve the timing information. This requirement is not necessarily satisfied by Serializer–Deserializer (SerDes) chip-sets, which can have latency variations in terms of integer numbers of unit intervals (UIs) and/or of clock cycles of the parallel domain. For instance, the TLK2711A [1] exhibits latency variations up to 31 UIs on the receiver data-path. The Gigabit link, or GLink, chip-set [2], produced by Agilent, was able to transfer data at data-rates up to 1 Gb/s with a fixed latency even after a power-cycle or a loss of lock. Serial links of data acquisition systems of HEP experiments have been often based on the GLink chip-set. For instance it has been deployed in the Alice, ATLAS, Babar [3], CDF, CMS, D0, and Nemo [4] experiments (just to cite some of them). The chip-set became so widely used, that CERN produced a radiation hard serializer compatible with it [5]. Unfortunately, a few years ago Agilent discontinued the production of the chip-set and users needing replacements are looking for alternative solutions. Latest FPGAs include embedded multi-Gigabit SerDes, which offer a wide variety of configurable features. The benefit from the integration of such a device in FPGA is in terms of power consumption, size, board layout complexity, cost and re-programmability. The Level-1 Barrel Muon Trigger of the ATLAS experiment includes GLink serial links in order to transfer data from the detector to the counting room. The transmission side of the links is on-detector and will unlikely be upgraded, however a replacement for the receivers in the counting room in case of failures is needed. We developed a replacement solution for GLink transmitters and receivers, based on the gigabit serial IO (GTP) embedded in Xilinx Virtex 5 Field Programmable Gate Array (FPGA). Our solution preserves the fixed-latency feature of the original chip-set. In the coming sections we will introduce the present L1 barrel muon trigger and the GLink chip-set, then we will describe the architecture and the implementation of our design. Finally, we will present some test results about our emulator, comparing them also with the GLink chip-set.

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A. Aloisio, F. Cevenini and R. Giordano are with the INFN Sezione di Napoli and Università degli Studi di Napoli "Federico II," Dipartimento di Scienze Fisiche, 80126, Napoli, Italy (e-mail: aloisio@na.infn.it; cevenini@na.infn.it; rgiordano@na.infn.it).

V. Izzo is with the INFN Sezione di Napoli, Dipartimento di Scienze Fisiche, 80126, Napoli, Italy (e-mail: izzo@na.infn.it).

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II. Atlas Barrel Muon Trigger and DAQ

The ATLAS detector [6] is installed in one of the four beam-crossing sites at the large Hadron collider (LHC) of CERN. The detector has a cylindrical symmetry and it is centered on the interaction point. ATLAS consists of several subsystems, among them there is a muon spectrometer, which in the barrel region is built in the loops of an air-core toroidal magnet and includes resistive plate chambers (RPCs). RPCs are arranged in towers used for the Level-1 (L1) muon trigger (Fig. 1). The spectrometer is divided in two halves along the axis and each half is in turn divided in 16 sectors. A physical sector is segmented in two trigger sectors, including six or seven RPC towers each.

The whole trigger system is implemented as a synchronous pipeline, with a total latency of 2.0 μs, clocked by the Timing, Trigger and Control (TTC) system [7] of the LHC. The TTC distributes timing information such as the bunch crossing clock (at about 40 MHz) and the L1 trigger.

The read-out and trigger electronics of the barrel muon spectrometer includes an on-detector part and an off-detector one. A board on the detector, the PAD [8], transfers data to a Versa Module Eurocard (VME) board in the counting room, the Sector Logic/RX (SL/RX) [9], via an 800-Mb/s serial link based on the GLink chip-set. Each SL/RX board includes eight GLink receivers and two FPGAs handling the received data and the communication with other off-detector boards.

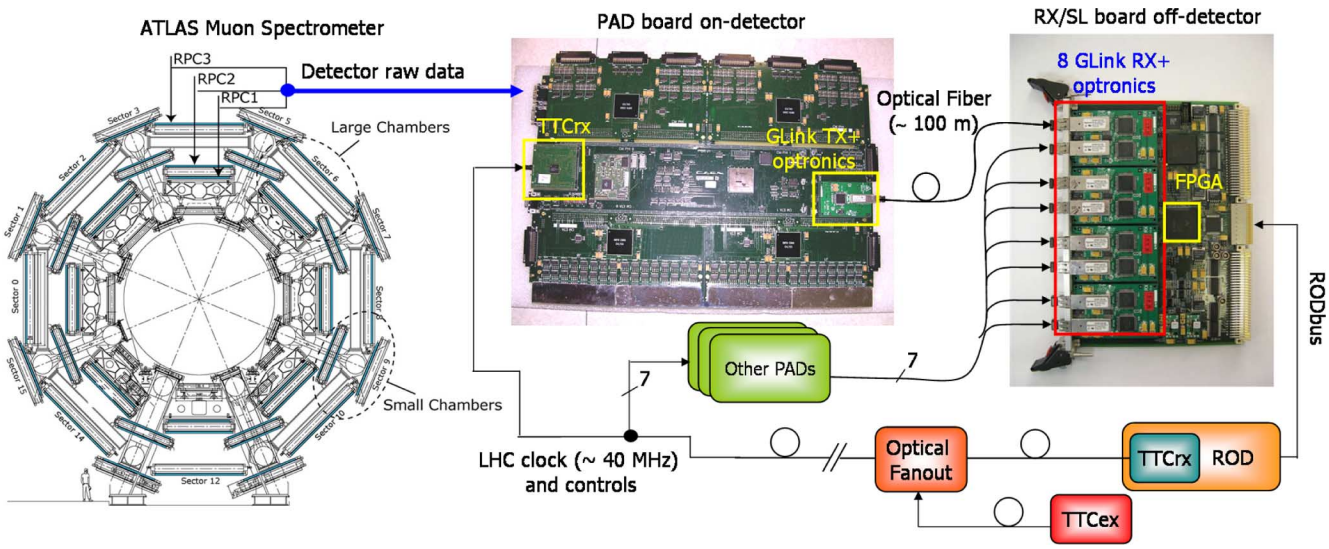

Fig. 1. Left: Cross section of the ATLAS muon spectrometer. Right: Level-1 Trigger and DAQ for the spectrometer.

During the trigger decision, data are stored by the on-detector electronics. If the event is validated, a L1 accept signal is broadcast to the PADs, which transfer data to the RX/SL. The RX/SL board, in turn, sends data to other VME boards for further processing and storage. More information about the ATLAS barrel muon trigger and data acquisition (DAQ) can be found in [10].

III. The GLink Chip-Set

The GLink chip-set consists of a serializer (HDMP-1032A) and a deserializer (HDMP-1034A). The chips work with data-rates up to 1 Gb/s and encode data according to the conditional inversion master transition (CIMT) protocol. In order to read serial data, the receiver extracts a clock from the CIMT stream and locks its phase to the master transition. The recovered clock synchronizes all the internal operations of the receiver and it is available as an output. Received data are transferred out of the device synchronously with the recovered clock and the chip-set architecture is such that the overall link latency is deterministic. Moreover, by means of the dedicated parallel automatic synchronization system (PASS), it is also possible to output data synchronously with a local receiver clock, provided that it has a constant phase relationship with the transmission clock (as is the case in the ATLAS L1 barrel muon trigger, which is clocked by the LHC machine clock).

We now briefly introduce the CIMT encoding protocol. A CIMT stream is a sequence of 20-bit words, each containing 16 data bits (D-Field) and 4 control bits (C-Field). The C-Field flags each word as a data word, a control word or an idle word. Idle words are used in order to synchronize the link at start-up and to keep it phase-locked when no data or control words are transmitted. The protocol guarantees a transition in the middle of the C-Field and the receiver checks for this transition in received data in order to perform word alignment and to detect errors. Two encoding modes are available: one compatible with older chip-sets and an enhanced one, which is more robust against incorrect word alignments. The DC-balance of the link is ensured by sending inverted or unaltered words in such a way to minimize the bit disparity, defined as the difference between the total number of transmitted 1s and 0s. By reading the C-Field content, the receiver is able to determine whether the payload is inverted or not and restore its original form.

IV. GLink Emulation

We built our GLink emulator around the Xilinx GTP transceiver [11], embedded in Virtex 5 [12] FPGAs. Other FPGA vendors offer embedded SerDes, for instance Altera with the GX and Lattice with the flexiPCS. However, the fixed-latency characteristic of our emulator is deeply based on some hardware features of the GTP. For a discussion about the possibility to implement a fixed-latency link with FPGA-embedded SerDes, see [13].

A. Architecture

The GTP can serialize/de-serialize words 8, 16, 10, and 20 bit wide. We configured it to work with 20-bit CIMT-encoded words at 40 MHz, in order to achieve an 800-Mb/s link. The receiver clock has an unknown, but fixed, phase offset with respect to the transmitter clock. In order to transfer data with minimum latency the GTP allows to skip internal elastic buffers, one being in the data-path of the transmitter and the other one in the data-path of the receiver. When skipping buffers, all phase differences must be resolved between the external parallel clock domain and a clock domain internal to the device. We set up the transmitter to work without the elastic buffer, while we left two options for the receiver: the first one without the buffer and with an improved latency (Configuration1), but with some constraints on the relative phase between transmission and reception clocks and the second one without any phase constraint, but with a higher latency (Configuration2).

On the transmitter, a phase control logic instructs the GTP to align the phase of the internal clock to the transmission clock and asserts the Ready signal when done. A dedicated logic encodes incoming 16-bit words into 20-bit CIMT words and transfers them to the GTP (Fig. 2). The encoder is able to send data, control or idle words and supports an input flag bit exactly like the original chip-set.

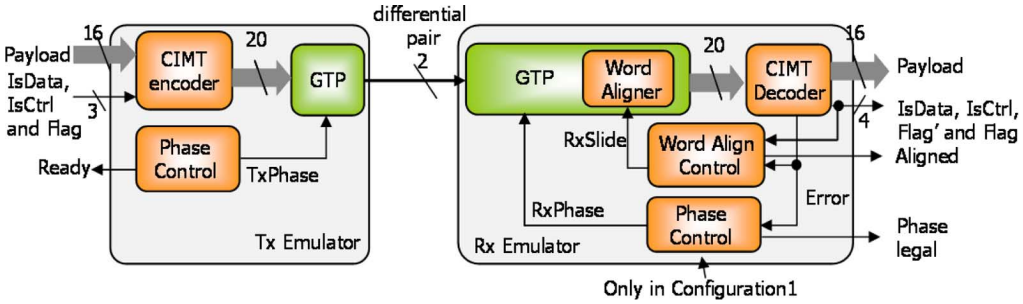

Fig. 2. Simplified block diagram of the emulator.

On the receiver side, when working in Configuration1, the phase align and control logic checks whether or not it is possible to retrieve data from the link with the assigned parallel clock phase. If it is not possible, the phase must be changed either in the FPGA or outside. In Configuration2 every phase offset is legal, therefore no checks are performed. In order to align received data to the correct word boundary, we added to the GTP: a CIMT decoder and a word align control logic. The decoder checks the C-Field of incoming CIMT words and, if it is not valid, flags an error to the word align control logic. When errors are found, the logic activates the shifter inside the GTP, changing the word boundary alignment of parallel data. If, for a defined number of clock cycles, no errors are found, the align control logic assumes parallel data are correctly aligned and asserts the Aligned signal. The decoder determines if the received word is an idle, a control or a data word, extracts the status of the flag and activates the corresponding outputs.

For the sake of completeness, we inform the reader that our emulator supports all the CIMT encoding modes of the HDMP-1032/34A chip-set, but not the 20/21-bit modes of the older HDMP-1022/24.

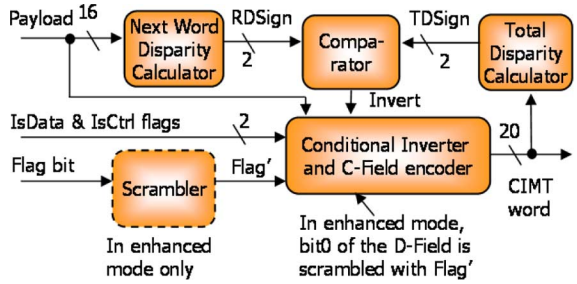

Fig. 3. Simplified block diagram of the encoder.

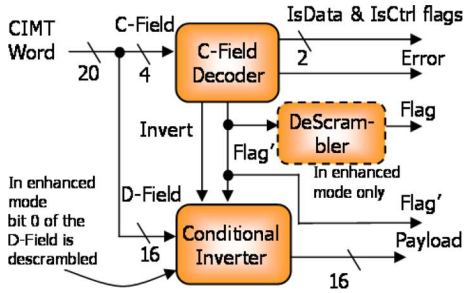

Fig. 4. Simplified block diagram of the decoder.

B. Encoder, Decoder, and Word Align Control Logic

An implementation of a CIMT encoder and a decoder with a word align controller can be derived from the CIMT protocol definition, which is available in the data-sheet of the G-Link chip-set. We will now discuss our implementation and we will present the improvements we added to the word align control logic with respect to the original one.

The encoder (Fig. 3) includes a block, which calculates the bit disparity on the incoming payload and outputs the sign of the disparity on the 2-bit RDSign bus. A "10" flags a majority of 1s, a "01" flags a majority of 0s and a "00" indicates the word has an equal number of 1s and 0s. For each encoded word, the total disparity calculator takes care of updating the total bit disparity of all encoded words and outputs the sign of the bit disparity on the 2-bit TDSign bus. The coding on the bus is the same as the RDSign bus. A comparator checks the RDSign and TDSign buses and if they are equal, it asserts the Invert signal. Another block conditionally inverts the payload bits, according to the Invert signal, thus generating the D-Field, and appends a C-Field to it, composing the CIMT-coded word. For the sake of correctness, we point out that control words include only 14 payload bits and then require the addition of 2 dummy bits. However, the details of the control words encoding add nothing to the discussion and we will not present them here. The C-Field encodes the status of IsData, IsCtrl, Invert and Flag' bits. In basic mode, Flag' equals the input Flag, while in enhanced mode the Flag' is the result of Flag after a scrambling operation. The scrambling is used to have transitions in the logical value of Flag' even if Flag is static. The likelihood of having at least one transition of the Flag' bit in a given number of clock cycles is determined by the scrambling polynomial. This property is then exploited by the word align control logic in the receiver in order to strengthen its error detection capability. For the same reason, the bit #0 of the D-Field is scrambled by means of a XOR operation with Flag'.

The CIMT decoder (Fig. 4) includes a C-Field decoder in order to retrieve IsData, IsCtrl and Flag' bits and to determine whether the D-Field needs to be inverted or not. If the C-Field has invalid value, e.g., if the master transition is missing, the logic asserts the Error signal. A dedicated logic conditionally inverts the D-Field in order to restore the original payload. In enhanced mode, the logic also de-scrambles bit #0 while another logic de-scrambles the Flag' bit.

The word align control logic (Fig. 5) is a finite state machine (FSM) monitoring the Error signal from the decoder. If a number M of consecutive errors are received, the logic as-

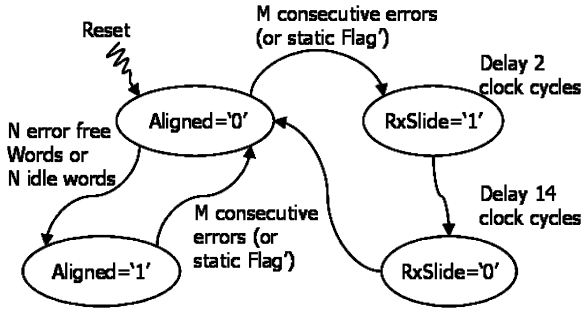

Fig. 5. Simplified bubble diagram of the word align control logic.

sumes the alignment is incorrect and asserts the RxSlide signal for two clock cycles, causing the GTP to shift parallel data by one more bit. Then, the FSM waits for the overall latency of the shifting operation and the CIMT decoder (14 clock cycles) and goes back to its initial state. The parameter M has default value of 2 and is programmable by writing a 8-bit register. In enhanced mode, the control logic also monitors the Flag' signal. If Flag' is static over the last 32 clock cycles, the logic assumes the word alignment is not correct. If after a number N of consecutive words no errors are observed, then the logic assumes the parallel data are correctly aligned to the word boundary and asserts the Aligned signal. The FSM continues monitoring the error signal (and Flag' in enhanced mode) and de-asserts the Aligned output upon the reception of M consecutive errors (or a static Flag' in enhanced mode). The parameter N has a default value of 256 and is programmable by writing a 10-bit register.

With respect to the original implementation we added the programmability of the N and M parameters, which allow the user to stiffen or soften the tolerance of the lock condition to errors. Even if the enhanced mode is more robust against fake lock conditions than the basic one, previous studies on the G-Link chip-set indicated that at start-up the receiver can achieve fake locks if the sent word is not an idle word [14]. In order to solve this problem, we added the optional capability to lock only if a sequence of idle words is received.

C. Physical Implementation

A full-duplex emulator (transmitter and receiver) requires around 500 lookup tables (LUTs) and 400 flip flops (FFs), which are 3% of the logic resources available in a Xilinx Virtex 5 LX50T FPGA (Table I). Such a tiny resource requirement, will allow us to integrate all the eight GLink receivers of the RX/SL board in the FPGA and the impact of this integration will be just a 6% of the fabric resources. The latencies of the transmitter and the receiver are respectively 6.75 and 5.25 parallel clock cycles (6.75 in Configuration2). Details about the contribution of internal blocks are given in Table II. For each component, we report the latencies in terms of clock cycles and the absolute value. For comparison with the latencies of our solution we recall that latencies of the GLink transmitter and receiver are respectively 1.4 and 3.0 parallel clock cycles. Hence, our emulator has a higher latency with respect to the original chip-set, however this is not an issue for our application.

We notice that a GLink receiver dissipates $\sim$ 800 mW and a transmitter $\sim$ 700 mW (typical @ 1 Gb/s). Each GTP pair (transmitter and receiver) dissipates $\sim$ 300 mW (typical @ 3 Gb/s), hence the power dissipation of the emulator is lower than the one of the original chip-set.

TABLE I
RESOURCES USED BY AN IMPLEMENTATION OF A GLINK TRANSMITTER/RECEIVER IN A XILINX VIRTEX 5 LX50T

Resource	Occupied	Percentage	Available
LUTs	651	2.3 %	28,800
Registers	408	1.4 %	28,800
Slices	265	3.7 %	7,200
DCMs	2	17 %	12
GTPs	1	8.3 %	12

TABLE II
LATENCY OF THE BUILDING BLOCKS OF THE LINK (RECEIVER IN CONFIGURATION 1)

	# of clock cycles	Block latency (ns)
Transmitter		
Total Encoding Latency (fabric)	4.5	112.5
Total GTP Latency	2.25	56.25
Total Transmitter Latency	6.75	168.75
Receiver		
Total GTP Latency	4.75	118.75
Total Decoding Latency (fabric)	1	25
Total Receiver Latency	5.25	143.75
Total Link Latency	12	312.5

V. TEST RESULTS

In order to test our link, we deployed two off-the-shelf boards [15] built around a Virtex 5 LX50T FPGA. The boards route the serial I/O pins of one of the GTPs on the FPGA to SubMiniature version A (SMA) connectors. We connected the transmitter and the receiver GTPs with a pair of 5 ns, 50 Ω impedance coaxial cables. Transmitted and received payloads were available on single-ended test-points as well as on low-voltage differential signaling (LVDS) outputs and were monitored by an oscilloscope to observe latency variations. We used a dual channel clock generator providing two 40-MHz clock outputs with a fixed phase offset. This way, we emulated the TTC system of the ATLAS experiment, which is used to clock data in and out from the link.

We checked that our emulator is able to correctly transmit (receive) data toward (from) an Agilent GLink receiver (transmitter) chip in all the encoding modes supported by the HDMP-1032/34A chip-set. In order to perform this test, we deployed a ML-505 board and a custom board hosting a GLink transmitter and a receiver. The test showed that the emulator correctly exchanges data with a GLink chip in both the CIMT encoding modes.

We present an eye diagram comparison between the Agilent GLink transmitter and the GTP (Fig. 6). We fed the transmitters with the same payload, a 16-bit pseudo random word sequence. We probed the signal on the positive line of the differential pair, at

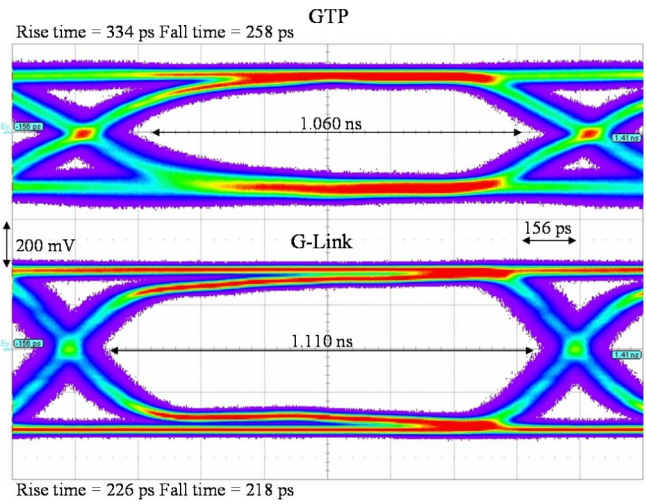

Fig. 6. Eye diagram comparison between GLink and the GTP.

the far end of a 5-ns 50-Ω coaxial cable. Between the transmitter and the cable, there was a 10-nF decoupling capacitor. We terminated the negative line on its characteristic impedance to keep the differential driver balanced. We notice that the GLink eye width is 50-ps wider than GTPs. Despite the GTP smaller voltage swing (400 mV) with respect to GLink (600 mV), the latter has rise and fall times respectively around 30% and 15% lower. The timing jitter on GTP's edges is $\sim$ 210 ps, while for Agilent transmitter is $\sim$ 180 ps. This difference could be due to the fact that the generation of high-speed serial clock, from the 40-MHz oscillator, requires only the internal phase locked loop (PLL) for GLink. Instead, in our clocking scheme for the GTP we deployed a delay locked loop (DLL) of the FPGA to multiply the 40-MHz clock in order to obtain the 80-MHz clock. Therefore, the total jitter on the transmitted serial stream includes the contribution of the jitters of both the PLL and the DLL. Moreover, we used a single ended oscillator to source the PLL of the GTP, while the user guide recommends to use a differential oscillator.

We performed bit error ratio (BER) measurements on the link implemented with our emulator. We deployed a custom bit error ratio tester (BERT) [16], checking the received payload against a local copy and flagging an error when a difference occurred. More than 10^{13} bits have been transferred and no errors have been observed, corresponding to a 10^{-12} BER, estimated with a 99% confidence level [17]. We did not perform BER measurements for a design integrating multiple G-Link receivers in the same FPGA. However, other studies [18] have shown that the GTP has a good tolerance both to the logic activity in the FPGA fabric and to the switching activity of surrounding IOs.

VI. Conclusion

Data-rates and transmission protocols of SerDes embedded in FPGAs can be changed by simply re-programming the device. By suitably configuring a GTP transceiver and adding few logic resources from the FPGA fabric ($\sim$ 3% of the total), we have been able to achieve a complete replacement for the GLink chip-set. Our emulator transfers data with a fixed latency, which was a crucial feature of the original chip-set. We experimentally verified the compatibility of our emulator with GLink both in transmission and reception. Our receiver offers two configuration options: the first one with a shorter internal data-path and with minimum latency, but with some constraints on the relative phase between transmission and reception parallel clocks and the second one without any phase constraint, but with a higher latency. Since the emulator has a tiny footprint in terms of logic resources, in a future upgrade of the RX/SL, it will allow us to integrate all the GLink receivers on the board in a single FPGA, still leaving most of the device resources free for trigger and readout tasks. Hence, the layout of the upgraded board would be simplified with respect to the present. Moreover, a GTP pair dissipates less power than the G-Link chip-set, so the power dissipation due to data de-serialization will be lowered in the upgrade.

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