National Semiconductor

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SCAN92LV090
9 Channel Bus LVDS Transceiver w/ Boundary SCAN

General Description

The SCAN92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of ±1V.

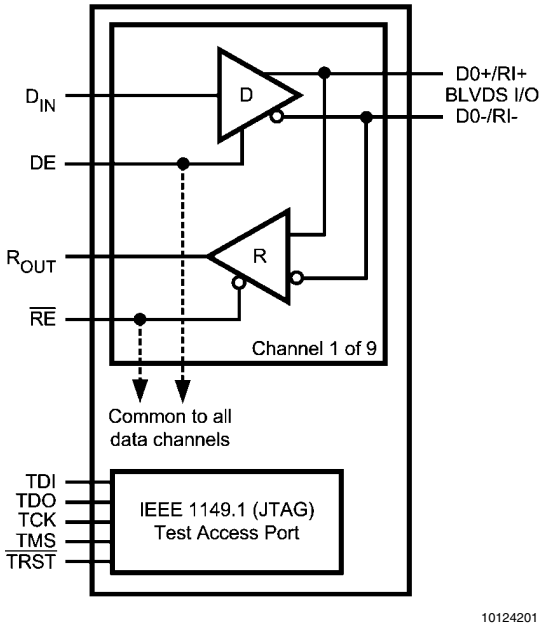
The receiver threshold is less than ±100 mV over a ±1V common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels.

This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCK), and the optional Test Reset ($\overline{TRST}$).

Features

- IEEE 1149.1 (JTAG) Compliant
- Bus LVDS Signaling
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- 0.1V to 2.3V Common Mode Range for V_{ID} = 200mV
- ±100 mV Receiver Sensitivity
- Supports open and terminated failsafe on port pins
- 3.3V operation
- Glitch free power up/down (Driver & Receiver disabled)
- Light Bus Loading (5 pF typical) per Bus LVDS load
- Designed for Double Termination Applications
- Balanced Output Impedance
- Product offered in 64 pin LQFP package and BGA package
- High impedance Bus pins on power off (V_{CC} = 0V)

Simplified Functional Diagram



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Connection Diagrams

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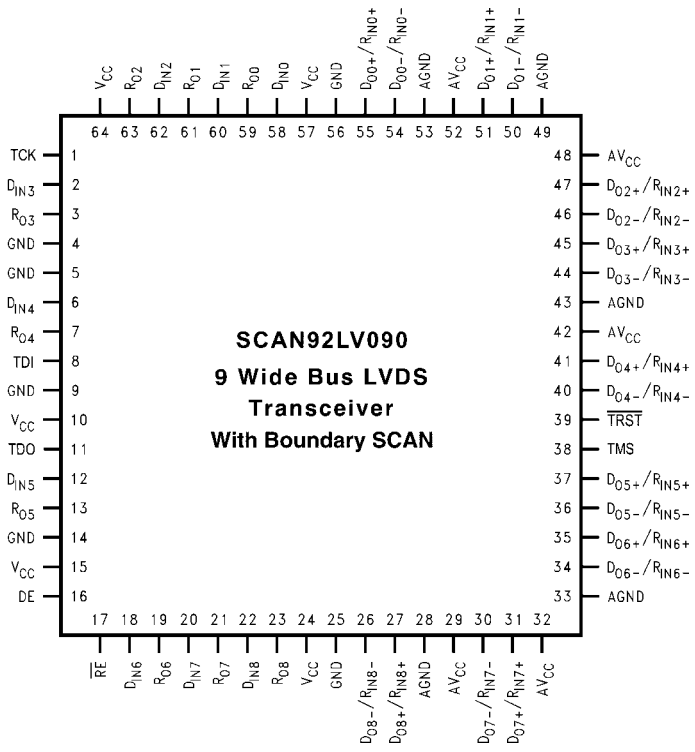

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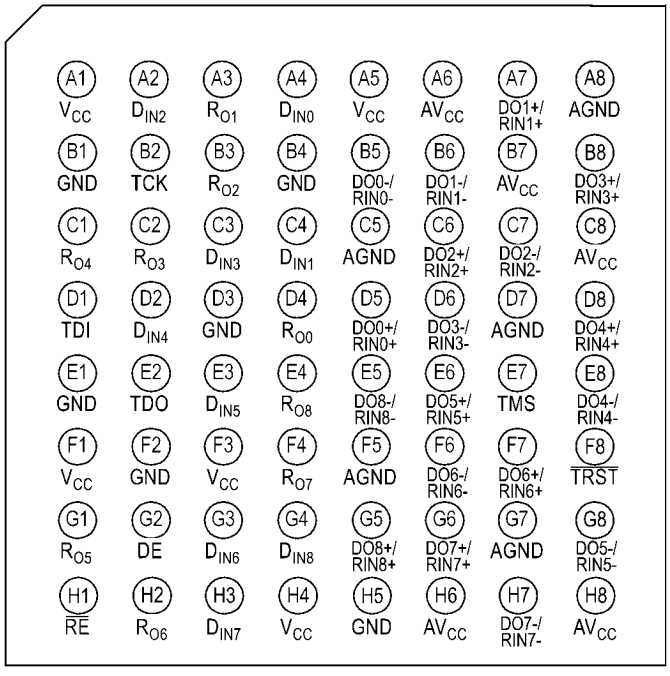
Top View
Order Number SCAN92LV090VEH
See NS Package Number VEH064DB



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Top View
Order Number SCAN92LV090SLC
See NS Package Number SLC64A

Pinout Description

Pin Name	TQFP Pin #	BGA Pin #	Input/Output	Descriptions
DO+/RI+	27, 31, 35, 37, 41, 45, 47, 51, 55	A7, B8, C6, D5, D8, E6, F7, G5, G6	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO−/RI−	26, 30, 34, 36, 40, 44, 46, 50, 54	B5, B6, C7, D6, E5, E8, F6, G8, H7	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D_{IN}	2, 6, 12, 18, 20, 22, 58, 60, 62	A2, A4, C3, C4, D2, E3, G3, G4, H3	I	TTL Driver Input.
RO	3, 7, 13, 19, 21, 23, 59, 61, 63	A3, B3, C1, C2, D4, E4, F4, G1, H2	O	TTL Receiver Output.
$\overline{RE}$	17	H1	I	Receiver Enable TTL Input (Active Low).
DE	16	G2	I	Driver Enable TTL Input (Active High).
GND	4, 5, 9, 14, 25, 56	B1, B4, D3, E1, F2, H5	Power	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V_{CC}	10, 15, 24, 57, 64	A1, A5, F1, F3, H4	Power	V_{CC} for digital circuitry (must connect to V_{CC} on PC board). These pins connected internally.
AGND	28, 33, 43, 49, 53	A8, C5, D7, F5, G7	Power	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV_{CC}	29, 32, 42, 48, 52	A6, B7, C8, H6, H8	Power	Analog V_{CC} (must connect to V_{CC} on PC board). These pins connected internally.
$\overline{TRST}$	39	F8	I	Test Reset Input to support IEEE 1149.1 (Active Low)
TMS	38	E7	I	Test Mode Select Input to support IEEE 1149.1
TCK	1	B2	I	Test Clock Input to support IEEE 1149.1
TDI	8	D1	I	Test Data Input to support IEEE 1149.1
TDO	11	E2	O	Test Data Output to support IEEE 1149.1

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	4.0V
Enable Input Voltage (DE, $\overline{RE}$)	−0.3V to (V_{CC} +0.3V)
Driver Input Voltage (D_{IN})	−0.3V to (V_{CC} +0.3V)
Receiver Output Voltage (R_{OUT})	−0.3V to (V_{CC} +0.3V)
Bus Pin Voltage (DO/RI±)	−0.3V to +3.9V
ESD (HBM 1.5 kΩ, 100 pF)	>4.5 kV
Driver Short Circuit Duration	momentary
Receiver Short Circuit Duration	momentary
Maximum Package Power Dissipation at 25°C	
LQFP	1.74 W
Derate LQFP Package	13.9 mW/°C
θ_{ja}	71.7°C/W
θ_{jc}	10.9°C/W
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.4	V
Operating Free Air Temperature	−40	+85	°C
Maximum Input Edge Rate			Δt/ΔV
(Note 6)(20% to 80%)			
Data		1.0	ns/V
Control		3.0	ns/V

DC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, *Figure 1*		DO+/RI+, DO−/RI−	240	300	460	mV
ΔV_{OD}	V_{OD} Magnitude Change						27	mV
V_{OS}	Offset Voltage				1.1	1.3	1.5	V
ΔV_{OS}	Offset Magnitude Change					5	10	mV
V_{OH}	Driver Output High Voltage	R_L = 27Ω				1.4	1.65	V
V_{OL}	Driver Output Low Voltage	R_L = 27Ω			0.95	1.1		V
I_{OSD}	Output Short Circuit Current (Note 10)	V_{OD} = 0V, DE = V_{CC}, Driver outputs shorted together				|36|	|65|	mA
V_{OH}	Voltage Output High (Note 11)	V_{ID} = +300 mV	I_{OH} = −400 µA	R_{OUT}	V_{CC}−0.2			V
		Inputs Open			V_{CC}−0.2			V
		Inputs Terminated, R_L = 27Ω			V_{CC}−0.2			V
V_{OL}	Voltage Output Low	I_{OL} = 2.0 mA, V_{ID} = −300 mV				0.05	0.075	V
I_{OD}	Receiver Output Dynamic Current (Note 10)	V_{ID} = 300mV, V_{OUT} = V_{CC}−1.0V			−110	|75|		mA
		V_{ID} = −300mV, V_{OUT} = 1.0V				|75|	110	mA
V_{TH}	Input Threshold High	DE = 0V, V_{CM} = 1.5V		DO+/RI+, DO−/RI−			+100	mV
V_{TL}	Input Threshold Low				−100			mV
V_{CMR}	Receiver Common Mode Range				|V_{ID}|/2		2.4 − |V_{ID}|/2	V
I_{IN}	Input Current	DE = 0V, $\overline{RE}$ = 2.4V, V_{IN} = +2.4V or 0V			−25	±1	+25	µA
		V_{CC} = 0V, V_{IN} = +2.4V or 0V			−20	±1	+20	µA
V_{IH}	Minimum Input High Voltage			D_{IN}, DE, $\overline{RE}$, TCK, $\overline{TRST}$, TMS, TDI	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V		D_{IN}, DE, $\overline{RE}$	−20	±10	+20	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			−20	±10	+20	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA			−1.5	−0.8		V

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
I_{IH}	Input High Current	$V_{IN} = V_{CC}$	TDI, TMS, TCK, $\overline{TRST}$	-20		+20	µA
I_{ILR}	Input Low Current	V_{IN} = GND, V_{CC} = 3.6v	TDI, TMS, $\overline{TRST}$	-25		-115	µA
I_{IL}	Input Low Current	VIN = GND	TCK	-20		+20	µA
I_{CCD}	Power Supply Current Drivers Enabled, Receivers Disabled	No Load, DE = $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND	V_{CC}		50	80	mA
I_{CCR}	Power Supply Current Drivers Disabled, Receivers Enabled	DE = $\overline{RE}$ = 0V, V_{ID} = ±300mV			50	80	mA
I_{CCZ}	Power Supply Current, Drivers and Receivers TRI-STATE®	DE = 0V; $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND			50	80	mA
I_{CC}	Power Supply Current, Drivers and Receivers Enabled	DE = V_{CC}; $\overline{RE}$ = 0V, DIN = V_{CC} or GND, R_L = 27Ω			160	210	mA
I_{CCS}	Power Supply Current (SCAN Test Mode), Drivers and Receivers Enabled	DE = V_{CC}; $\overline{RE}$ = 0V, DIN = V_{CC} or GND, R_L = 27Ω, TAP in any state other than Test-Logic-Reset			180	230	mA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0V or OPEN, D_{IN}, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED}$ = 3.6V (Port Pins)	DO+/RI+, DO−/RI−	−20		+20	µA
C_{OUTPUT}	Capacitance @ Bus Pins		DO+/RI+, DO−/RI−		5		pF
C_{OUTPUT}	Capacitance @ R_{OUT}		R_{OUT}		7		pF

AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Note 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low (Note 8)	R_L = 27Ω, *Figure 2*, *Figure 3* C_L = 10 pF	1.0	1.8	2.6	ns
t_{PLHD}	Differential Prop. Delay Low to High (Note 8)		1.0	1.8	2.6	ns
t_{SKD1}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (Note 9)			120		ps
t_{SKD2}	Chip to Chip Skew (Note 12)				1.6	ns
t_{SKD3}	Channel to Channel Skew (Note 13)			0.25	0.55	ns
t_{TLH}	Transition Time Low to High			0.5	1.2	ns
t_{THL}	Transition Time High to Low			0.5	1.2	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, *Figure 4*, *Figure 5* C_L = 10 pF		3	8	ns
t_{PLZ}	Disable Time Low to Z			3	8	ns
t_{PZH}	Enable Time Z to High			3	8	ns
t_{PZL}	Enable Time Z to Low			3	8	ns
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Prop. Delay High to Low (Note 8)	*Figure 6*, *Figure 7* C_L = 35 pF	2.0	2.4	3.9	ns
t_{PLHD}	Differential Prop Delay Low to High (Note 8)		2.0	2.4	3.9	ns
t_{SDK1}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (Note 9)			210		ps
t_{SDK2}	Chip to Chip Skew (Note 12)				1.9	ns
t_{SDK3}	Channel to Channel skew (Note 13)			0.35	0.7	ns
t_{TLH}	Transition Time Low to High			1.5	2.5	ns
t_{THL}	Transition Time High to Low			1.5	2.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, *Figure 8*, *Figure 9* C_L = 35 pF		4.5	10	ns
t_{PLZ}	Disable Time Low to Z			3.5	8	ns
t_{PZH}	Enable Time Z to High			3.5	8	ns
t_{PZL}	Enable Time Z to Low			3.5	8	ns
SCAN CIRCUITRY TIMING REQUIREMENTS						
f_{MAX}	Maximum TCK Clock Frequency	R_L = 500Ω, C_L = 35 pF	25.0	75.0		MHz
t_S	TDI to TCK, H or L		1.5			ns
t_H	TDI to TCK, H or L		1.5			ns
t_S	TMS to TCK, H or L		2.5			ns
t_H	TMS to TCK, H or L		1.5			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{TRST}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{TRST}$ to TCK		2.0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.

Note 3: All typicals are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) > 4.5 kV EIAJ (0Ω, 200 pF) > 300V.

Note 5: C_L includes probe and fixture capacitance.

Note 6: Generator waveforms for all tests unless otherwise specified: f = 25 MHz, Z_O = 50Ω, t_r, t_f = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

Note 7: The DS92LV090A functions within datasheet specification when a resistive load is applied to the driver outputs.

Note 8: Propagation delays are guaranteed by design and characterization.

Note 9: t_{SKD1} $\lvert t_{PHLD} - t_{PLHD} \rvert$ is the worse case skew between any channel and any device over recommended operation conditions.

Note 10: Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.

Note 11: V_{OH} failsafe terminated test performed with 27Ω connected between RI+ and RI− inputs. No external voltage is applied.

Note 12: Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.

Note 13: Channel to Channel skew is the difference in driver output or receiver output propagation delay between any channels within a device, common edge.

Applications Information

General application guidelines and hints may be found in the following application notes: AN-808, AN-1108, AN-977, AN-971, and AN-903.

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Two or three high frequency, multi-layer ceramic (MLC) surface mount (0.1 µF, 0.01 µF, 0.001 µF) in parallel should be used between each V_{CC} and ground. The capacitors should be as close as possible to the V_{CC} pin. Multiple vias should be used to connect V_{CC} and Ground planes to the pads of the by-pass capacitors.
  In addition, randomly distributed by-pass capacitors should be used.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.
- Isolate TTL signals from Bus LVDS signals

MEDIA (CONNECTOR or BACKPLANE) SELECTION:

- Use controlled impedance media. The backplane and connectors should have a matched differential impedance.

TABLE 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

TABLE 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	**D_{IN}**	**DO+**	**DO–**
H	L	L	H
H	H	H	L
H	0.8V< D_{IN} <2.0V	X	X
L	X	Z	Z

TABLE 3. Receiver Mode

INPUTS		OUTPUT
$\overline{RE}$	**(RI+) – (RI–)**	
L	L (< –100 mV)	L
L	H (> +100 mV)	H
L	–100 mV < V_{ID} < +100 mV	X
H	X	Z

X = High or Low logic state
L = Low state
Z = High impedance state
H = High state

Test Circuits and Timing Waveforms

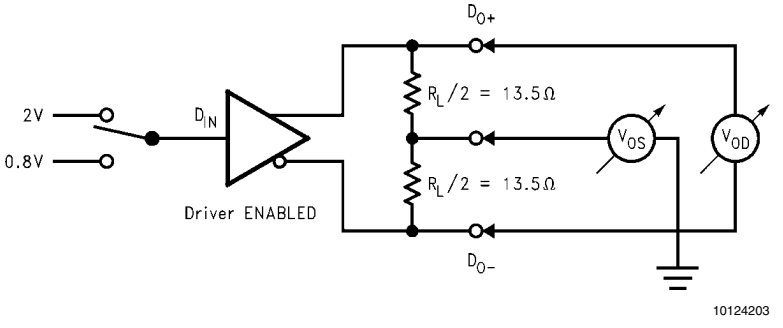


FIGURE 1. Differential Driver DC Test Circuit

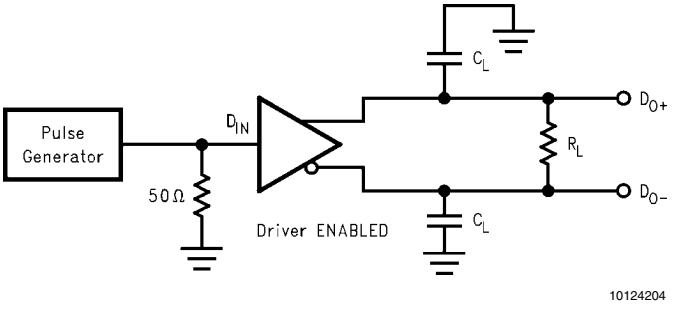


FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

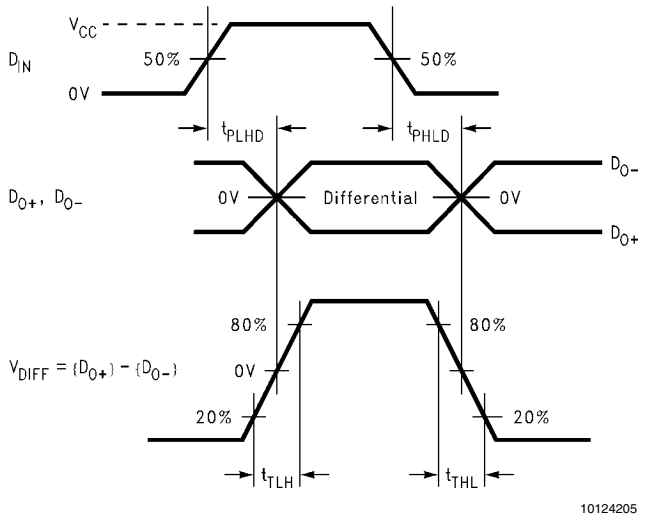


FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

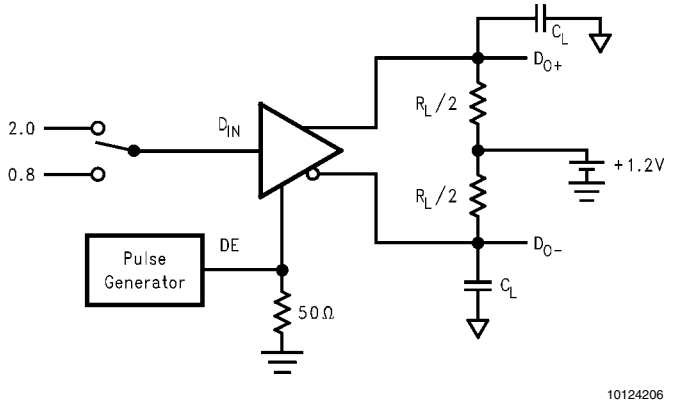


FIGURE 4. Driver TRI-STATE Delay Test Circuit

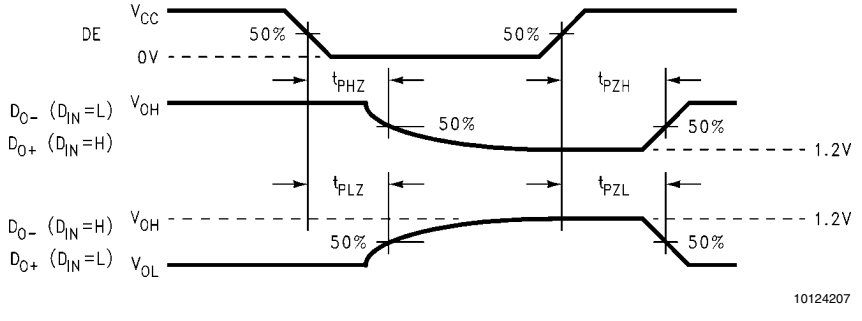


FIGURE 5. Driver TRI-STATE Delay Waveforms

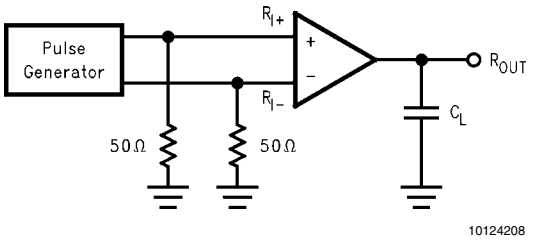


FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

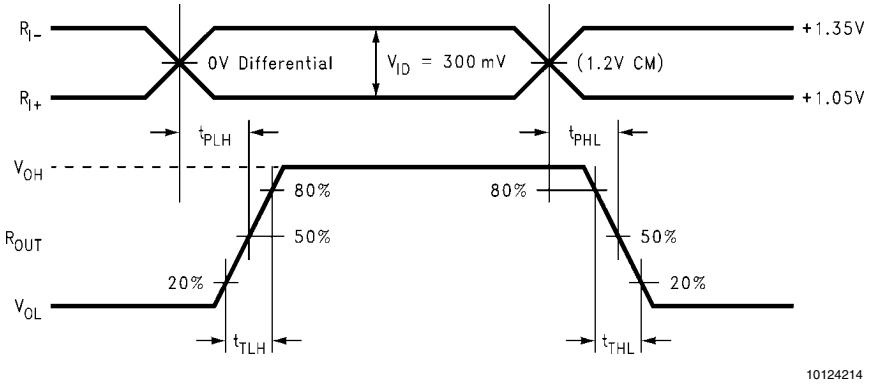


FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

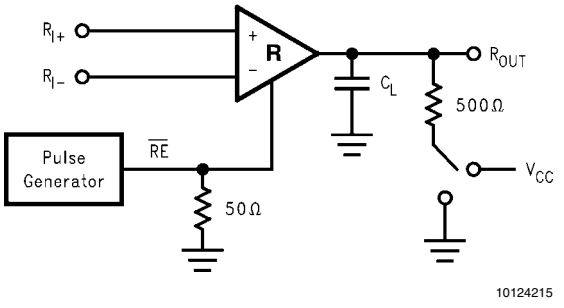


FIGURE 8. Receiver TRI-STATE Delay Test Circuit

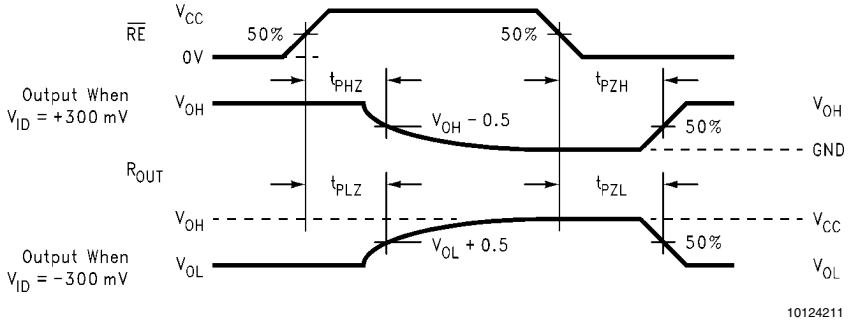
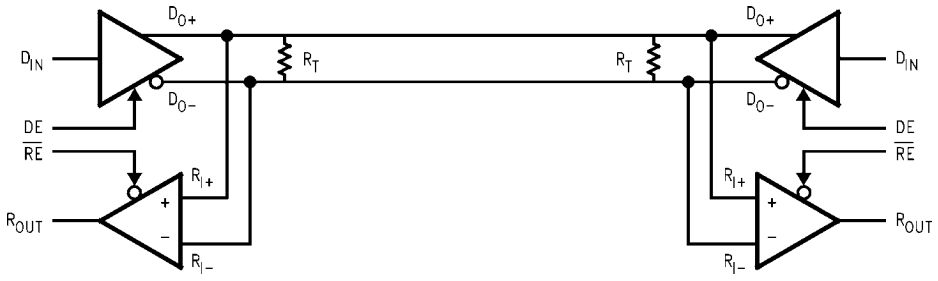


FIGURE 9. Receiver TRI-STATE Delay Waveforms

Typical Bus Application Configurations



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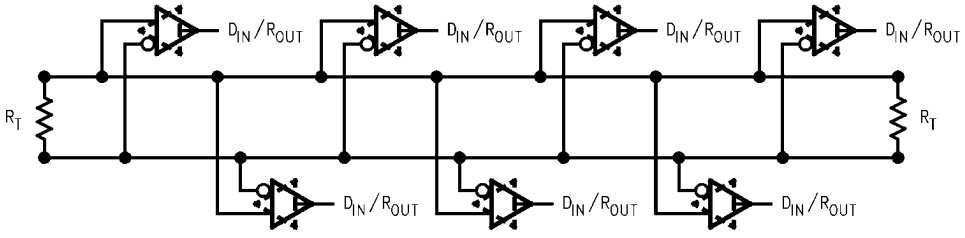
Bi-Directional Half-Duplex Point-to-Point Applications



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Multi-Point Bus Applications

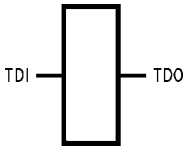
Description of Boundary-Scan Circuitry

The SCAN92LV090 features two unique Scan test modes, each which requires a unique BSDL model depending on the level of test access and fault coverage goals. In the first mode (Mode0), only the TTL Inputs and Outputs of each transceiver are accessible via a 1149.1 compliant protocol. In the second mode (Mode1), both the TTL Inputs and Outputs and the differential LVDS I/Os are included in the Scan chain.

All test modes are handled by the ATPG software, and BSDL selection should be invisible to the user.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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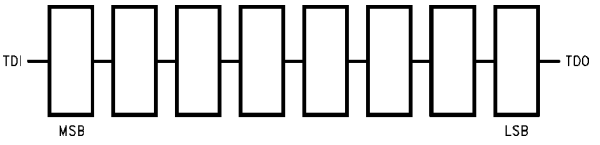
The INSTRUCTION register is an eight-bit register which captures the value 00111101.

Instruction Register Scan Chain Definition



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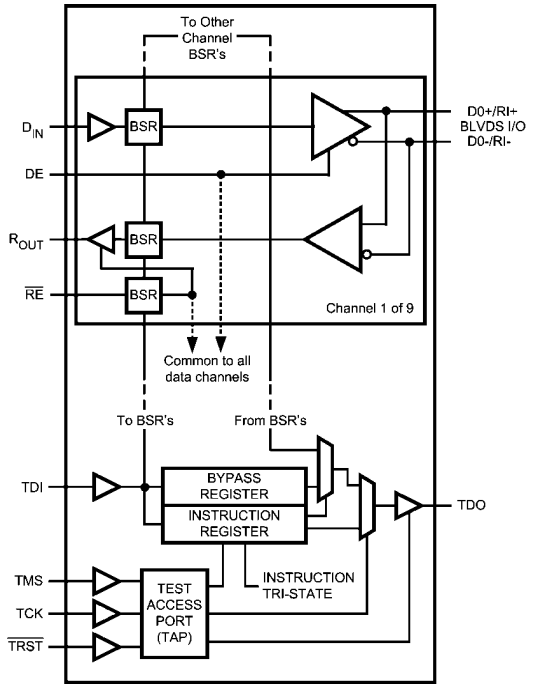
MSB → LSB (Mode0)

Instruction Code	Instruction
00000000	EXTEST
10000010	SAMPLE/PRELOAD
10000111	CLAMP
00000110	HIGHZ
All Others	BYPASS

MSB → LSB (Mode1)

Instruction Code	Instruction
10011001	EXTEST
10010010	SAMPLE/PRELOAD
10001111	CLAMP
00000110	HIGHZ
All Others	BYPASS



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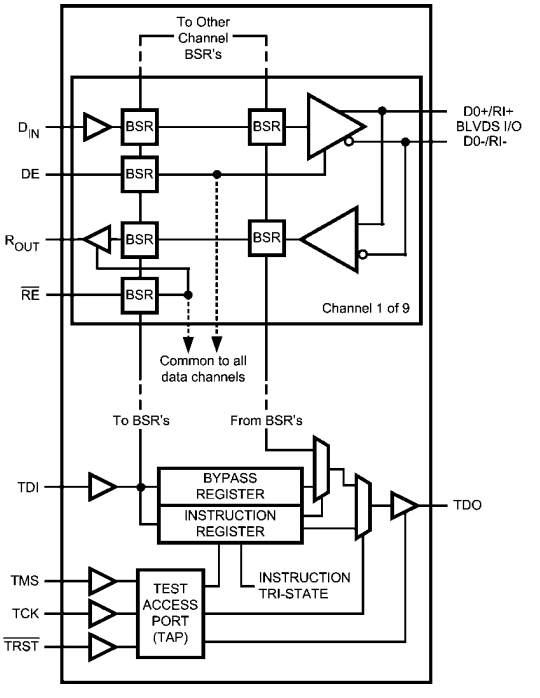
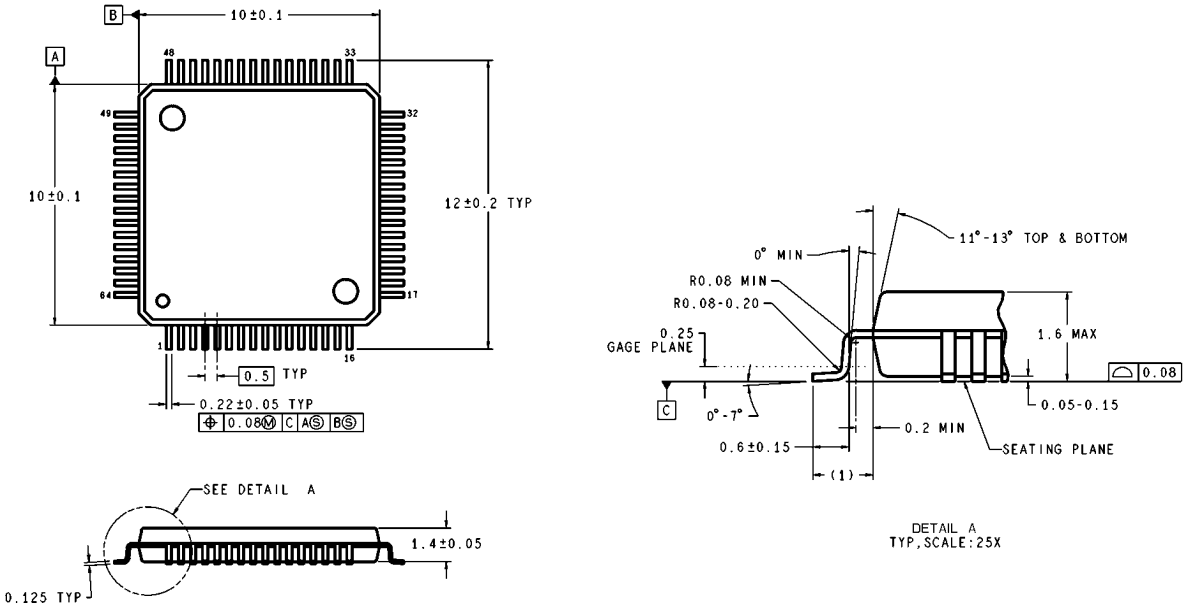
Mode 0 Boundary Scan Register Configuration
(Refer to the BSDL for exact register order)



10124220

Mode 1 Boundary Scan Register Configuration
(Refer to the BSDL for exact register order)

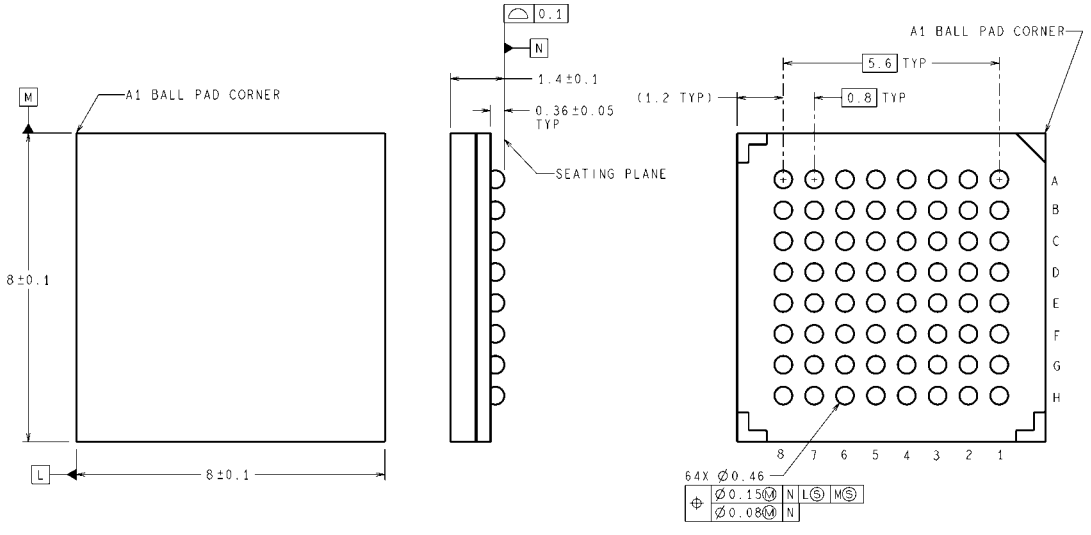
Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

VEH64A (Rev C)

64-Lead Molded LQFP Package
Order Number SCAN92LV090VEH
NS Package Number VEH064DB



DIMENSIONS ARE IN MILLIMETERS

SLC64A (Rev C)

64-Lead Ball Grid Array Package
Order Number SCAN92LV090SLC
NS Package Number SLC64A

Notes

Notes

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