PICOLIGHT

SNAP12
12 channel pluggable optical module MSA

MAGNUS ™

12 x 1.6 / 2.5 / 2.7 Gbps Parallel Optical Transmitter/Receiver

PL-TCP-00-SD3 / S53 / SE3 Transmitter
PL-RCP-00-SD3 / S53 / SE3 Receiver

The MAGNUS parallel optical interconnect is a transmitter/receiver pair operating with 12 channels at 1.6, 2.5, and 2.7 Gbps for an aggregate bandwidth of 19, 30, and 32 Gbps respectively. The parallel modules are another in Picolight's MAGNUS family of products for optical backplane applications, where high-speed, high-density components are needed to handle increased bandwidth demand. The parallel optical interconnect complies with the SNAP12 multisource agreement, and features Picolight's highly reliable 850 nm, oxide vertical-cavity surface-emitting laser (VCSEL) array with a standard Ball Grid Array (BGA) connector interface. The module's pluggable, connectorized design enables manufacturers to provision bandwidth on demand, upgrading cards in the field with the snap-on optics. The parallel optical interconnect complies with the IEEE802.3 1000BASE-SX standard.

Key benefits

- Delivers bandwidth to key system bottlenecks
- Reduces inventory costs
- Enables field replacement
- Improves manufacturing yield
- Minimizes impact on system power budget
- Eases system design
- Enables multiple data channel fanout
- Multisource availability strengthens supply chain

Applications

- Optical backplane extension
- System interconnect
  - Cross connect switching
  - Network edge devices
  - Access network equipment
  - Mass storage systems
- Massively parallel OC-48 or Gigabit Ethernet extension
- High end CPU interconnect
- Rack-to-rack/Board-to-board interconnect

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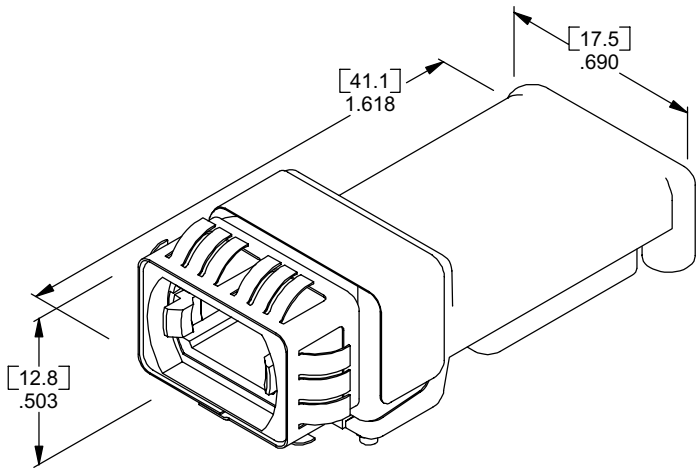
Highlights

- ***Expands bandwidth across equipment backplanes**, meeting ultra-high capacity demand for faster central office switching*
- ***BGA connector attachment enables "snap-on" optics** that improve customers' manufacturing yields, reduce inventory costs, and provide capability for system field upgrade to add bandwidth*
- ***Thumb-sized modules consume only 2 watts of power per pair,** lowering system power costs and increasing density*
- ***System backplanes become "distance-independent,"** seamlessly connecting equipment from 0 to 600 meters over high-bandwidth fiber, 0 to 300 meters over low-bandwidth fiber*
- ***Data rates per channel range from 1.6 Gbps to 2.7 Gbps**, allowing customers to select the optimum model for their applications*
- ***SNAP12 multisource agreement** compliance ensures reliable supply chain*

PL-xCP-00-SD3 / S53 / SE3 features

- Utilizes a Picolight high reliability, high speed, 850 nm, oxide VCSEL array
- Data rate to 1.6 / 2.5 / 2.7 Gbps per channel for a total link data rate of 19 / 30 / 32 Gbps
- Mass production compatible Ball Grid Array (BGA) connector interface
- Low power consumption (approx. 2 watts per module pair)
- 12 asynchronous independent electrical/optical data channels
- Meets IEEE 802.3z 1000Base-SX std.
- Bit Error Rate < $1x10^{-12}$ without FEC
- Supports 50/125 μm and 62.5/ 125 μm multimode fiber
- Industry standard MTP optical interface
- BGA connector compatible with industry standard wave solder and aqueous wash processes
- IEC 60825-1 Amendment 2 (2001-01) Class 1M laser eye safe
- 0°C to 80°C operating range
- Single +3.3 V power supply
- Supplied with process plug



The 12-channel PL-xCP-00-SD3 / S53 / SE3 parallel optical interconnect is the first of its kind to combine the convenience of low-cost, snap-on connector pluggability with the speed of parallel optics. It sets a new standard for ease of design, manufacture, test and field support of ultrahigh-speed optics required across equipment backplane in core switches, routers and multiplexors.

Ordering information

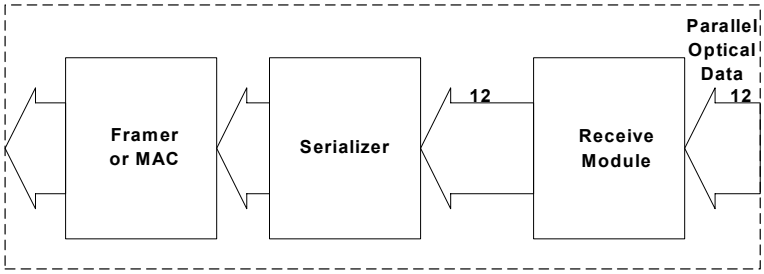
Part Number:	Description:	Contact Information:
PL-TCP-00-SD3-0A	MAGNUS 12 x 1.6 Gbps Transmitter	Picolight Incorporated 4665 Nautilus Court South Boulder, CO 80301 Tel: 303.530.3189 E-mail: sales@picolight.com Web site: www.picolight.com For information on SNAP12: Web site: www.snapoptics.org
PL-RCP-00-SD3-0B	MAGNUS 12 x 1.6 Gbps Receiver	
PL-TCP-00-SD3-3A	MAGNUS 12 x 1.6 Gbps Transmitter, without EMI collar	
PL-RCP-00-SD3-3B	MAGNUS 12 x 1.6 Gbps Receiver, without EMI collar	
PL-TCP-00-S53-OB	MAGNUS 12 x 2.5 Gbps Transmitter	
PL-RCP-00-S53-0C	MAGNUS 12 x 2.5 Gbps Receiver	
PL-TCP-00-S53-3A	MAGNUS 12 x 2.5 Gbps Transmitter, without EMI collar	
PL-RCP-00-S53-3B	MAGNUS 12 x 2.5 Gbps Receiver, without EMI collar	
PL-TCP-00-SE3-0A	MAGNUS 12 x 2.7 Gbps Transmitter	
PL-RCP-00-SE3-0B	MAGNUS 12 x 2.7 Gbps Receiver	
PL-TCP-00-SE3-3A	MAGNUS 12 x 2.7 Gbps Transmitter, without EMI collar	
PL-RCP-00-SE3-3B	MAGNUS 12 x 2.7 Gbps Receiver, without EMI collar	

Section 1 Functional description

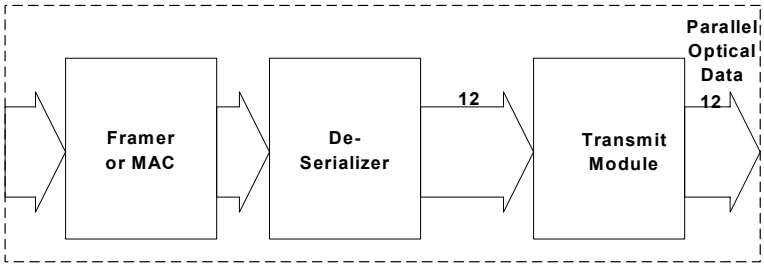
The PL-xCP-00-SD3 / S53 / SE3 850 nm VCSEL Gigabit Transmitter/Receiver is designed to transmit and receive DC balanced data, such as 2.488G OC-48, or 8B/10B encoded data, over 50/125 μm or 62.5/125 μm optical fiber.

Note: All references to SNAP12 MSA specifications refer to version 1.0 of that document.

Figure 1 Recommended application for the PL-xCP-00-SD3 / S53 / SE3 transmitter/receiver



Receiver Module Application Block Diagram



Transmitter Module Application Block Diagram

Transmitter

The transmitter converts 12 channels of encoded DC balanced CML electrical data into serial optical data. Transmit data lines (DIN 01: DIN 12) are terminated with 100 Ω, differential. See Figure 7 on page 6, and Figures 8 and 9 on page 7 for application schematic information. Unused channels should have inputs tied together.

The transmitter has an internal PIN monitor diode that is used to ensure constant optical power output across supply voltage and temperature variations.

TXEN/TXDIS

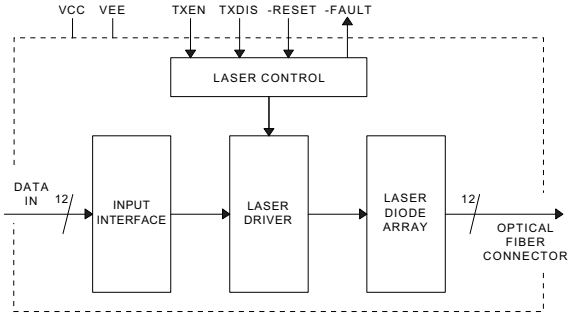
LVCMOS logic level Transmit Enable (TXEN) and Transmit Disable (TXDIS) are provided. A logic “1” or no connection on the TXEN pin **and** a logic “0” or no connection on the TXDIS pin allow normal operation. Both signals **must** be connected as described for normal operation. A logic “0” on the TXEN pin **or** a logic “1” on the TXDIS pin will disable all transmit channels.

-Reset/-Fault

An LVCMOS logic level fault output (-Fault) is provided. A logic “1” on this pin indicates proper operation. A logic “0” on this pin indicates a fault has occurred in the laser circuitry and all laser outputs are disabled.

An LVCMOS logic level reset input (-Reset) is provided. A logic “1” on this pin allows normal operation. A logic “0” on this pin will reset the laser circuitry and disable all laser outputs. (-Fault will indicate logic “0” when -Reset is logic “0”.) During power-up, -Reset must remain logic “0” until the power supply (Vcc) has reached a minimum of 3V.

Figure 2 Transmit module block diagram



Receiver

The receiver converts encoded serial optical data into DC balanced parallel CML electrical data. Receive data lines (DOUT1:DOUT12) should be terminated into single-ended 50 Ω loads or equivalent.

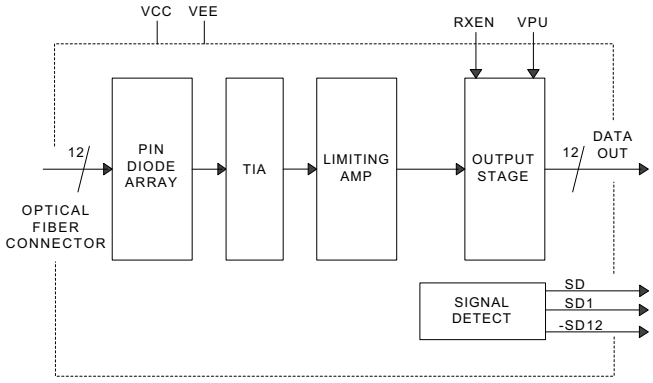
SD/SD1/-SD12

LVCMOS Signal Detect Status Outputs (SD, SD1 and -SD12) are provided. SD, SD1 and -SD12 are independent signal detect status indicators for all channels, channel 1, and channel 12 respectively. A logic “1” on SD indicates that sufficient optical signal has been detected on all channels (see Section 3.5 Electrical characteristics; “Signal Detect Assert/Negate Level on page 17). A logic “0” on SD indicates that insufficient optical signal for proper operation has been detected on at least one of the 12 channels. A logic “1” on SD1 and a logic “0” on -SD12 indicate that sufficient optical signal has been detected on channels 1 and 12. A logic “0” on SD1 and/or a logic “1” on -SD12 indicates that insufficient optical signal has been detected at channel 1 and/or 12 for proper operation.

RXEN

An LVCMOS Receive Output Enable Input (RXEN) is provided. A logic “1” on RXEN will enable proper operation of the high speed data outputs. A logic “0” on RXEN sets all of the differential channel data outputs to a fixed logic “0” state. RXEN does not affect the Signal Detect functionality.

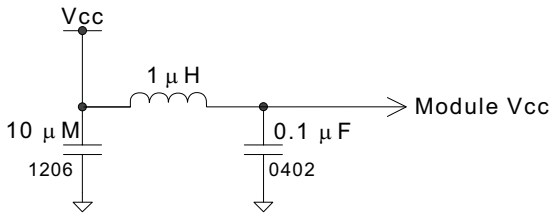
Figure 3 Receive module block diagram



Power supply and grounding

Power supply filtering is recommended for both the transmitter and receiver. Filtering should be placed on the host assembly as close to the Vcc pins as possible for optimal performance. Recommended filtering shown in Figure 4.

Figure 4 Recommended filtering



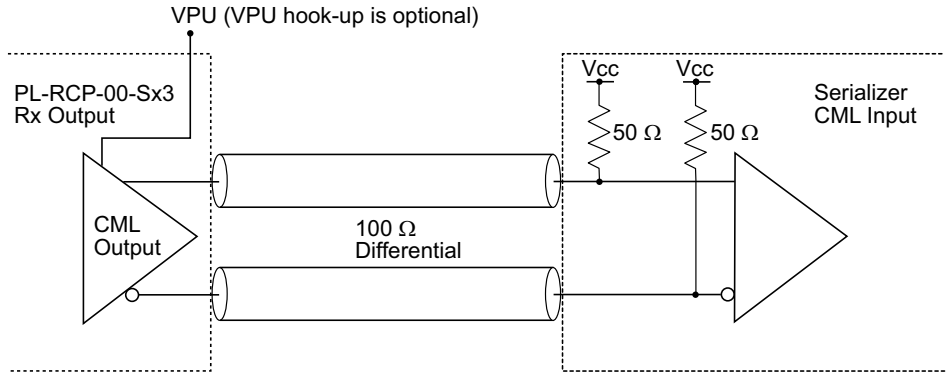
L1 - 1 µ H or Murata BLM21P221SG

Module signal and power grounds are common. The module case is not connected internally to power ground. The module case can be electrically contacted through the front or rear screws.

Section 2 Application schematics

Recommended connections to the PL-xCP-00-SD3 / S53 / SE3 transmitter/receiver are shown in Figure 5, 6, 7, 8, and 9.

Figure 5 Rx module; high speed output; CML interface



Note: VPU connection leave open or connect to external CML pull-up voltage (SNAP12 MSA VPU connect to 3.3 V).

Figure 6 Rx module; high speed output; AC coupled interface

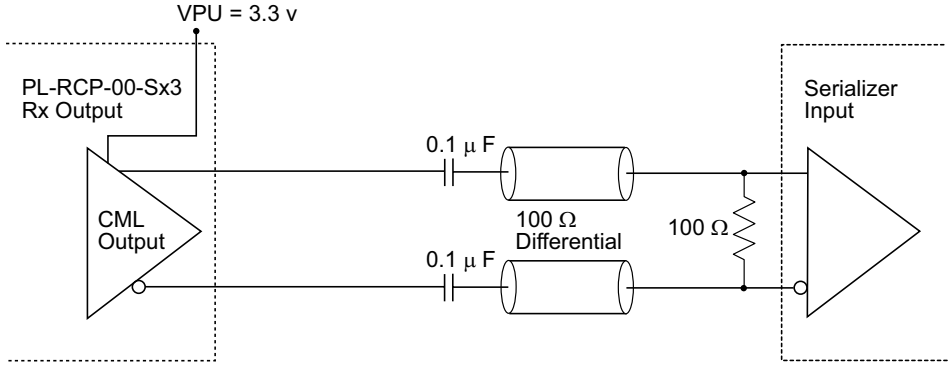


Figure 7 Tx module; high speed input; CML interface

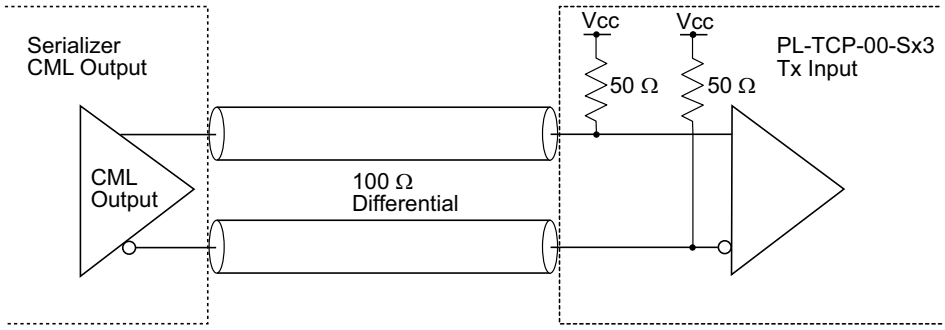


Figure 8 Tx module; high speed input; LVDS or similar interface

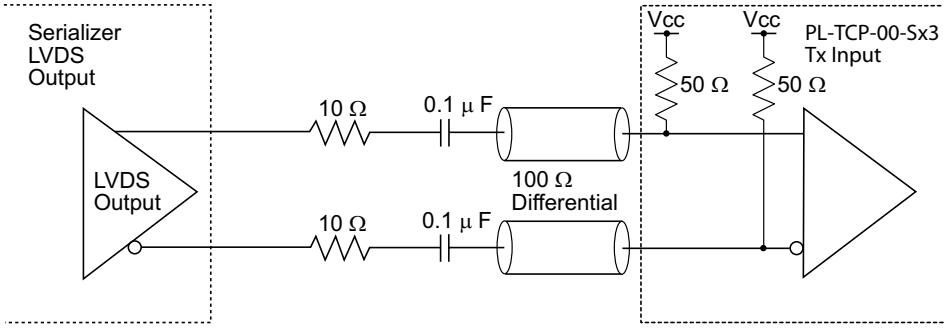
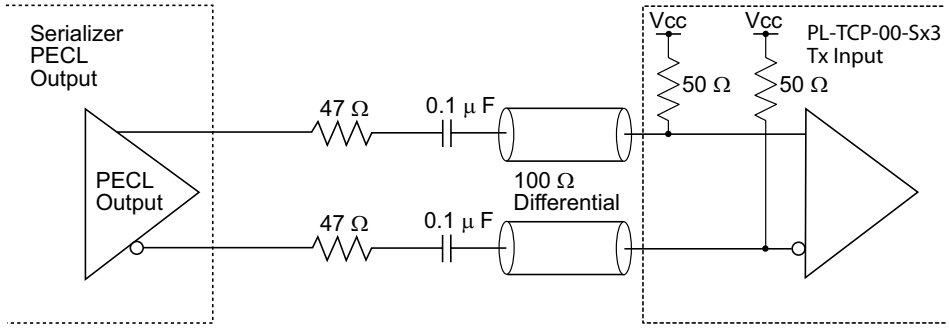


Figure 9 Tx module; high speed input; PECL or similar interface



Notes

Power supply filtering components should be placed on the opposite side of the PCB directly under the PL-xCP-00-SD3 / S53 / SE3 transmitter/receiver, as close to the Vcc pins as possible for optimal performance.

PECL, LVDS, or other outputs may require biasing networks, not shown. Consult Application Information for those devices.

Transmission lines should be 100 ohm differential traces. It is recommended that the termination resistor be placed beyond the Rx IC pins.

For unused channels, receiver output pairs should be left unconnected. Unused transmitter inputs should be tied together.

If using dc coupling, users must ensure data remains dc balanced. Otherwise, rated optical output power may be exceeded.

Series resistors can be used to improve electrical crosstalk on a system board and to improve impedance match at the source.

Section 3 Technical data

Technical data related to the 12x1.6 / 2.5 / 2.7 Gbps Parallel Optical Transmitter/Receiver includes:

3.1 Receiver pin descriptions

Pin Number	Symbol	Type	Description
A2	GND		Ground
A3	GND		Groung
A5	GND		Ground
A6	GND		Ground
B1	GND		Ground
B2	Dout9n	CML Out	Data Output, inverted
B3	Dout9p	CML Out	Data Output, non-inverted
B4	GND		Ground
B5	Dout10p	CML Out	Data Output, non-inverted
B6	Dout10n	CML Out	Data Output, inverted
B7	GND		Ground
B8	GND		Ground
B9	GND		Ground
C1	GND		Ground
C2	GND		Ground
C3	Dout8n	CML Out	Data Output, inverted
C4	Dout8p	CML Out	Data Output, non-inverted
C5	GND		Ground

3.1 Receiver pin descriptions (continued)

Pin Number	Symbol	Type	Description
C6	Dout11p	CML Out	Data Output, non-inverted
C7	Dout11n	CML Out	Data Output, inverted
C8	GND		Ground
C9	GND		Ground
D1	GND		Ground
D2	GND		Ground
D3	GND		Ground
D4	Dout7n	CML Out	Data Output, inverted
D5	Dout7p	CML Out	Data Output, non-inverted
D6	GND		Ground
D7	Dout12p	CML Out	Data Output, non-inverted
D8	Dout12n	CML Out	Data Output, inverted
D9	GND		Ground
E1	GND		Ground
E2	Dout6n	CML Out	Data Output, inverted
E3	Dout6p	CML Out	Data Output, non-inverted
E4	GND		Ground
E5	Dout3n	CML Out	Data Output, inverted
E6	Dout3p	CML Out	Data Output, non-inverted
E7	GND		Ground
E8	GND		Ground
E9	GND		Ground
F1	GND		Ground
F2	GND		Ground
F3	Dout5n	CML Out	Data Output, inverted
F4	Dout5p	CML Out	Data Output, non-inverted
F5	GND		Ground
F6	Dout2n	CML Out	Data Output, inverted
F7	Dout2p	CML Out	Data Output, non-inverted
F8	GND		Ground
F9	GND		Ground
G1	GND		Ground
G2	GND		Ground
G3	GND		Ground
G4	Dout4n	CML Out	Data Output, inverted

3.1 Receiver pin descriptions (continued)

Pin Number	Symbol	Type	Description
G5	Dout4p	CML Out	Data Output, non-inverted
G6	GND		Ground
G7	Dout1n	CML Out	Data Output, inverted
G8	Dout1p	CML Out	Data Output, non-inverted
G9	GND		Ground
H3	VCC		Power supply voltage
H4	VCC		Power supply voltage
H5	VCC		Power supply voltage
H6	VCC		Power supply voltage
H7	SD	LVCMOS Out	Signal Detect on all fibers High=signal of sufficient AC power is present on all fibers Low=signal on at least one fiber is insufficient
H8	SD1	LVCMOS Out	Signal Detect on fiber #1 High=signal of sufficient AC power is present on fiber #1 Low=signal on fiber #1 is insufficient
I3	VCC		Power supply voltage
I4	VCC		Power supply voltage
I5	VCC		Power supply voltage
I6	VCC		Power supply voltage
I8	SD12	LVCMOS Out	Signal Detect on fiber #12 Low=signal of sufficient AC power is present on fiber #12 High=signal on fiber #12 is insufficient
I9	RXEN	LVCMOS In	High=normal output operation Low=all data outputs set low Internal pull-up
J1	VPU (SNAP12 MSA = VCC)		Power supply voltage to internal pull-up resistors. No connection required for existing boards with external CML pull-up resistors.
J2	VPU (SNAP12 MSA = VCC)		Power supply voltage to internal pull-up resistors. No connection required for existing boards with external CML pull-up resistors.
J10	SQEN	LVCMOS In	Squelch enable. High=all data outputs driven to logic “0” when SD is active (low) Low=squelch disabled Internal pull-up

3.1.1 RX module signals on user's board

Top view of user's board (this edge towards fiber ribbon)										
Larger connector orientation feature/key										
	J	**I**	**H**	**G**	**F**	**E**	**D**	**C**	**B**	**A**
1	VPU (SNAP12:VCC)	NIC	NIC	GND	GND	GND	GND	GND	GND	NIC
2	VPU (SNAP12:VCC)	NIC	NIC	GND	GND	DOUT6n	GND	GND	DOUT9n	GND
3	NIC	VCC	VCC	GND	DOUT5n	DOUT6p	GND	DOUT8n	DOUT9p	GND
4	NIC	VCC	VCC	DOUT4n	DOUT5p	GND	DOUT7n	DOUT8p	GND	NIC
5	NIC	VCC	VCC	DOUT4p	GND	DOUT3n	DOUT7p	GND	DOUT10p	GND
6	NIC	VCC	VCC	GND	DOUT2n	DOUT3p	GND	DOUT11p	DOUT10n	GND
7	NIC	NIC	SD	DOUT1n	DOUT2p	GND	DOUT12p	DOUT11n	GND	NIC
8	NIC	-SD12	SD1	DOUT1p	GND	GND	DOUT12n	GND	GND	NIC
9	NIC	RXEN	DNC	GND	GND	GND	GND	GND	GND	NIC
10	NIC	NIC	NIC	NIC	NIC	NIC	NIC	NIC	NIC	NIC
Smaller connector orientation feature/key										

Note: NIC is no internal connection, reserved for future use.
Note: DNC is do not connect, reserved for future use.

3.1.2 Rx MTP connector (front view of module)

FRONT VIEW – MTP KEY IS UP											
CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
User PCB below											

3.2 Transmitter pin descriptions

Pin Number	Symbol	Type	Description
A2	GND		Ground
A3	GND		Ground
A5	GND		Ground
A6	GND		Ground
B1	GND		Ground
B2	Din9p	Signal In	Data Input, non-inverted
B3	Din9n	Signal In	Data Input, inverted
B4	GND		Ground
B5	Din10	Signal In	Data Input, inverted

3.2 Transmitter pin descriptions (continued)

Pin Number	Symbol	Type	Description
B6	Din10	Signal In	Data Input, non-inverted
B7	GND		Ground
B8	GND		Ground
B9	GND		Ground
C1	GND		Ground
C2	GND		Ground
C3	Din8p	Signal In	Data Input, non-inverted
C4	Din8n	Signal In	Data Input, inverted
C5	GND		Ground
C6	Din11n	Signal In	Data Input, inverted
C7	Din11p	Signal In	Data Input, non-inverted
C8	GND		Ground
C9	GND		Ground
D1	GND		Ground
D2	GND		Ground
D3	GND		Ground
D4	Din7p	Signal In	Data Input, non-inverted
D5	Din7n	Signal In	Data Input, inverted
D6	GND		Ground
D7	Din12n	Signal In	Data Input, inverted
D8	Din12p	Signal In	Data Input, non-inverted
D9	GND		Ground
E1	GND		Ground
E2	Din6p	Signal In	Data Input, non-inverted
E3	Din6n	Signal In	Data Input, inverted
E4	GND		Ground
E5	Din3p	Signal In	Data Input, non-inverted
E6	Din3n	Signal In	Data Input, inverted
E7	GND		Ground
E8	GND		Ground
E9	GND		Ground
F1	GND		Ground
F2	GND		Ground
F3	Din5p	Signal In	Data Input, non-inverted
F4	Din5n	Signal In	Data Input, inverted

3.2 Transmitter pin descriptions (continued)

Pin Number	Symbol	Type	Description
F5	GND		Ground
F6	Din2p	Signal In	Data Input, non-inverted
F7	Din2n	Signal In	Data Input, inverted
F8	GND		Ground
F9	GND		Ground
G1	GND		Ground
G2	GND		Ground
G3	GND		Ground
G4	Din4p	Signal In	Data Input, non-inverted
G5	Din4n	Signal In	Data Input, inverted
G6	GND		Ground
G7	Din1p	Signal In	Data Input, non-inverted
G8	Din1n	Signal In	Data Input, inverted
G9	GND		Ground
H3	VCC		Power supply voltage of laser driver
H4	VCC		Power supply voltage of laser driver
H5	VCC		Power supply voltage of laser driver
H6	VCC		Power supply voltage of laser driver
H8	-FAULT	LVCMOS Out	Transmit laser fault. Low level indicates a fault.
H9	TXDIS		Transmit laser disable. Active high. Internal pull-down.
I3	VCC		Power supply voltage of laser driver
I4	VCC		Power supply voltage of laser driver
I5	VCC		Power supply voltage of laser driver
I6	VCC		Power supply voltage of laser driver
I7	NC		No connect
I8	-RESET	LVCMOS In	Reset fault condition. Active Low. Internal pull-down.
I9	TXEN	LVCMOS In	Transmit laser enable. Active high. Internal pull-up.

3.2.1 TX module signals on user's board

Top view of user's board (this edge towards fiber ribbon)										
Larger connector orientation feature/key										
	J	**I**	**H**	**G**	**F**	**E**	**D**	**C**	**B**	**A**
1	NIC	NIC	NIC	GND	GND	GND	GND	GND	GND	NIC
2	NIC	NIC	NIC	GND	GND	DIN6p	GND	GND	DIN9p	GND
3	NIC	VCC	VCC	GND	DIN5p	DIN6n	GND	DIN8p	DIN9n	GND
4	NIC	VCC	VCC	DIN4p	DINn	GND	DIN7p	DIN8n	GND	NIC
5	NIC	VCC	VCC	DIN4n	GND	DIN3p	DIN7n	GND	DIN10n	GND
6	NIC	VCC	VCC	GND	DIN2p	DIN3n	GND	DIN11n	DIN10p	GND
7	NIC	NIC	NIC	DIN1p	DIN2n	GND	DIN12n	DIN11p	GND	NIC
8	NIC	-RESET	-FAULT	DIN1n	GND	GND	DIN12p	GND	GND	NIC
9	NIC	TXEN	TXDIS	GND	GND	GND	GND	GND	GND	NIC
10	NIC	NIC	NIC	NIC	NIC	NIC	NIC	NIC	NIC	NIC
Smaller connector orientation feature/key										
Note: NIC is no internal connection, reserved for future use.										

3.2.2 Tx MTP connector (front view of module)

FRONT VIEW – MTP KEY IS UP											
CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
User PCB below											

3.3 Signaling timing diagrams

Figure 10 Transmit fault

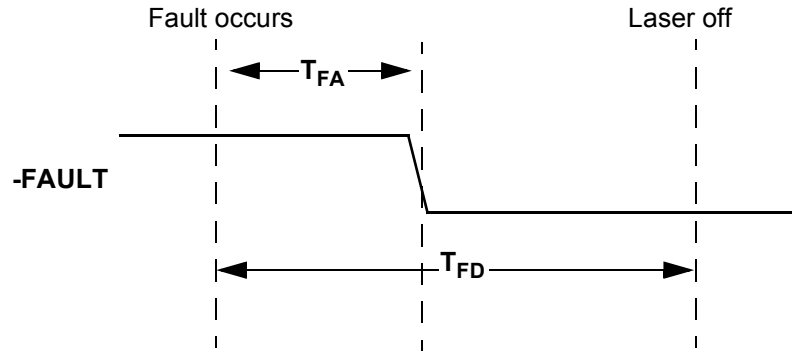


Figure 11 Transmit startup and reset

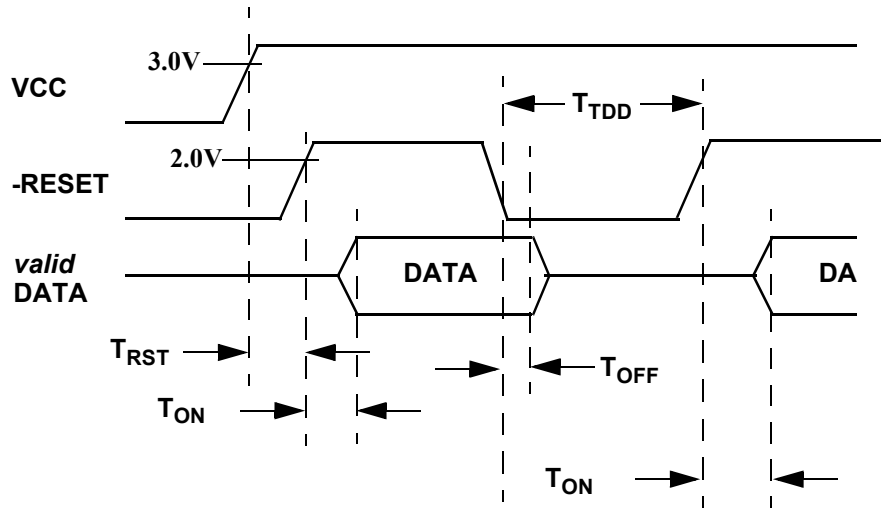


Figure 12 Transmit enable/disable

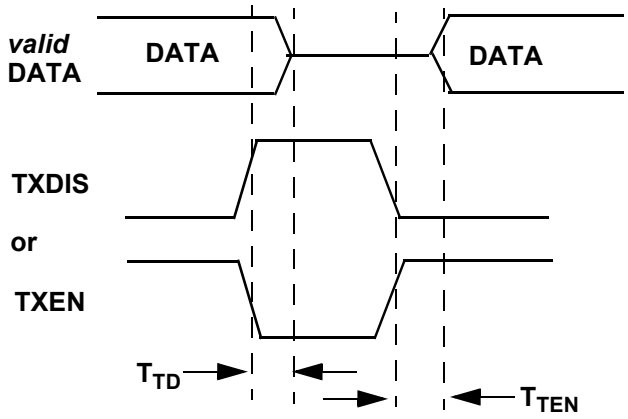


Figure 13 Receive data signal detect

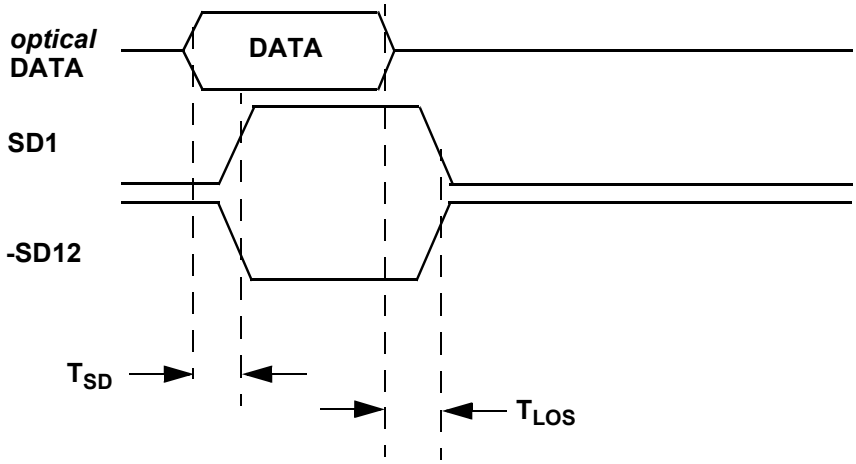
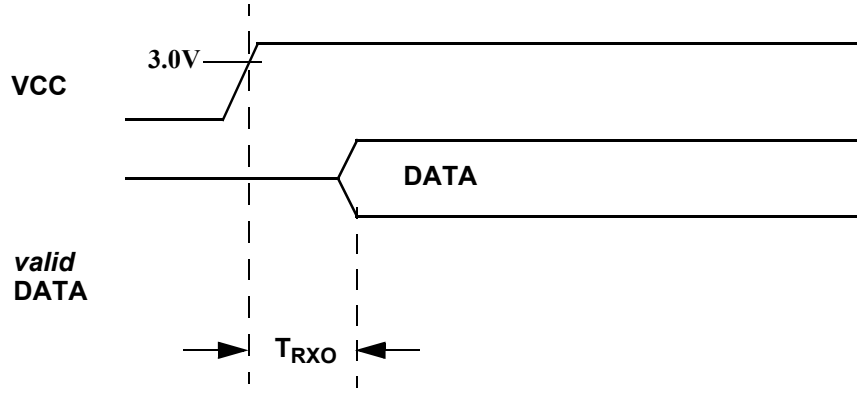


Figure 14 Receive startup timing



3.4 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Storage Temperature	T_{st}	-20 to +100	°C
Transmitter Operating Case Temperature	T_{CTX}	0 to +80	°C [5]
Receiver Operating Case Temperature	T_{CRX}	0 to +90	°C [5]
Power Supply Voltage	V_{cc}	-0.3 to +4.5	V
Transmitter Differential Input Voltage	V_D	2.0 (SNAP12 MSA = 1.4)	V
Input Voltage Range	V_{IR}	-0.5 to Vcc + 0.5	V
Electrostatic Discharge	ESD	1000	V
Relative Humidity	RH	5% to 95% non-condensing	

3.5 Electrical characteristics

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 90°C, Vcc = 3.15V to 3.45V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes[1]
Supply Voltage	Vcc	3.15	3.3	3.45	V	
Data Rate	D_{TR}	0.5		1.6/2.5/ 2.72	Gbps	BER < $1x10^{-12}$ SONET
Power Supply $Noise_1$	N_{P1}			10	mV_{p-p}	@ 1KHz to 1MHz
Power Supply $Noise_2$	N_{P2}			100	mV_{p-p}	@ 1MHz to 2GHz
Transmitter						
Supply Current	I_{CCT}		350	450	mA	SNAP12 MSA = 500 mA max
Power Consumption	P_I		1.2	1.6	W	SNAP12 MSA = 1.75 W max
Data Input Voltage Swing	V_{TDp-p}	200		2000	mV_{p-p}	Differential, peak to peak SNAP12 MSA = 800 mV max
Data Input Range	V_{INR}	825		Vcc	mV	
Data Input Rise/Fall Time	t_{INR}/t_{INF}	100		200	ps	20% - 80%, Differential

3.5 Electrical characteristics (continued)

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 90°C, Vcc = 3.15V to 3.45V)

Parameter	Symbol	Min	Typical	Max	Unit	Notes[1]
Data Input Skew	t_{INS}	0		30	ps	Single Channel, Data/$\overline{Data}$
Transmit Control Signal Voltage Level (LVCMOS)	V_{IH}	2		Vcc	V	
	V_{IL}	0		0.8	V	
Transmit Disable/Enable Assert Time	T_{TD}			10	µs	See Figure 12, "Transmit enable/ disable," on page 15
	T_{TEN}			1	ms	
Transmit Disable Duration	T_{TDD}	10			µs	See Figure 11, "Transmit startup and reset," on page 15
Transmit Reset Time	T_{RST}	10			µs	See Figure 11, "Transmit startup and reset," on page 15
	T_{ON}			100	ms	
	T_{OFF}			10	µs	
Transmit Fault Time	T_{FA}			10	µs	See Figure 10, "Transmit fault," on page 14 SNAP12 MSA = 100 µs max for T_{FA} and T_{FD}
	T_{FD}			10	µs	
Receiver						
Supply Current	I_{CCR}		300	350	mA	SNAP12 MSA = 450 mA max
Power Consumption	P_R		1.0	1.2	W	SNAP12 MAS = 1.5 W max
Data Output Voltage Range	V_{DOR}	Vcc -2.1		Vcc +0.5	V	
Data Output Voltage Swing	V_{DOS}	450		800	mV_{p-p}	R_{LOAD} = 100 Ω, Differential
Data Output Rise/Fall Time			100	150	ps	20% - 80%, Differential
Data Output Skew				30	ps	R_{LOAD} = 100 Ω, Intra Channel, Differential
Data Output Impedance	R_{OL}		200		Ohm	Differential, does not include pull-up resistors
Data Output Deterministic Jitter				0.14	UI	±K28.5 pattern, [1,6]
Data Output Total Jitter				0.33	UI	2^{23}-1 pattern, BER < $1x10^{-12}$, [1,6] SNAP12 MSA = 0.39 UI max
Control Signal Output Current High (LVCMOS)	I_{COH}			0.5	mA	
Control Signal Output Current Low (LVCMOS)	I_{COL}			4.0	mA	
Signal Detect Voltage Level	V_{OH}	Vcc -1.0		Vcc	V	[2]
	V_{OL}	0		0.8	V	
Signal Detect/Loss of Signal Assert Time	T_{SD}			10	µs	See Figure 13, "Receive data signal detect," on page 15 SNAP12 MSA = 50 µs typ. for T_{SD} and T_{LOS}
	T_{LOS}			10	µs	
Receive Reset Time	T_{RXO}			500	ms	See Figure 14, "Receive startup timing," on page 16

See Specification notes on page 19.

3.6 Optical characteristics

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 90°C, Vcc = 3.15V to 3.45V)

Parameter	Symbol	Min.	Typical	Max	Unit	Notes[1]
Transmitter						
Wavelength	λ_p	840	850	860	nm	
RMS Spectral Width	$\Delta\lambda$		0.5	0.65	nm	SNAP12 MSA = 0.85 nm max
Average Optical Power	P_{AVG}	-8.0		-1.5	dBm	
Average Optical Power, disabled				-30	dBm	
Optical Output Rise/Fall Time	$t_{rise/fall}$			160	ps	20% - 80%, unfiltered
Optical Modulation Amplitude	OMA	190			μW	Equivalent to 6dB ER at P_{AVG} = -8dBm
Deterministic Jitter	DJ			0.14	UI	±K28.5 pattern, [1,6]
Total Jitter	TJ			0.33	UI	2^{23}-1 pattern, BER<$1x10^{-12}$, [1,6]
Channel to Channel Skew	T_{C-C}			200	ps	
Relative Intensity Noise	RIN		-130	-117	dB/Hz	1GHz, 12 dB reflection
Receiver						
Wavelength	λ	830	850	860	nm	
Optical Input Power	Po			-1.5	dBm	SNAP12 MSA = 2.5 dBm max
Sensitivity	S			-16	dBm	[3]
Stressed Sensitivity	S_S		-14	-12	dBm	[4]
Signal Detect Assert/Negate Level	SD_A		-21	-17	dBm	Chatter Free Operation SNAP12 MSA = SD_N -30 dBm min
	SD_N	-27	-23		dBm	
Signal Detect Hysteresis	SD_A-SD_N	1	1.7	4	dB	
Low Frequency Cutoff	F_C	25		160	kHz	-3 dB, P<-16 dBm
Optical Modulation Bandwidth	BW			2500	MHz	-3 dB, P<-16 dBm
Optical Return Loss		12			dB	

See Specification notes on page 19.

3.7 Link length

(T_{CTX} = 0°C to 80°C, T_{CRX} = 0°C to 90°C, Vcc = 3.15V to 3.45V)

Data Rate / Standard	Fiber Type	Modal Bandwidth @ 850 nm (MHz*km)	Distance Range (m)	Notes
2.5Gbps 2.488Gbps / OC-48	62.5/125 μm MMF	200	0 to 150	
	50/125 μm MMF	500	0 to 325	
	50/125 μm MMF	900	0 to 500	
	50/125 μm MMF	1500	0 to 650	

Specification notes

1. UI (Unit Interval): one UI is equal to one bit time. For example, 2.488 Gbits/s corresponds to a UI of 408 ps.
2. For SD_A and SD_N definitions, see Signal Detect Assert/Negate Level in Section 3.6 Optical characteristics on page 18.
3. Sensitivity and saturation parameters using a Pseudo Random Bit Sequence (PRBS) 2^{23} - 1, an extinction ration (ER) greater than 6 dB and a maximum bit error rate (BER) of 10^{-12}. For sensitivity measurements, the maximum BER shall be maintained in the presence of the maximum crosstalk penalty. The maximum crosstalk possibility is defined as the 'victim' receiver channel operating at its sensitivity limit and remaining eleven the 'aggressor' receiver channels being actively driven at 6 dB higher incident power and 2.72 Gbps data rate. The minimum average optical power and minimum extinction ratio is equivalent to 30 μW Optical Modulation Amplitude (OMA).
4. Measured with stressed eye pattern as per IEEE 802.3z (Gigabit Ethernet), sec. 38.6.11.
5. Typical ambient temperature with no air flow is 65°C to result in 80°C case temperature.
6. Jitter specified assumes no input signal jitter. Ethernet model has the following budget:

	DJ (UI)	TJ (UI)
Tx Input budget	.1	.21
Tx Output budget	.21	.43
Rx Input budget	.2	.47
Rx Output budget	.38	.65

7. Performance specified with all 12 channels carrying asynchronous PRBS data.

3.8 Regulatory compliance

The PL-xCP-00-SD3 / S53 / SE3 complies with common ESD, EMI, Immunity, and Component recognition requirements and specification (see details in Table 1 on page 19).

ESD, EMI, and Immunity are dependent on the overall system design. Information included herein is intended as a figure of merit for designers to use as a basis for design decisions.

Table 1 Regulatory compliance

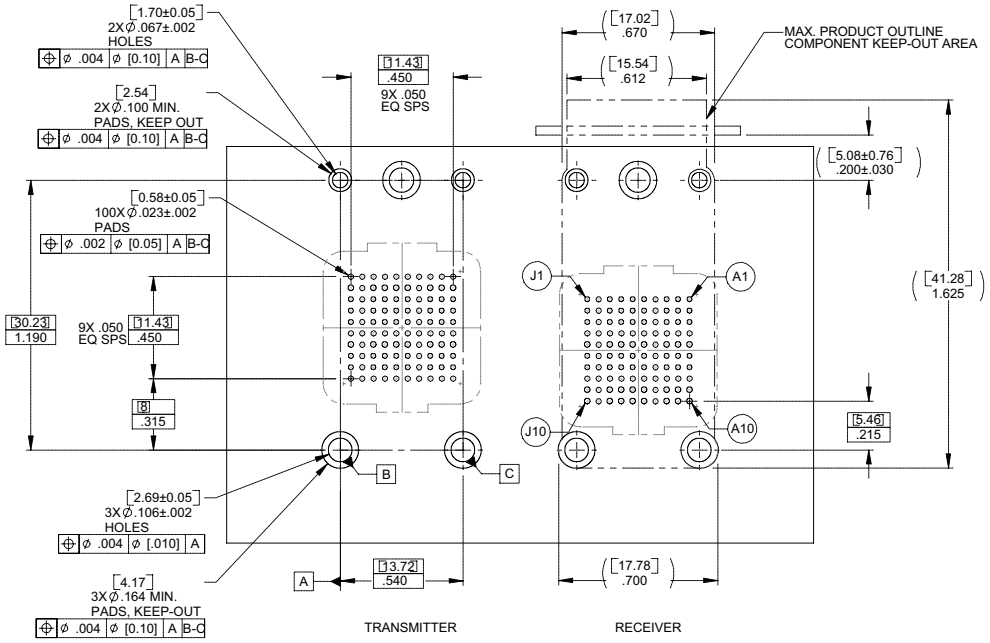
Feature	Test Method	Comments
Laser Eye Safety	IEC 60825-1 1988 + IEC 60825-1 Amendment 2 (2001-01) CDRH 21CFR 1040.10 and 1040.11	Class 1M TUV Certificate #
Electrostatic Discharge (ESD) to electrical pins	MIL-STD 883C; Method 3015.4	Class 1 (> 1 kV)
Electrostatic Discharge (ESD) to optical connector	IEC 61000-4-2: 1999	Withstand discharges of 15 kV using a "Human Body Model" probe

Table 1 Regulatory compliance (continued)

Feature	Test Method	Comments
Electromagnetic Interference (EMI)	FCC Part 15 Subpart J Class B CISPR 22: 1997 EN 55022: 1998 Class B VCCI Class I	Noise frequency range: 30 MHz to 10 GHz. Good system EMI design practice required to achieve Class B margins.
Radiated Immunity	IEC 61000-4-3: 1998	Field strength of 3 V/m RMS, from 80 MHz to 1 GHz. No effect on transmitter/receiver performance is detectable between these limits.
Component	UL 1950 CSA C22.2 #950 IEC 60950: 1999	UL File # CSA File # TUV Certificate #

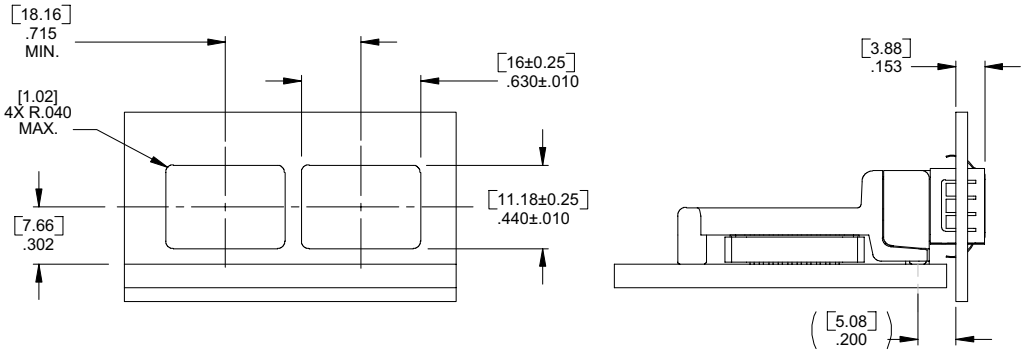
3.9 PCB layout

Figure 15 Top view



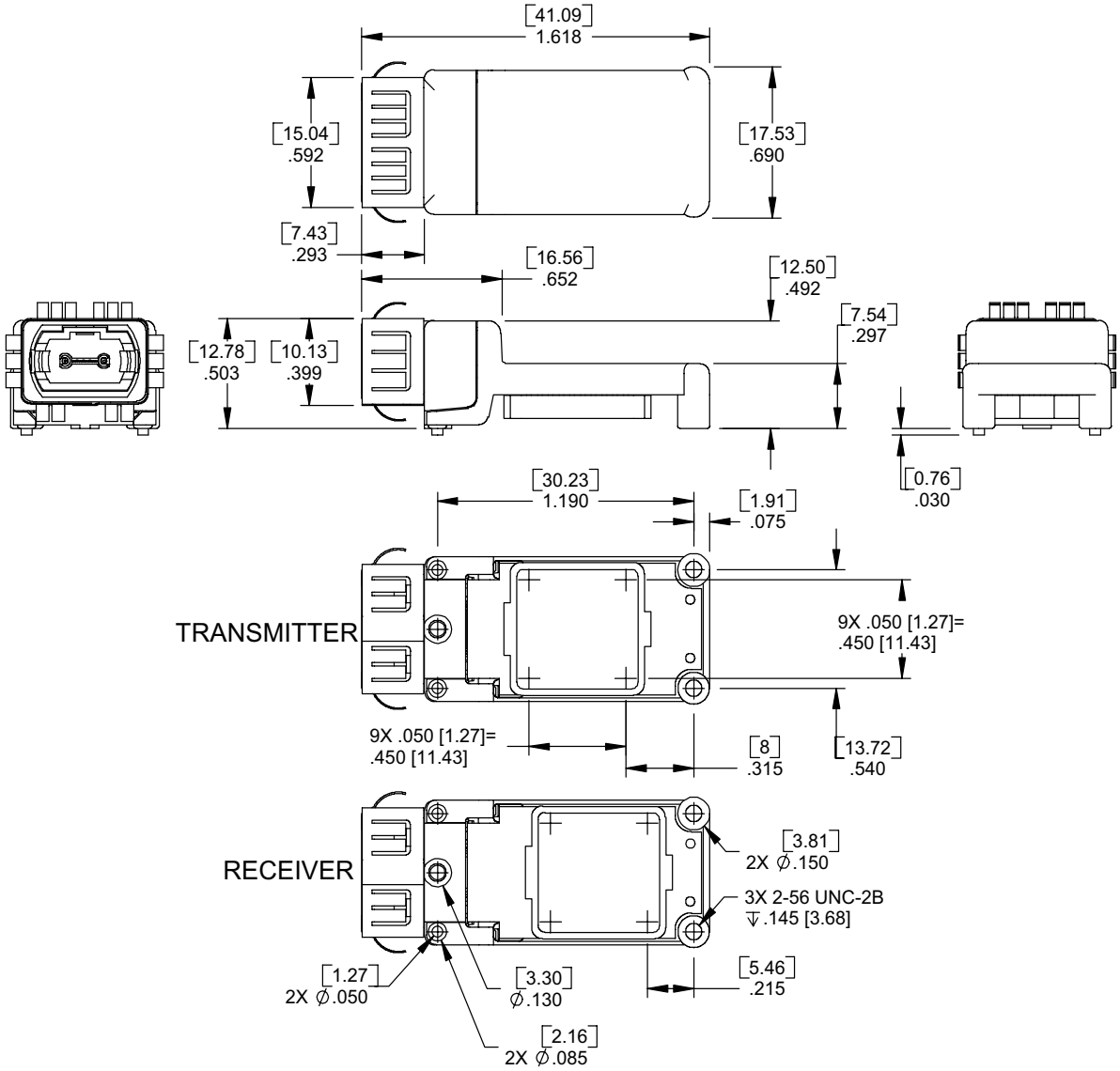
3.10 Front panel opening

Figure 16



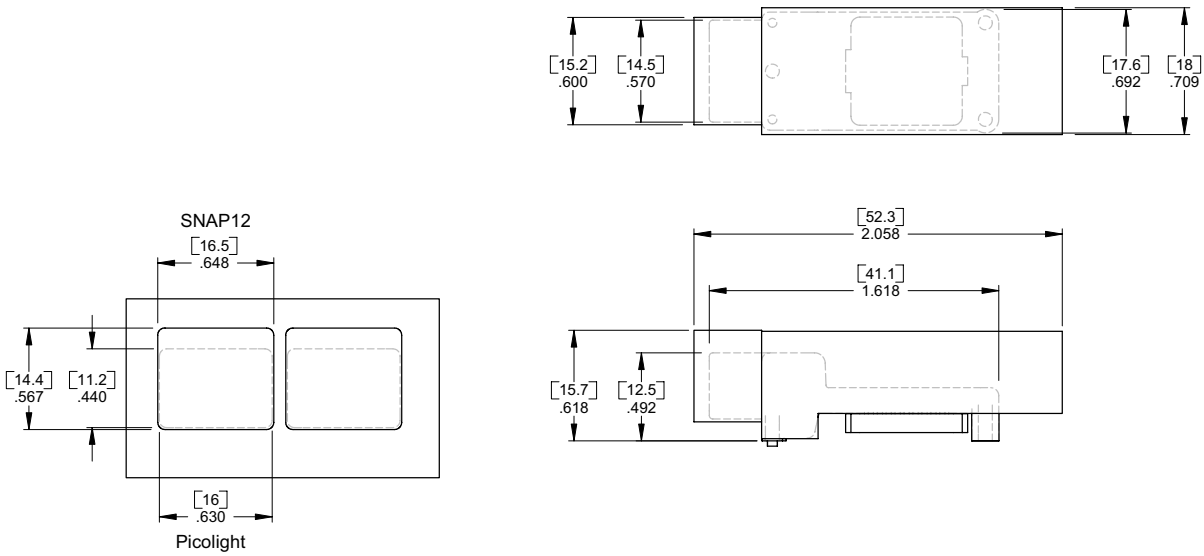
3.11 Module outline

Figure 17



3.12 Mechanical comparison to SNAP12 MSA

Figure 18



Note: The diagram above shows the mechanical outline of PL-xCP-00-Sx3 modules to the SNAP12 MSA maximum mechanical outline. The Picolight module is indicated in gray.

3.13 Host connector information

Optical	MTP Industry Standard - female
Electrical	MEG-Array #84512 manufactured by FCI/Berg

Section 4 Related information

Other information related to the 12x1.6 / 2.5 / 2.7 Gbps Parallel Optical Transmitter/Receiver includes:

- Section 4.1 Package and handling instructions below
- Section 4.2 ESD discharge (ESD) below
- Section 4.3 Eye safety on page 24

4.1 Package and handling instructions

Process plug

The PL-xCP-00-SD3 / S53 / SE3 is supplied with a process plug. This plug protects the transmitter/ receiver's optics during standard manufacturing processes by preventing contamination from dust or other airborne particles.

Note: It is recommended that the process plug remain in the transmitter/receiver whenever an optical fiber connector is not inserted.

Recommended solder and wash process for host BGA connector

PL-xCP-00-SD3 / S53 / SE3's mating BGA connector is compatible with standard industry wave solder, hand solder and wash processes. Air knife drying is recommended.

The BGA connector pickup cap must be installed during these process steps.

Recommended cleaning and de-greasing chemicals

Picolight recommends the use of methyl, isopropyl and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (e.g. trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrolldone).

Flammability

The PL-xCP-00-SD3 / S53 / SE3 housing is a zinc casting.

4.2 ESD discharge (ESD)

Handling

Normal ESD precautions are required during the handling of this module. This transmitter or receiver is shipped in ESD protective packaging. It should removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and operation

In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transmitter/receiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

Typical of optical transmitter/receivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization at the higher layers (e.g. Serializer/Deserializer chip).

4.3 Eye safety

The PL-TCP-00-SD3 / S53 / SE3 is a Class 1M Laser Product per IEC/EN 60825-1:2001 and complies with CDRH 21CRF 1040.10 and 1040.11 except for deviations pursuant to Laser Notice no. 50, dated 5/27/2001. The PL-TCP-00-SD3 / S53 / SE3 is an eye safe device when operated within the limits of this specification.

Operating this product in a manner inconsistent with intended usage and specification may result in hazardous radiation exposure.

CAUTION!

Tampering with this laser-based product or operating this product outside the limits of this specification may be considered an act of "manufacturing," and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration.