Digital Diagnostic Monitoring Interface (DMI) on Avago Enterprise and Storage Fiber Optic Transceivers: Applications and Implementation

Application Note 5016

Introduction

The present application note describes Avago's transceiver implementation of an enhanced digital diagnostic interface, compliant to the "Digital Diagnostic Monitoring Interface for Optical Transceivers" SFF-8472 Multi-Source Agreement (MSA.) The document also outlines the range of application options, both hardware and software, available to the host system for exploiting the digital diagnostic features of the transceiver. The enhanced digital interface allows real-time access to device operating parameters, and includes optional digital features such as soft control and monitoring of SFP I/O signals. In addition, it fully incorporates the functionality needed to implement digital alarms and warnings, as defined by the SFF-8472 MSA. With the digital diagnostic monitoring interface, the user has capability of performing component monitoring, fault isolation and failure prediction functions on their transceiver based applications.

As stated in the SFF-8472 MSA, the diagnostic monitoring interface (DMI) is an extension of the serial ID interface defined in the GBIC specification, as well as the SFP MSA. Both specifications define a 256-byte memory map in EEPROM that is accessible over a two-wire serial interface at the 8-bit address 1010000X (0xA0). The digital diagnostic monitoring interface makes use of the 8-bit address 1010001X (0xA2), so the originally defined serial ID memory map remains unchanged. The interface is backward compatible with both the GBIC specification and the SFP MSA.

Mechanics and Definitions of the Digital Diagnostic Monitoring Interface (DMI)

DMI MSA defined EEPROM pages (0xA0 and 0xA2): byte definitions, features and functionality

The diagnostic monitoring interface outlined in the SFF-8472 DMI MSA [1] is an extension of the serial ID interface defined in the GBIC specification, as well as the SFP MSA. Both specifications define a 256-byte memory map in EEPROM that is accessible over a two-wire serial interface at the 8-bit address 1010000X (0xA0). The bulleted items below outline how the host software interface defined in the DMI MSA differs from normal SFP:

- There are now two 256-byte pages of memory, accessible at serial addresses 0xA0 and 0xA2.
- 0xA0 memory page (as in GBIC/SFP definition) remains with few minor updates in information.
- Address 0xA2 memory page contains all DMI feature sets.
- Write operations are now allowed (on specific 0xA2 bytes)
- 0xA0 remains read-only
- 0xA2 has 2 writeable control bytes and 120 customer writeable bytes.
- Read operations for parametric sensors require additional care:
  - each value is stored in two bytes (MSB and LSB) which must be "coherent"
  - simple math operation by the host is needed to "scale" each sensor value.
- Periodic polling of the 0xA2 memory contents is required to monitor diagnostics:
  - alarm & warning flag bytes are available in 0xA2 to serve as indicators of transceiver health
  - real time parametric sensors can be accessed on 0xA2.

0xA0 byte definitions

Table 1 illustrates the serial ID byte definitions for DMI transceiver memory page 0xA0 (per DMI MSA.) Except for a few additions, DMI MSA byte definitions are the same as those in original GBIC and SFP MSAs[2]. 0xA0 bytes 3-10 (Standard Compliance codes) definitions have been updated in DMI MSA to include InfiniBand, in addition to Fibre Channel, Sonet and Ethernet, and to indicate Sonet reach. In addition, bytes 60-61 (previously reserved) have been defined in DMI MSA to indicate laser wavelength.

Bytes 92-94 (previously reserved on SFP MSA) have been defined to indicate DMI features and DMI MSA compliance of a transceiver:

– Byte 92 is used to indicate diagnostic monitoring type. Table 2 illustrates the definition of each one of the bits on byte 92. Bit 6 is used to indicate whether or not the transceiver has DMI functionality. Bits 4-5 indicate the type of diagnostic monitor parameter calibration that is implemented in the module (external or internal.) From a host software perspective, internal calibration (indicated by transceiver if bit 5 is set to '1') requires simple host scaling by a parameter unit per LSB factor (defined in DMI MSA.) If bit 4 is set to '1', external calibration is required, which involves more complex math from host to add slopes and offsets to the transceiver's raw A/D parameter values. Bit 3 is used to indicate the RX power measurement type implemented by the transceiver (average or OMA.) Bit 2, if set to '1', indicates that an I2C General Call is required from host to change address from 0xA0 to 0xA2 [4].

– Byte 93 is the DMI enhanced options byte, used to indicate which optional DMI functionality is implemented on a transceiver. Table 3 illustrates the bit definitions.

– Byte 94 contains an unsigned integer that indicates which feature set(s) are implemented in the transceiver (see Table 4.)

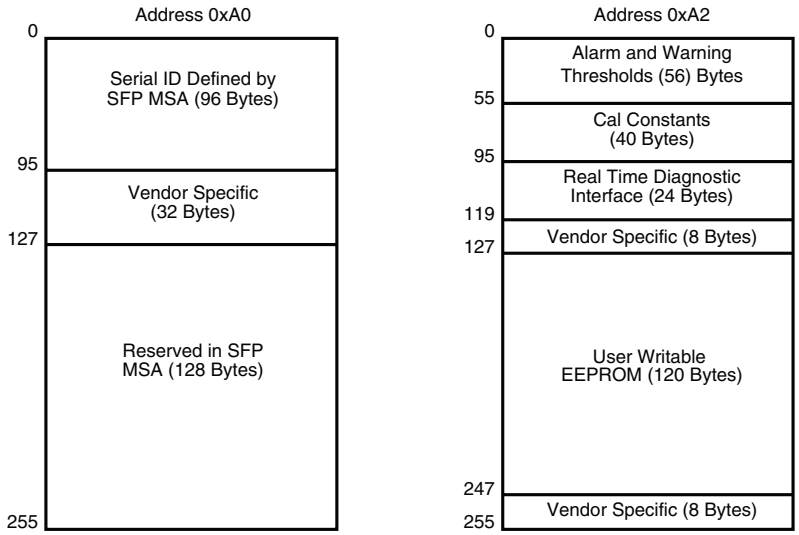

Figure 1. Digital diagnostic memory map – specific data field descriptions (from SFF-8472 MSA).

Table 1. Serial ID data fields – Address 0xA0 (from SFF-8472 MSA).

Data Address	Size (Bytes)	Name of Field	Description of Field
			BASE ID FIELDS
0	1	Identifier	Type of serial transceiver (see table 3.2)
1	1	Ext. Identifier	Extended identifier of type of serial transceiver (see table 3.3)
2	1	Connector	Code for connector type (see table 3.4)
3-10	8	Transceiver	Code for electronic compatibility or optical compatibility (see table 3.5)
11	1	Encoding	Code for serial encoding algorithm (see table 3.6)
12	1	BR, Nominal	Nominal bit rate, units of 100 Mbits/sec.
13	1	Reserved	
14	1	Length (9µm) km	Link length supported for 9/125 Ïm fiber, units of km
15	1	Length (9µm)	Link length supported for 9/125 Ïm fiber, units of 100m
16	1	Length (50µm)	Link length supported for 50/125 Ïm fiber, units of 10m
17	1	Length (62.5µm)	Link length supported for 62.5/125 Ïm fiber, units of 10m
18	1	Length (Copper)	Link length supported for copper, units of meters
19	1	Reserved	
20-35	16	Vendor name	SFP vendor name (ASCII)
36	1	Reserved	
37-39	3	Vendor OUI	SRP vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by SFP vendor (ASCII)
58-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-61	2	Wavelength	Laser wavelength
62	1	Reserved	
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
			EXTENDED ID FIELDS
64-65	2	Options	Indicates which optional transceiver signals are implemented (see Table 3.7)
66	1	BR, max	Upper bit rate margin, units of %
67	1	BR, min	Lower bit rate margin, units of %
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date Code	Vendor's manufacturing date code (see Table 3.8)
92	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 3.10)
93	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 3.10)
94	1	SFF-8472 Compliance	Indicates which revision of SFF8472 the transceiver complies with (see Table 3.12)
95	1	CC_EXT	Check code for the Extended ID Fields addresses 64 to94)
			VENDOR SPECIFIC ID FIELDS
96-127	32	Vendor Specific	Vendor Specific EEPROM
128-255	128	Reserved	Reserved for future use

Note:
Section References in Table 1 refer to the document "SFF-8472 Digital Diagnostic Monitoring Interface MSA document Revision 9.3"

Table 2. Diagnostic monitoring type 0xA0 byte 92 bit descriptions (from SFF-8472 MSA).

Data Address	Bits	Description
92	7	Reserved for legacy diagnostic implementations. Must be '0' for compliance with this document.
92	6	Digital diagnostic monitoring implemented (described in this document). Must be "1" for compliance with this document.
92	5	Internally Calibrated
92	4	Externally Calibrated
92	3	Received power measurement type 0 = OMA, 1 = Average Power
92	2	Address change required see section above, "addressing modes"
92	1-0	Reserved

Table 3. Enhanced options byte 0xA0 byte 93 bit descriptions (from SFF-8472 MSA).

Data Address	Bits	Description
93	7	Optional Alarm/warning flags implemented for all monitors quantities (see table 3.18)
93	6	Option Soft TX_DISABLE control and monitoring implemented
93	5	Optional Soft TX_FAULT monitoring implemented
93	4	Optional Soft RX_LOS monitoring implemented
93	3	Optional Soft RATE_SELECT control and monitoring implemented
93	2-0	Reserved

Table 4. DMI functionality byte 0xA0 byte 94 description (from SFF-8472 MSA).

Data Address	Value	Interpretation
94	0	Digital diagnostic functionality not included or undefined.
94	1	Includes functionality described in Rev 9.3 SFF-8472.
94	2	TBD
94	3	TBD

0xA2 byte definitions

With respect to the memory bytes available at two-wire serial address 0xA2, there are four functional sub-categories of interest, as it relates to Avago's storage and enterprise DMI transceivers:

a) real-time digital diagnostic sensors – bytes 96-105
b) alarm and warning thresholds and flags – bytes 0-55 and 112-119 respectively
c) soft status and control I/O functional byte – byte 110
d) customer writeable memory space – bytes 128-247

a) Real-time digital diagnostic sensors

Via the two wire serial interface, the user can access real-time internal measurements of the transceiver temperature, supply voltage, transmitter bias current, transmitter output power, and received optical power. The real-time measurement information is stored on bytes 96 through 105 of address 0xA2. The DMI MSA allows the sensor byte values to be interpreted differently depending upon the option bits set at address 92 of address 0xA0. If bit 5 (internal calibration) is set, (such as the case of Avago DMI transceivers), the values are calibrated absolute measurements. If bit 4 (external calibration) is set, the values are A/D counts, which are converted into real values by adding slopes and offsets per "External Calibration" section of SFF-8472 DMI MSA. The following sensor byte definitions and formats (per SFF-8472 MSA) apply to internally calibrated DMI devices such as Avago's DMI transceivers. The host must translate and scale sensor byte data per the definitions below, to obtain real monitor values:

1) Internally measured transceiver temperature – Represented as a 16-bit signed two's complement value, in increments of 1/256° C. Byte 96 is temp MSB (most significant byte), byte 97 is temp LSB (least significant byte.) MSA defines an accuracy of ±3° C.
2) Internally measured transceiver supply voltage (Vcc) – Represented as a 16-bit unsigned integer with the voltage defined as the full 16 bit value (0 to 65535) with least significant bit equal to 100 μV. Byte 98 is Vcc MSB, Byte 99 is Vcc LSB. Accuracy per MSA must be ±3%.
3) Measured TX bias current in μA – Represented as a 16 bit unsigned integer with the current defined as the full 16-bit value (0 to 65535) with least significant bit equal to 2 μA. Byte 100 is the TX bias MSB, byte 101 is TX bias LSB. Accuracy per MSA must be ±10% of nominal value (defined by vendor.)
4) Measured TX output power in mW – Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with least significant bit equal to 0.1 μW. Byte 102 is TX power MSB, Byte 103 is TX power LSB. Accuracy per MSA must be ±3 dB.
5) Measured RX received optical power in mW – Value can represent either average received power or OMA depending how bit 3 of byte 92 (0xA0) is set. Represented as a 16-bit unsigned integer with the power defined as the full 16-bit value (0 to 65535) with the least significant bit equal to 0.1 μW. Byte 104 is RX power MSB, Byte 105 is RX power LSB. Accuracy per MSA must be ±3 dB.

Note: For all digital diagnostic monitors, parameters such as operational range, resolution, measurement point (in the case of supply voltage and temperature sensors), update frequency, linearity are vendor specific and depend on intended application.

b) Alarm and warning thresholds and flags

For the five digital diagnostic read-backs defined in the SFF-8472 MSA (supply voltage, transceiver temperature, RX OMA power, TX average optical power, and TX bias current), corresponding high alarm, low alarm, high warning and low warning thresholds are also defined. Bytes 00-55 in address 0xA2 are allocated, per MSA definition (see Figure 1 in the beginning of document) for the purpose of storing these threshold values in the transceiver's memory. The threshold values, which are typically defined by the vendor and factory preset, allow the user to determine whether or not the transceiver is operating outside target limits for desired performance.

In addition to alarm and warning thresholds, the DMI MSA allocates bytes 112-119 of address 0xA2 for storing of an optional set of alarm and warning flags. As defined in the MSA, there are two types of flags:

1) Alarm flags, which indicate conditions likely to be associated with a non-operational link, and which are causes for immediate action.
2) Warning flags, which indicate conditions outside the normally guaranteed bounds, but not necessarily causes of immediate link failures.

When the alarm and warning feature is enabled (indicated by 0xA0 byte 93), the transceiver, in addition to cyclically performing internal measurements of the diagnostic read-back parameters and digitally storing on memory, also checks how these read-back values compare with programmed alarm/warning threshold values. If the diagnostic read-back value falls outside range delimited by thresholds, the transceiver sets a corresponding soft flag. The alarm and warning functionality gives the user an alternative to directly polling the diagnostic read-back values to monitor transceiver performance, saving the user the work needed to interpret the diagnostic read-back data. By continually polling the alarm and warning flag bytes via its system software, the user has the power to better screen transceiver performance, so as to avoid the occurrence of link failures and potential system downtime.

Note: On Avago DMI transceivers, alarm and warning flags are **unlatched**; in other words, if monitored parameter once again reads values within limits, flag will be de-asserted.

c) Soft status and control I/O functional byte

Byte 110 of address 0xA2 is an optional byte defined by DMI MSA which gives the host a tool for implementing transceiver status & control I/O functionality over two-wire serial interface. In other words, it is a "soft" mirroring of the traditional status and control I/O functionality implemented via hardware. Table 5 illustrates the functionality of each of the eight bits of byte 110.

The functional capability of the bits of byte 110 (per DMI MSA definition) is outlined below:

– Status flags (display of auxiliary signal status) - Tx_Disable state, Rx_LOS state, Tx_Fault state, Rx_Rate state

– Control bits (allow switching of state of signals by changing logic state of bit): Rx_Rate assert/de-assert, Tx_Disable assert/de-assert

d) Customer write enabled memory space

Bytes 128-247 on address 0xA2 are defined by DMI MSA as user writeable EEPROM. In other words, these bytes are meant to serve as non-volatile memory space for storing customer information.

Table 5. Soft status and control I/O byte 0xA0 byte 110 functional bit description.

110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100 msec of change on pin.
110	6	Soft TX Disable	Read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100 msec max from acknowledgement of serial byte transmission. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.
110	5	Reserved	
110	4	RX Rate Select State	Digital state of the SFP RX Rate Select Input Pin. Updated within 100 μsec of change on pin.
110 rate	3	Soft RX Rate Select	Read/write bit that allows software RX rate select. Writing '1' selects full bandwidth operation. This bt is "OR"d with the hard RX RATE_SELECT pin value. Enable/disable time is 100 μsec max from acknowledgement of serial byte transmission. Soft RX select does not meet the auto-negotiation requirements specified in FC-FS. Default at power up is zero. If Soft RX Rate Select is not implemented, the transceiver ignores the value of this bit.
110	2	TX Fault	Digital state of the TX Fault Output Pin. Updated within 100 μsec of change on pin.
110	1	LOS	Digital stated of the LOS Output Pin. Updated within 100 μsec of change on pin
110	0	Data_Ready_Bar	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.

Two-wire serial bus functionality and timing

Start/Stop conditions, signaling and addressing
To define the data transfer format and timing characteristics needed for communication with DMI transceivers via the two-wire serial interface, the SFF-8472 DMI MSA references the Atmel AT24C01A/02/04 EEPROM family's two-wire serial protocol. Below are the basic details of Atmel protocol two-wire serial communication [3]:

Pin Description
The two pins needed for serial communication are serial clock (SCL) and serial data (SDA.) The SCL input is used to positive edge clock data into each DMI device and negative edge clock data out of each device. The SDA pin is bi-directional for serial data transfer. On DMI devices, SFP MSA defined pin MOD_DEF2 is used to implement SDA, while MOD_DEF1 is used for SCL.

Start/stop conditions and acknowledging
A high-to-low transition of SDA with SCL high is the defined two-wire serial start condition that must precede any other command. A low-to-high transition of SDA with SCL high constitutes a two-wire serial stop condition. All addresses and data transmitted over two-wire serial interface use an 8-bit word format. The two-wire serial receive device must hold data low during ninth clock cycle to signal an "acknowledge", i.e. it has received the eight bit word.

Differences between standard I2C and SFF-8472 MSA (Atmel EEPROM protocol) requirements

Atmel supports 100 kHz only (while I²C specifies both a 100 kHz and 400 kHz mode)

- DMI devices can behave only as a slave device.
- Atmel protocol does not allow for clock stretching.
- Atmel does not support "repeated start" memory write operations i.e. issuing a start condition before a stop condition has been issued on a previous serial operation, an operation allowed by I²C [4]. Figure 2 illustrates a two-wire serial operation where a repeated-start is executed.

AC/DC characteristics of the interface and DMI timing
Table 6 contains the timing requirements relevant to the two-wire serial bus (per Atmel specification [3].) Avago DMI transceivers are compliant with these characteristics.

DMI soft-timings
The "soft" control functions (address 0xA2, byte 110) specified in SFF-8472 DMI MSA and outlined in section 1.1 of the present document (TX_DISABLE, TX_FAULT, RX_LOS, and RATE_SELECT) do not meet the timing requirements specified in the SFP MSA section B3 ("Timing Requirements of Control and Status I/O") for their corresponding hard pins. The soft functions allow a host to poll or set these values over the serial bus as an alternative to monitoring/setting hard pin values. Timing is vendor specific, but must meet the requirements listed in Table 7.

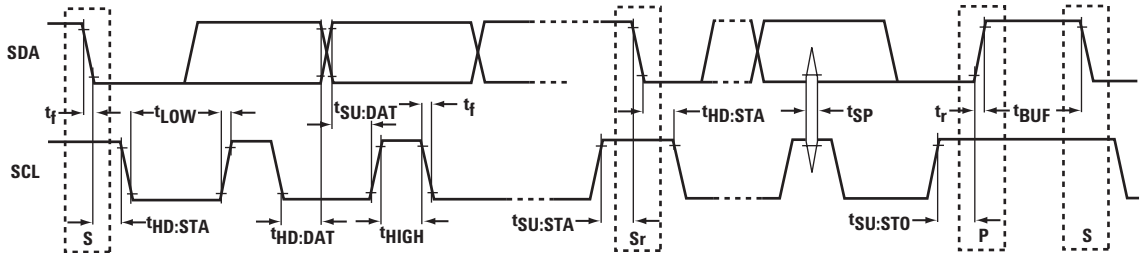

Figure 2. Two-wire serial operation illustrating a repeated start operation (labeled "Sr", from Phillips I²C specification).

Table 6. Two-wire serial bus AC/DC Characteristics.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Output high level	V_{OH}	Vcc∗ 0.7		Vcc + 0.5	V	1, 2
Output low level	V_{OL}	-0.6		Vcc∗ 0.3	V	1, 2
Clock pulse width high	t_{high}	4.0			µs	1
Clock pulse width low	t_{low}	4.7			µs	1
Serial clock frequency	f_{scl}			100	kHz	1,2
Rise time	t_{rise}			1000	ns	1,2
Fall time	t_{fall}			300	ns	1,2
Start hold time	$t_{HD:STA}$	4.0			µs	1
Data in hold time	$t_{HD:DAT}$	0			µs	1,2
Data setup time	$t_{SU:DAT}$	250			ns	1,2
Start setup time	$T_{SU:STA}$	4.7			µs	1
Stop setup time	$t_{SU:STO}$	4.0			µs	1
Write cycle time	t_{WR}			10	ms	2

Notes:

1. In agreement with two-wire serial bus requirements described in Atmel EEPROM protocol specification @ 100 kHz
2. Timing requirement applies to two-wire serial slave devices (other timing only apply to master)

Table 7. I/O Timing for Soft Control & Status Functions (from SFF-8472 MSA).

Parameter	Symbol	Min	Max	Units	Conditions
TX_DISABLE assert time	t_off		100	ms	Time from TX_DISABLE bit set1 until optical output falls below 10% of nominal.
TX_DISABLE de-assert time	t_on		100	ms	Time from TX_DISABLE bit cleared1 until optical output rises above 90% of nominal.
Time to initialize, including	t_init		300	ms	Time from power on or negation of TX_FAULT using reset of TX_Fault TX_DISABLE until transmitter output is stable[2].
TX_FAULT assert time	t_fault		100	ms	Time from fault to TX_FAULT bit set.
LOS assert time	t_loss_on		100	ms	Time from LOS state to RX_LOS bit set.
LOS de-assert time	t_loss_off		100	ms	Time from non-LOS state to RX_LOS bit cleared.
Rate select change time	T_rate_sel		100	ms	Time from change of state of Rate Select bit[1] until receiver bandwidth is in conformance with appropriate specification.
Serial ID clock rate	f_serial_clock		100	kHz	n/a
Analog parameter data ready	t_data		1000	ms	From power on to data ready, bit 0 of byte 100 set.
Serial bus hardware ready	t_serial		300	ms	Time from power on until module is ready for data transmission over the serial bus.

Notes:

1. measured from falling clock edge after stop bit of write transaction
2. See Gigabit Interface Converter (GBIC). SFF-0053. rev. 5.5. September 27, 2000

C) Read and write operations per Atmel protocol [3]

Atmel protocol allows for the following types of two-wire serial operations:

- Single-byte write: A write operation requires an 8-bit data word address following the device address word and slave acknowledgement. Upon receipt of this address, the slave device will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the slave will output a zero and the two-wire serial master must terminate the write sequence with a stop condition. At this time, the DMI slave device enters an internally timed write cycle, t_{WR} (refer to Table 1**)**, to internal memory. The DMI slave device will not respond to two-wire serial operations until the write is complete.
- Page write: Atmel protocol specifies up to 8-byte page write service capability. A page write is initiated the same way as a byte write, but the two-wire serial master does not send a stop condition after the first data word is clocked in. Instead, after the slave device acknowledges receipt of the first data word, the two-wire serial master can transmit up to seven more data words. The slave device will respond with an acknowledgement after each data word is received. The master must terminate the page write sequence with a stop condition.
- Random read: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the slave device, the two-wire serial master must generate another start condition. The master then initiates a read by sending a device address with the read/write select bit high. The slave acknowledges the device address and serially clocks out the data word. The master does not respond with a zero but does generate a following stop condition.
- Sequential read: Sequential reads are initiated when after the master receives a data word during a read operation, it responds with an acknowledge instead of a stop condition. As long as the slave receives an acknowledgement from the master device, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the master does not respond with a zero, but does generate a following stop condition.

System hardware configurations of Two-Wire Serial (TWS) master

Single microcontroller master

A microcontroller is a logical choice for implementing the two-wire serial interface defined in the SFP MSA (whose timing and functional requirements are covered by Atmel protocol specification), and subsequently expanded in the DMI MSA to include diagnostic features. Its flexibility (with respect to functionality that can be implemented via software), speed and processing capability, interrupt generation and support, and on-chip memory make a microcontroller suitable for implementation as a two-wire serial master. Furthermore, the microcontroller's typical low-power consumption, and the maturity of IC process and packaging technology used in manufacture of microcontrollers make these devices attractive from a system design standpoint.

A two-wire serial bus master (any type of master including micro-controller, FPGA, or other) must incorporate the following basic features:

- Two lines (bi-directional serial data line and serial clock output line)
- Clock signal generation capability (up to 100 kHz for standard two-wire serial operation)
- AC/DC characteristics per Atmel EEPROM specification
- Data transfer per Atmel protocol

Controller options

a) Controller with embedded I2C functionality

The two-wire serial interface defined for DMI and non-DMI transceiver applications is compatible with Philips I2C bus specification [4]. The Philips I2C bus protocol is a widely adopted industry standard; hence, commercial microcontrollers and microprocessors with I2C bus functionality embedded in them are readily available. These microcontrollers with embedded I2C typically have sub-routines for implementing two-wire serial start/stop conditions and read/write operations already written, making the development process easier for the system designer. Versions of Motorola microprocessors and Microchip PIC microcontrollers are both available, for example, with such embedded I2C functionality. Avago's HFBR-0534 DMI SFP evaluation board is an example of using a microcontroller as a two-wire serial bus master. The HFBR-0534 DMI SFP evaluation board has an on-board microcontroller that emulates two-wire serial interface commands and functions executed by a master device in a DMI-like environment, to communicate with an SFP transceiver. Figure 3 shows a schematic of the basic hardware implemented on the HFBR-0534 evaluation board to communicate to DMI SFP's over the two-wire serial interface. Please contact Avago for more information regarding the HFBR-0534 DMI SFP evaluation board.

b) I2C bus controller chip from Philips in combination with standard controller or processor

Philips has a wide family of IC's designed to implement standard I2C functionality in a serial bus system. I2C bus controllers such as the Philips PCA9564 and the Philips PCF8584 provide an interface between most standard parallel-bus microcontrollers/microprocessors and the two-wire serial bus [5]. The I2C controller allows the system host to communicate bi-directionally with the I2C bus using a standard micro-controller interface, minimizing the amount of I2C specific hardware/software development and debugging needed. The I2C controller controls all of the I2C bus specific sequences, protocol, arbitration and timing with no external timing element required.

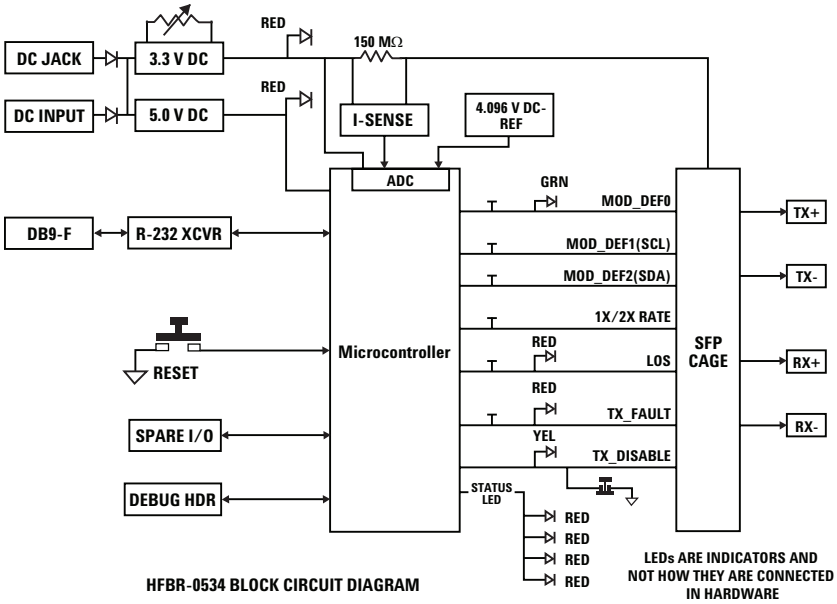

Figure 3. Block diagram of two-wire serial master implementation used on Avago HFBR-0534 DMI SFP Evaluation board.

c) Other Microcontroller

A microcontroller with no embedded two-wire serial bus functionality can be used to implement the two-wire serial interface master. The system designer would then be required to develop hardware and software that properly execute the seven bit addressing, acknowledging, start/stop conditions, voltage levels, timing and all other data transfer requirements of the two-wire serial protocol (per Atmel or I2C specifications) from the ground up.

GPIO interface pins on network protocol IC or ASIC

The controller ICs (i.e. protocol chips) used in fiber optic networking systems to generate Gigabit Ethernet or Fibre Channel data typically have tri-state, bi-directional General Purpose I/O pins (GPIO) available. These pins provide the networking system designer with a basic means for implementing a low-speed serial bus such as the SFP two-wire serial interface. Internal registers on the protocol IC typically control these GPIO pins. Figure 4 shows a typical schematic of a Protocol IC interfacing to a SFP.

Performing the two-wire serial master functionality needed for either a DMI or non-DMI SFP environments using GPIO pins on a protocol IC requires the implementation of a "bit-banging" software scheme. The GPIO pins in a protocol IC typically interface with a control register. Hence, to implement the polling routines needed to communicate to a SFP via the two-wire serial interface, hardware/software control external to protocol IC is needed.

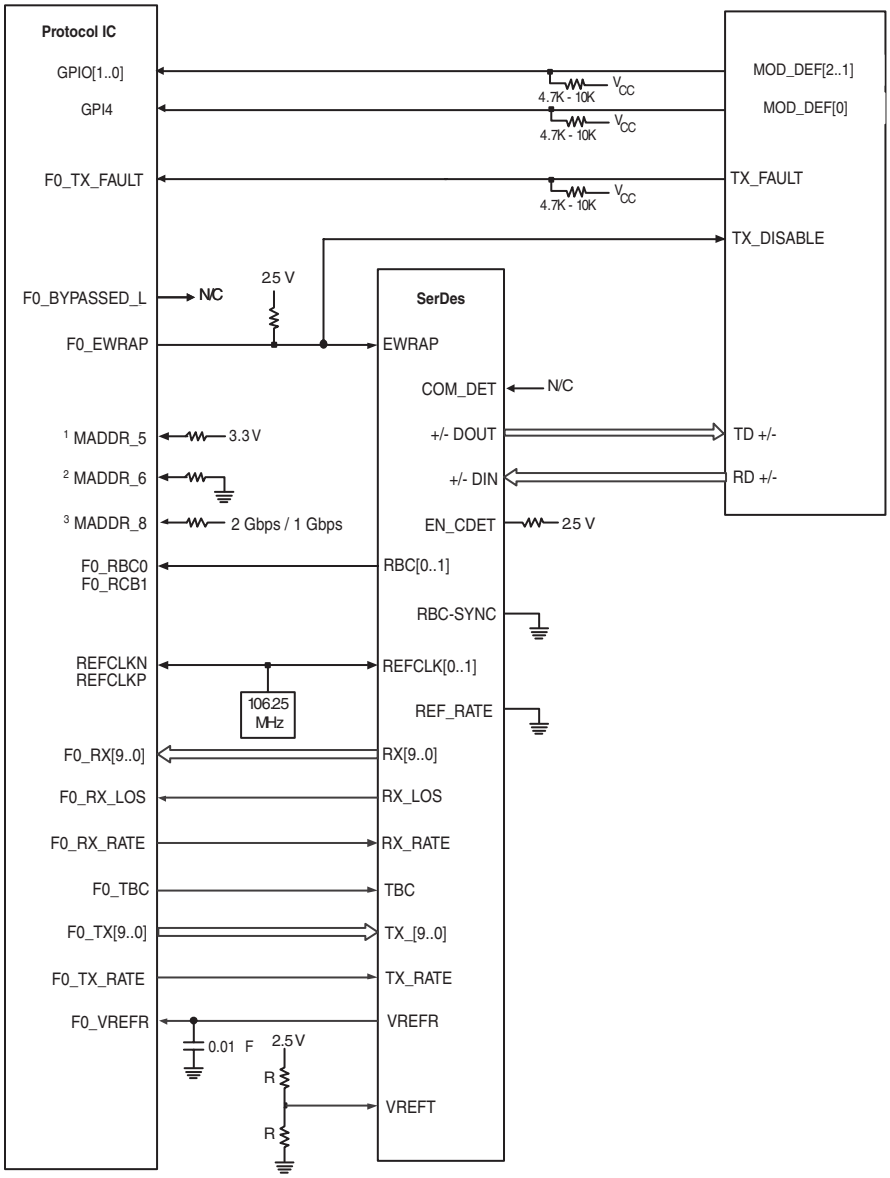

Figure 4. Schematic of a Protocol IC interfacing with a SFP transceiver.

Programmable gate array (PGA) as TWS master

Programmable gate arrays are a viable alternative for implementing the two-wire serial bus functionality needed in a DMI transceiver system. Programmable logic arrays (PLA) and field programmable gate arrays (FPGA) are examples of viable options. Due to its configurable logic, PGAs give great flexibility with respect to functionality and allow application specific customization. FPGAs in particular, because of their unlimited re-programmability, allow, for example, for DMI functionality to be programmed into a FPGA already present in an existing, non-DMI, fiber-optic networking system design.

Two-wire serial bus protocol functionality need not be developed from the ground up on a FPGA based design. Soft IP cores containing two-wire serial bus functionality are available for commercial FPGAs. An I2C soft IP core, for example, is available for incorporation on Xilinx family of FPGAs [3]. The Xilinx I2C soft IP core includes the following two-wire serial bus features, not all of which are supported by SFP/Atmel [6]:

- Master or slave operation
- Multi-master operation
- Software selectable acknowledge bit
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt with automatic mode switching from master to slave
- START and STOP signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus busy detection
- Fast Mode 400 kHz operation or Standard Mode 100 kHz
- 7-bit or 10-bit addressing
- General Call Enable or Disable

Bus expansion or multiplexing

Because DMI SFPs have fixed addresses at 0xA0 and 0xA2, multiple devices cannot be directly supported on a single two-wire serial bus. Via analog switching or multiplexing, nevertheless, the two-wire serial bus can be expanded to allow interfacing with several devices with same two-wire serial address. Figure 5 shows a block diagram of a typical analog switch based multiplexer used for two-wire serial bus expansion. On the diagram in Figure 2, both SDA and SCL are multiplexed using transistor switches to generate eight SDA-SCL pairs. In a typical application, the two-wire serial master would select one of the channels via the two-wire serial bus, in order to communicate to it.

Both SDA and SCL need not be multiplexed in a two-wire serial bus application. SFPs will typically ignore serial clock line if proper serial data is not received and vice-versa. Hence, to expand the serial bus, the system designer could choose to directly route either SDA or SCL to all two-wire serial devices. The system designer then must come up with a scheme to both multiplex the non-routed serial line and to properly address either one of the multiple channels for individual two-wire serial communication.

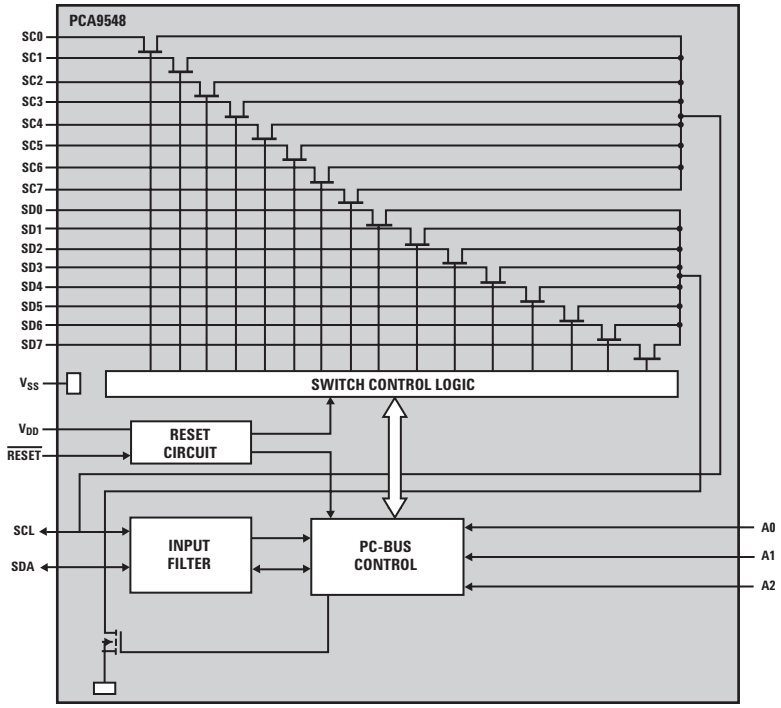

Figure 5. Example block diagram of a two-wire serial bus switch (from Philips "PCA9548 8-channel I2C switch with reset" IC datasheet).

Digital diagnostics implementation for component monitoring, fault isolation and predictive failure

Uses of Digital Diagnostic Read-backs

Overview of applications of DMI

The digital diagnostic monitoring interface gives the host the ability to implement in-situ component monitoring on transceiver applications. Not only can the system user poll the individual parametric read-backs to monitor transceivers, the user can also take advantage of the DMI soft flags, and alarms and warnings to gauge link/transceiver health. Alarm flags signal impending link fault or significant functionality issues. Warning flags are meant to indicate potential compliance violations or non-ideal operating conditions. Soft Flags (bits on address 0xA2, byte 110) offer a mirror of the hard pin state warnings (e.g. TX fault, RX LOS) accessible via the two-wire serial interface.

The uses of the real-time parametric monitoring data can be broken down into the following functional categories with increasing complexity (either at the system software level or transceiver functional level):

Operating Environment Compliance Verification

The real-time diagnostic parameters can be monitored to alert the system when the transceiver's specified operating limits are exceeded and compliance (to standard or datasheet) cannot be ensured. See section 3.2 for an example of implementation of alarms and warnings for compliance verification.

Fault Isolation

The diagnostic information can allow the host to pinpoint the location of a link problem and accelerate system servicing and minimize downtime.

Failure Prediction

The diagnostic information can allow the host system to identify potential link problems. Once identified, a "fail over" technique can be used to isolate and replace suspect devices before system uptime is impacted.

Note: Alarm and warning flag bytes polling versus read-back polling.

DMI devices cannot assert themselves on the system. The host needs to poll the devices to determine module health. To monitor transceivers via DMI, the user can either poll alarm and warning flags, or poll the diagnostic monitors themselves. Polling the alarm and warning flags provides a quick transceiver status update, requiring user to read less total bytes and perform less software based parametric analysis. Polling diagnostic read-backs, nevertheless, allows for closer parametric monitoring and independent failure or drift calculations.

Individual diagnostic monitor parameter descriptions: transceiver temperature, transceiver supply voltage, TX average power, RX OMA power, and TX bias current

Transceiver temperature

The transceiver temperature diagnostic read-back allows monitoring of the DMI transceiver's thermal environment condition. For the transceiver temperature diagnostic monitor, the measurement point is not formally defined by SFF-8472 DMI MSA; Per DMI MSA, location of temperature sensor is to be specified by the vendor. The temperature sensor is commonly located on the transceiver's PCB. If located near ICs, it will read "hotter" than if distant. With regard to external transceiver temperature measurement, datasheets typically specify temperature requirements in terms of module case. As it relates to reliability prediction, the most crucial temperature point to monitor inside the transceiver is the laser junction. On DMI transceivers, (unless correlated) temperature diagnostic monitor readings will typically be hotter than the module case temperature and cooler than the actual laser junction temperature. To measure the true temperature read-back accuracy (±3° C per MSA) the transceiver temperature monitor readings should be compared with physical measurements at the actual temperature sensor location. Transceiver temperature read-back may be empirically correlated to external case in individual environments.

Transceiver supply voltage

The transceiver voltage diagnostic read-back allows monitoring of the transceiver supply voltage. The measurement point for transceiver voltage monitor is left undefined by SFF-8472 DMI MSA. The transceiver vendor will typically specify which supply (VccT or VccR) is monitored, and the location of the voltage measurement point on the transceiver. The transceiver voltage read-back will tend to run slightly lower than host supply due possibly to connector series resistance or transient suppression circuitry series resistance. Transceiver voltage monitor is meant to be DC detector only (cannot assess power supply noise.)

Laser bias current
The laser bias current readings generated by diagnostic monitor are commonly measured by mirroring bias current off of the laser driver circuit. Variations in laser bias current are expected under normal operation; a closed loop feedback circuit is typically implemented on fiber-optic transceivers, which adjust bias current to maintain constant laser output optical power. Laser bias varies for normal changes over temperature such as slope efficiency, forward voltage, or threshold variations. The laser bias diagnostic monitor has limited usefulness in assessing environmental compliance; its most valuable use is for fault or failure prediction applications.

Transmit Average Optical Power
The TX average power read-back allows monitoring of the transceiver's launched optical power. The TX average power diagnostic monitor is not a true "coupled power" optical measurement. Mirroring the monitor photocurrent in laser feedback circuit is the approach typically implemented to generate transceiver level TX average power measurements. Significant variations in average optical power are not expected due to the closed-loop control of TX optical power. The main use of the TX power monitor is allowing the host to ensure that TX power meets minimum compliance requirements.

Received optical modulation amplitude (OMA) or Average Optical Power (μW)
The DMI MSA allows for both average and OMA types of RX power measurement for the RX diagnostic monitor. RX OMA measurements are ideal for Fibre Channel standard applications, which define required receiver sensitivity in terms of OMA. Traditional Sonet customers and Ethernet customers, though, specify RX and TX power requirements in terms of average; hence, RX average power measurement type might be preferred in those applications. Please contact Avago for information on available DMI transceivers and respective RX power measurement type. OMA represents peak-to-peak power; hence, a modulated optical input signal is required for an OMA power sensor to generate meaningful measurements. It is generally difficult to measure RX OMA with equipment in the field; for that reason, DMI transceivers with RX OMA sensing offer a good measurement tool to the user.

Average represents DC power, so it does not require a modulated signal to be measured. The following equations state the basic definitions for the optical power figures of merit (see Figure 6 for illustration of parameters):

OMA = Power High – Power Low

ER (linear extinction ratio) = Power High ÷ Power Low

Average = (Power High + Power Low) ÷ 2

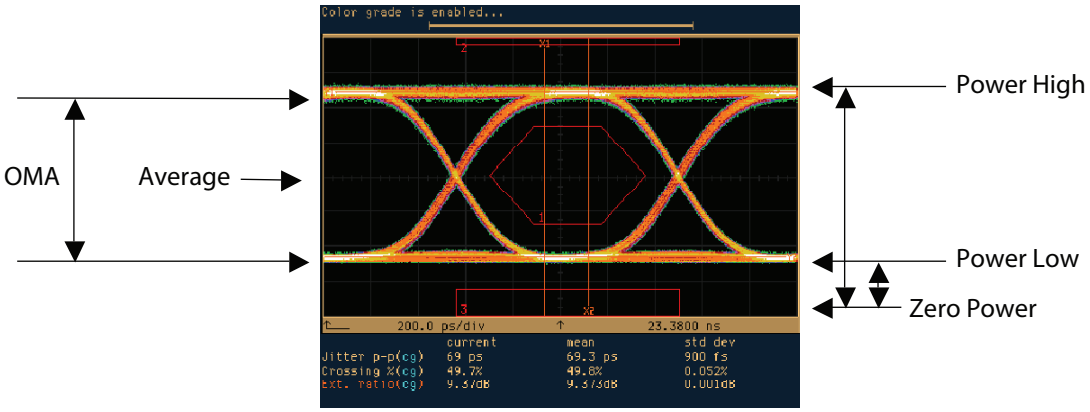

Figure 6. Eye diagram illustrationg optical figures of merit: average power, OMA, power high, power low and zero level power.

The average power value of the optical data signal output of a transmitter source can still be calculated from a receiver optical modulation amplitude (OMA) type measurement. The relationship between average power and OMA power is expressed in the equation below:

P_{ave} (dBm) = 10 * log {0.5*OMA*[(ER+1)/(ER-1)]},

where OMA is in units of mW, and extinction ratio (ER) is in linear scale unit.

If information about the average value of the incoming optical signal to the receiver is desired by the system user, but the DMI transceiver used implements an RX OMA type measurement, the calculation shown above can be used to obtain the average power value. There is inherently an accuracy penalty involved when calculating average power from a received OMA power, since the ER of the remote incoming signal is not known to the transceiver. By making an assumption on transmitter ER, nevertheless, the accuracy penalty due to calculation can be limited to only 1 dB (see Figure 7), making it very feasible to meet the MSA required ±3 dB accuracy for the RX power diagnostic monitor. Please contact Avago for more information about the implementation of RX average power read-back calculated from an OMA measurement on DMI transceivers.

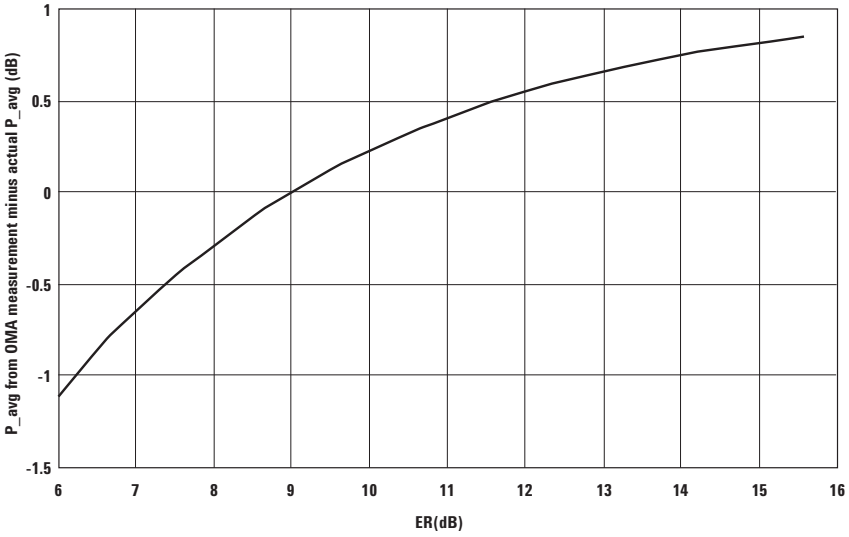

Figure 7. Plot of the data between true power and average power calculated from OMA power (assuming ER=9 dB) as a function of true ER.

Use of DMI for Fault isolation

The basic principle behind DMI based fault isolation is to use a combination of DMI status flags, transceiver hard pins and diagnostic parametric monitor data to pinpoint the specific location and cause of a link failure. Figure 8 shows a basic block diagram of the physical layer hardware in a DMI network system.

As illustrated in Figure 8, the physical layer hardware can be broken down into six sections that are potential fault sources (numbering below corresponds to figure):

1) Cable Plant
2) Local TX
3) Remote TX
4) Local RX
5) Host IC, PCB
6) Pluggable connector

With DMI fault isolation, the goal is to attempt to map specific combinations of transceiver digital diagnostic read-back flags and hard status flags to a particular location in the fiber-optic networking system. Table 8 illustrates how to map the DMI transceiver's status flags to the six system locations listed numerically above.

In Table 8, the columns labeled "local device digital diagnostic read-back flags" correspond to the alarm and warning flags located in 0xA2 bytes 112-119. The transceiver hardware flags LOS and TX_Fault are also included in the table. In addition to the alarm and warning flags and the hardware flags, the digital read-backs themselves can help in fault isolation by indicating the magnitude of the monitored parameters.

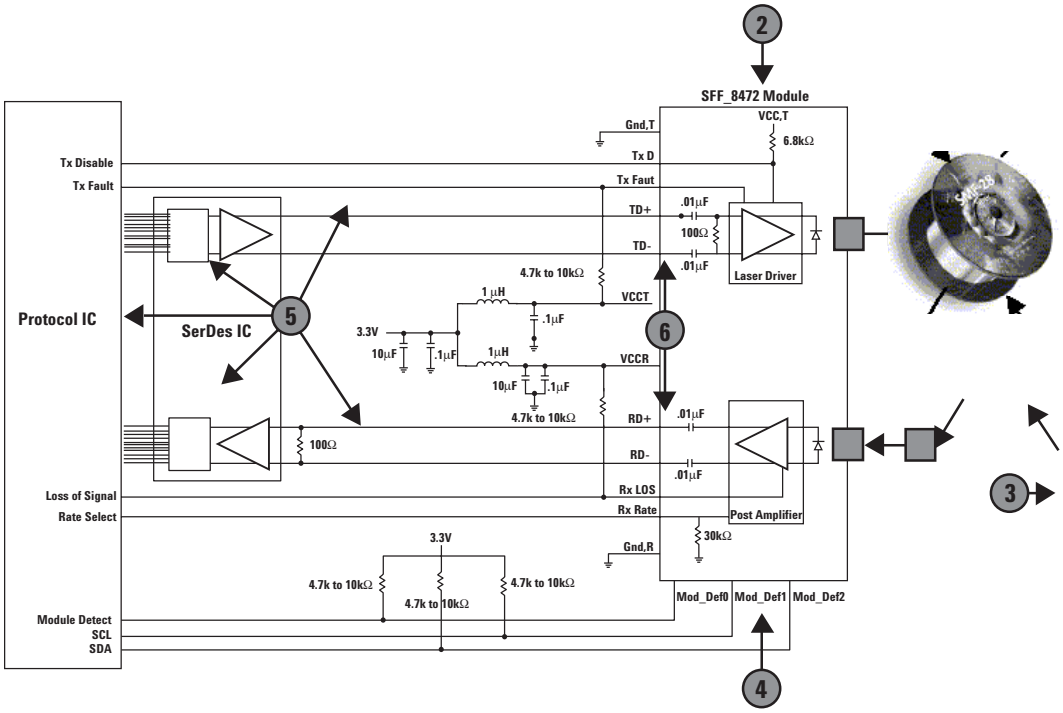

Figure 8. Generic block diagram of physical layer in a fiber-optic network system.

Table 8. Breakdown of applicable transceiver status flags (software and hardware) applied to fault isolation.

	Local Device Digital Diagnostic Read-back Flags				Local Device Status Flags		
Location/Type of Problem	**Vcc**	**Temperature**	**Rx OMA**	**Tx Power**	**Laser Bias**	**LOS**	**Tx_Fault**
Cable Plant Fault (Connectors, Fiber)	n/a	n/a	X	n/a	n/a	X	n/a
Local Transmitter Fault (Laser)	x	x	n/a	X	X	n/a	x
Remote Transmitter Fault (Laser)	n/a	n/a	X	n/a	n/a	x	n/a
Local Receiver Fault (Various)	x	x	x	n/a	n/a	x	n/a
Host IC, PCB, Filter Circuit, etc	x	n/a	n/a	x	x	n/a	x
Pluggable Connector (SFP)	x	n/a	n/a	n/a	n/a	n/a	n/a

Note: n/a Not Application X Alarm/Warming Indication x Possible Alarm/Warning Indicated

Mapping of flags to system locations
Potential Source – #1 Cable Plant:
Passive losses related to cable plant such as fiber attenuation, connector losses, or insertion losses can lead to fault. Local receiver flag Rx_LOS helps in indicating if there is sufficient light received to operate, while the local received power diagnostic monitor indicates the magnitude of the received power.

Potential Sources – #2 Local Transmitter:
Local laser flags (Tx_Fault and Tx_Disable) help in indicating whether the laser been disabled intentionally or due to fault? Local laser functionality (Tx power and laser bias diagnostic monitors) outline whether the laser is within valid operational limits. Local laser environment (Temperature, Vcc) points to whether the local environment is within acceptable transceiver limits or at conditions likely to lead to device failure.

Potential Sources – #3 Remote Transmitter (similar to cable plant):
Local receiver flag RX LOS indicates if asserted if there is insufficient light received to operate. Local received power diagnostic monitor supplies information about the magnitude of received power. IF the RX power monitor is of OMA type, it provides the system user information on whether there is modulation on the received power or if the modulation has drifted.

Potential Sources – #4 Local Receiver (similar to remote transmitter)
Local receiver flag RX LOS indicates if asserted if there is insufficient light received to operate. Local received power diagnostic monitor supplies information about the magnitude of received power. IF the RX power monitor is of OMA type, it provides the system user information on whether there is modulation on the received power or if the modulation has drifted. The Local receiver environment (Temperature, Vcc) points to whether the local environment is within acceptable transceiver limits or at conditions likely to lead to device failure.

Potential Sources – #5 Host ICs, PCB, Filter Circuit, etc:
There is no way to detect whether there is modulated electrical data into the transceiver or not (TX power monitor and laser bias monitor are both DC level indicators.) To gauge whether or not there is electrical data out of the transceiver external host SerDes LOS indicator should be used. The transceiver's Vcc diagnostic monitor can be used to assess whether supply voltage for transceiver is at acceptable level.

Potential Sources – #6 Pluggable Electrical Connector (SFP)
Transceiver pins Mod_Def0 (internally pulled low) and Tx_Disable (internally pulled high) can be used to gauge whether an SFP is properly sitting in the puggable connector. Transceiver Vcc diagnostic monitor can be monitored to check whether there is voltage drop due to the connection being resistive.

Use of DMI for failure preemption and/or prediction

The DMI feature sets can be used to help in device failure prediction on fiber-optic networking systems. Failure prediction in a DMI environment relates to the ability to anticipate a link failure based on transceiver parametric performance. There are two basic types of failure conditions that can be seen on fiber-optic transceivers:

- Device faults – A device non-operation or malfunction. Typically applies more to transmitter performance, due to nature of semiconductor lasers.
- High error rate conditions – Operating conditions are such that transceiver is operating at its signal-to-noise limit. Applies more to fiber-optic receiver performance.

Failure (Device Fault) Prediction – Local Transmitter Laser
Laser failure prediction via DMI feature sets is not yet a fully mature application. Laser lifetime prediction based on DMI measurements does not yet result in precise time-to-failure conclusions. Many factors need to be considered in laser reliability predictions such as current density, junction temperature, fabrication and structure. A practical approach for pre-empting of potential laser faults is setting of operational limits on measurable laser bias drift. Laser parametric changes (quantum efficiency, threshold or slope efficiency) seen through die level measurements can be evaluated during reliability qualification.

Figure 9 shows an example of accelerated stress data on 850 nm VCSEL devices in TO-46 package. The devices plotted in the figure were stressed using T = 125° C, and 25 mA bias. The endpoint condition used to generate data in Figure 9 was temperature of 25° C. In addition, laser bias was implemented so as to maintain 2 mW constant output power. From the data, an upper limit (failure limit) can be chosen for operational laser bias current; devices exceeding chosen bias limit in regular operation are considered failures. Note that in its typical use condition, SFP temperature is around 40° C and SFP laser bias current is around 5 mA.

Laser bias is observed in a constant optical power loop in fiber-optic transceiver applications. As part of failure prediction process, system user can monitor for consistent increases in laser bias current, reflected in diagnostic monitor readings. When monitoring laser bias current, constant temperature and Vcc are needed to resolve actual device degradation from normal changes in laser operating conditions. Baseline measurements should be taken over all temperature and Vcc and stored (either at transceiver level or system software level) to isolate bias current drifts due to device degradation. Subsequent DMI measurements can then be compared at current transceiver temperature and Vcc. Time-to-failure based on DMI drifts may possibly resolve months to years. If finer granularity on transceiver degradation or failure prediction is required, contact Avago for guidance and limitations on particular products.

The TX optical output power diagnostic monitor can also be used to assist user in failure prediction, though it is not as effective as bias current monitor, specifically in providing margin in terms of time-to-failure. Significant variations in average optical power are not expected, due to transceiver's closed loop control of optical power. Hence, if significant drifting is observed (i.e. greater than ±3 dB) it is very likely an indication of an impending TX fault: either laser closed-loop control has been lost or extreme laser bias conditions might be present.

Failure (Device Fault) Prediction – Remote Transmitter Laser
Degradation in a remote laser may be observable using a RX_OMA diagnostic monitor. Most transceivers maintain constant average transmit power. It is more challenging for transceivers, nevertheless, to maintain constant transmit laser modulation (OMA or ER.) As a remote laser degrades, its OMA (and ER) will also degrade. An RX OMA sensor can resolve variations in remote transmitter peak-peak swing, while remote OMA drift will be masked by an RX average input power detector.

Figure 10 illustrates typical laser optical power versus bias current curves. There are two curves in the plot: one corresponds to beginning of life (0 hr) and the other corresponds to laser characteristic after extended operation (N hr.) Slope efficiency degrades as laser ages due to extended use (more bias current needed to output a given average optical power.) Via closed-loop control, constant power is maintained. However, if modulation is not adjusted as laser slope efficiency degrades, OMA (or peak-peak) power can decrease substantially (see figure.) An RX OMA diagnostic monitor and not an average power one will detect such potential modulation drift.

Failure (Device Fault) Prediction – Other Operational Faults

- Supply Voltage – CMOS breakdown voltage is approximately 4 V. Transceiver de-biasing (non-operation) typically happens below 2.8 V.
- Rx Power – Transceivers may saturate or overload with excessive received optical power, leading to high bit error rates.
- Temperature – High temperatures may accelerate component degradation.

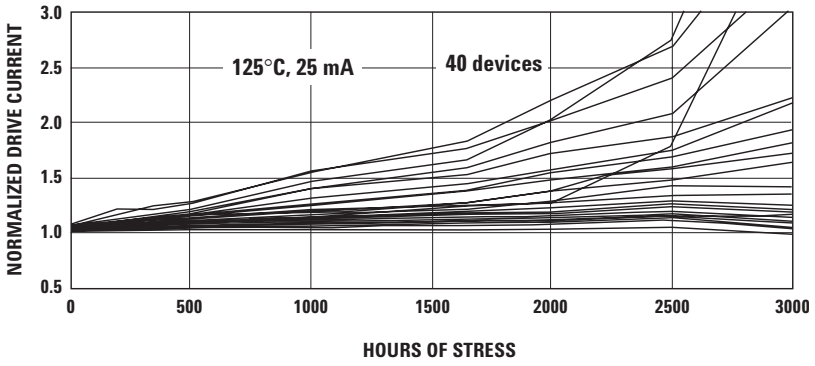

Figure 9. 850 nm VCSEL TO-46 accelerated stress data; endpoint measured for T=25° C and laser bias current needed to obtain 2 mW optical power output.

Implementation of Alarms and Warnings and customer writeable EEPROM bytes

Example scheme for selecting alarm and warning threshold limits

The present section describes an algorithm for choosing the alarm and warning thresholds for each of the diagnostic read-backs. The proposed warning thresholds for each of the five read-backs are meant to designate operating ranges outside of which the transceiver, per specification, might drift from required network standard compliance (i.e. Fibre Channel, Gigabit Ethernet, etc.) The proposed alarm thresholds are intended to demarcate parametric conditions where the transceiver is likely to fault, and/or device reliability is seriously at risk.

Supply Voltage

- The low and high warning thresholds for the supply voltage read-back correspond to the minimum and maximum supply voltage limits, per the transceiver's recommended operating range listed on its datasheet.
- The low and high alarm thresholds for supply voltage read-back correspond to numbers approaching the minimum and maximum supply voltage limits per the transceiver's absolute maximum ratings. At the low end, the transceiver IC's run out of headroom for proper functionality. The high-end alarm threshold is a voltage approaching the IC breakdown level.

Transceiver temperature

- The low and high warning thresholds for the transceiver temperature read-back are determined by the minimum and maximum values of the transceiver's recommended operating range, as listed on its datasheet.
- The low and high alarm thresholds for the transceiver temperature read-back correspond to the minimum and maximum temperature limits per the transceiver's absolute maximum ratings, as listed on its datasheet. Transceiver reliability is not guaranteed beyond the maximum rating temperature range.

Transmitter average light output power (TX average LOP)

- The low end warning threshold for TX LOP corresponds to the minimum transmitter average power specified by the standard (FC or GbE); this minimum power generally corresponds to the minimum TX power allowed by the link power budget.
- The low end alarm threshold for TX LOP corresponds to the minimum TX LOP (value used for the low warning threshold) MINUS 3 dB. A standard fiber optic receiver will typically have, over temperature and voltage, an optical sensitivity that offers at least 3 dB of margin to the minimum RX input power specified by the applicable networking standard. The minimum TX power per standard, in theory, is the minimum power needed to guarantee delivering the minimum RX input power (per standard) at worst case link conditions (max link length, high dispersion.) If the TX output power, however, falls 3 dB below the min TX LOP, margin to the minimum RX input power cannot be insured for the allowable worst case link, and therefore, proper link error rate cannot be maintained over all conditions required by standard.

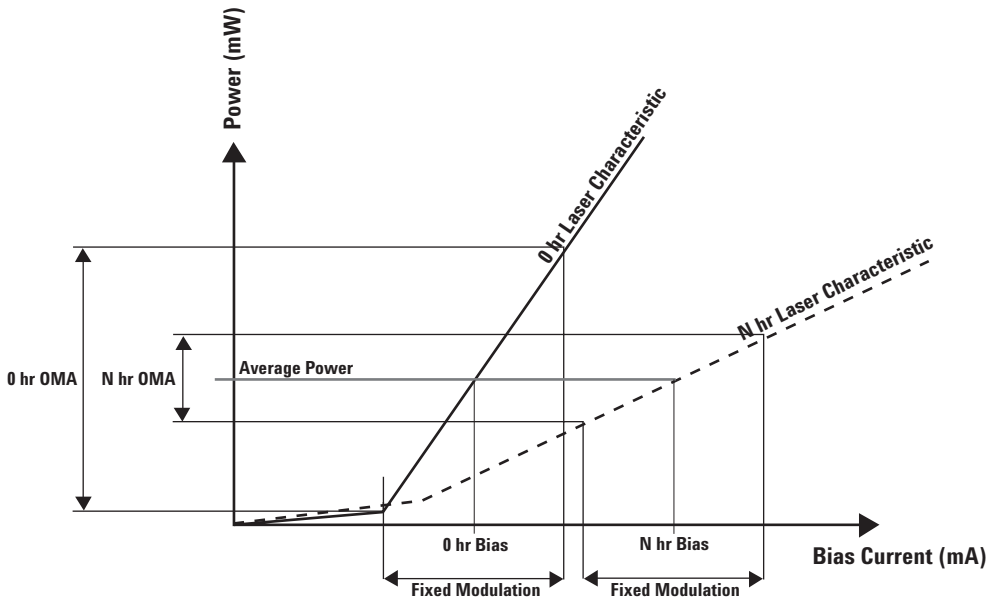

Figure 10. Typical laser optical power versus bias current characteristic, illustrating case where modulation is not compensated after laser aging.

- The high end alarm corresponds to a TX LOP approaching the limit set forth by eye safety standards (Class 1 eye safety limit).
- The high end warning is not needed, unless the customer or application dictates the need for a TX LOP upper limit that is lower than the eye safety limit.

Receiver optical modulation amplitude (OMA) power

- The low end warning threshold for RX OMA corresponds to the minimum OMA required by the network standard or application
- The high end warning threshold for RX OMA shall be either the eye safety limit, the RX overload power specified by standard, or the maximum TX LOP specified by customer or application (whichever of the three is lower), translated into units of OMA.
- The low alarm threshold shall not be used; the loss-of-signal (LOS) digital output signal covers the necessary low RX input power alarm functionality for the transceiver. Because of A/D noise, the signal-to-noise performance of the RX OMA read-back, although meeting the required accuracy per DMI MSA, will not be as robust as the LOS signal for very low input powers. Therefore, LOS and RX OMA read-back would not coincide in a given application.
- The high end alarm threshold for RX OMA shall not be used. The power needed to actually saturate a standard Avago receiver and have an inoperable link, is much greater than both Class 1 eye safety limits and RX overload limits, specified by network standards (Fibre Channel and Gigabit Ethernet.)

Transmitter bias current

- The high end warning threshold for the TX bias current read-back, as well as the low and high alarm thresholds shall be set by Avago based on realistic laser bias range, and will take into consideration factors such as reliability, and expected drifts over life and operating conditions.

Use of Customer Writable EEPROM bytes (page 0xA2, bytes 128-247)

120 total bytes of non-volatile memory are available to the system user (located on DMI transceiver address 0xA2 bytes 128-247) per SFF-8472 MSA definition for storing of information. Part number information, and parametric beginning of life data are examples of useful transceiver data that could be stored in the customer writable space. These customer writable bytes can be pre-loaded at the factory by the vendor based on customer requirements. The bytes could also possibly be used as operational system memory.

References

[1] SFF-8472 "Digital Diagnostic Monitoring Interface for Optical Transceivers" Multi-source Agreement, Revision 9.3; http://www.sffcommittee.org

[2] Small-Form Factor Pluggable (SFP) Multi-source Agreement INF-8074

[3] Atmel AT24C02A/04A/08A Two-wire Serial EEPROM Family Specification

[4] Philips I2C bus Specification

[5] Philips PCF8584 I2C Controller Datasheet

[6] Xilinx IC Bus Interface Design Specification

Table 9. Alarm and warning threshold limits for the Avago HFBR-57L5AP 1xGbE and 1xFC multi-mode transceiver, implementing the proposed limit criteria.

Digital read-back	Warning limits		Alarm limits	
	Low	High	Low	High
Transceiver Voltage, V	2.97	3.63	2.7	3.9
Transceiver Temperature, ° C	-10	85	-40	100
TX Average Power, dBm (Class 1 Eye safe)	-10	-4	-13	-1.5
RX OMA power, mW (peak-to-peak)	31 μW	1.1[1]	0	6.55
TX laser bias current, mA	2	8.5	2	10

Note:

1. -1.5 dBm average for ER = 9 dB

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