

Integrated Power Management Solutions

ADI Announces a New Family of Multichannel Regulators

Multichannel Regulator (μ PMUs) Benefits

- Easy to Use
- Minimize PCB Area
- Reduced BOM Cost



Adjustable Output Voltages

3 MHz Switching Frequency for
Ultrasmall External Components

LFCSP (QFN) Package Options

Tiny WLCSP Package Options

Minimal External Components

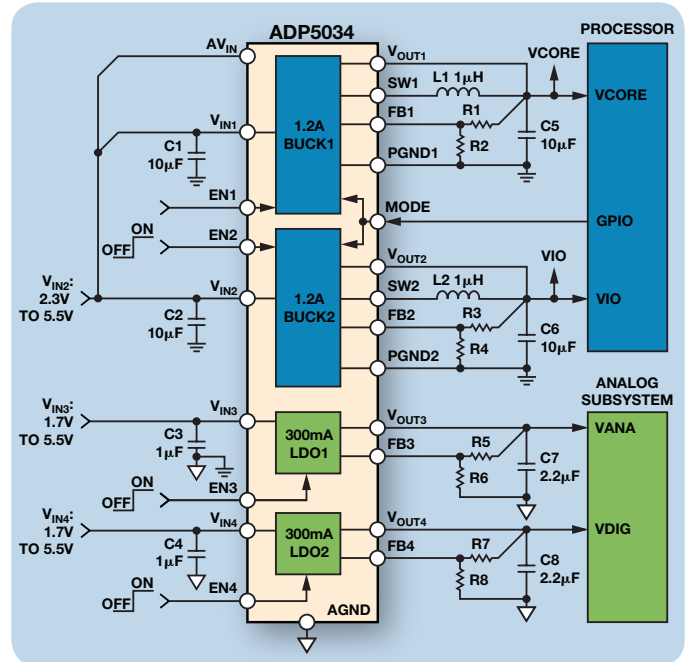
Small Solution Size

ADP5034

Dual, 3 MHz, 1.2 A Buck Regulator with Two 300 mA LDOs in LFCSP

Key Features

- Input voltage range: 2.3 V to 5.5 V
- Two 1.2 A buck regulators
- Two 300 mA LDOs
- Initial regulator accuracy: $\pm 1\%$
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Factory-programmable or external adjustable V_{OUTx}
- Buck1 and Buck2 key specifications
 - Stable with 1 μF ceramic output capacitors
 - High PSRR: 65 dB PSRR 1 kHz to 10 kHz
 - Low output noise: 80 μV rms typical output noise at $V_{OUT3} = 2.5 \text{ V}$
 - Low dropout voltage: 150 mV @ 300 mA load
 - Low input supply voltage from 1.7 V to 5.5 V
- -40°C to $+125^\circ\text{C}$ junction temperature
- ADP5034: 24-lead, 4 mm \times 4 mm LFCSP package
- ADP5033: 16-lead WLCSP



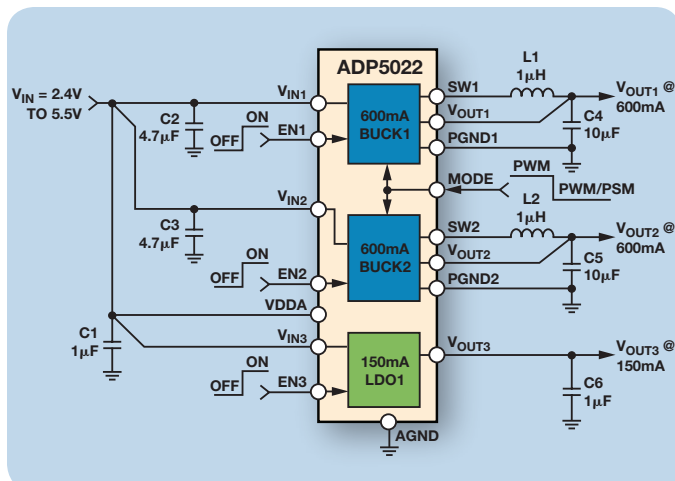
ADP5034 functional block diagram.

ADP5022

Industry's Smallest Dual Buck Regulator Reduces Component Count and Board Space in Portable Systems

Key Features

- Input voltage range: 2.4 V to 5.5 V
- Tiny 16-ball, 2 mm \times 2 mm WLCSP package
- Soft start
- Factory-programmable UVLO on VDDA system supply of either 2.2 V or 3.9 V
- Factory-programmable default output voltages for all 3 channels
- Total BOM size: 4.7 mm \times 5 mm



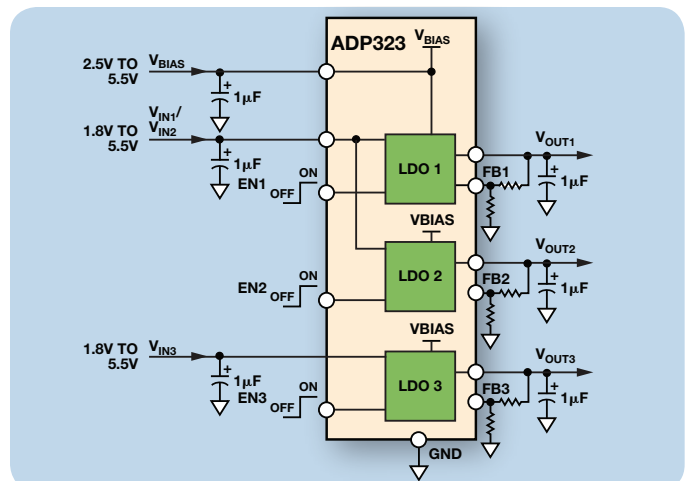
ADP5022 functional block diagram.

ADP323

Triple, 200 mA, Low Noise, High PSRR Voltage Regulator

Key Features

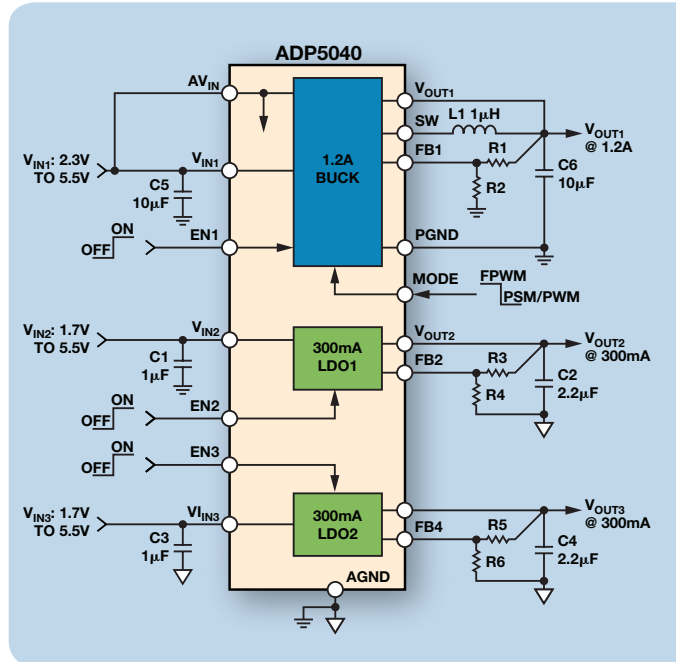
- Bias voltage range (V_{BIAS}): 2.5 V to 5.5 V
- LDO input voltage range ($V_{IN1}/V_{IN2}, V_{IN3}$): 1.8 V to 5.5 V
- Three 200 mA low dropout voltage regulators
- Adjustable output voltages, fixed-output voltages (ADP322)
- 16-lead, 3 mm \times 3 mm LFCSP
- 3 independent logic controlled enables
- High PSRR, 60 dB PSRR, 10 kHz
- Low output noise, 29 μV rms typical at $V_{OUT} = 1.2 \text{ V}$



ADP323 functional block diagram.

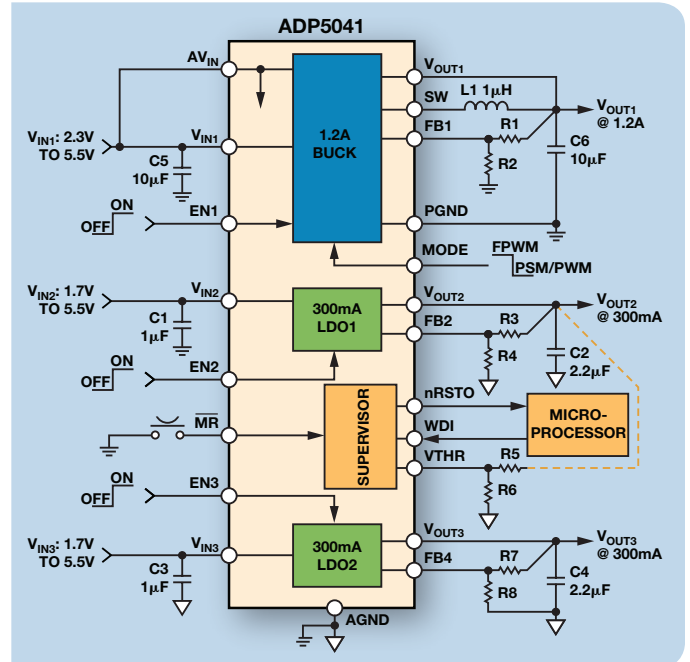
ADP5040 and ADP5041

ADP5040: 1.2 A Buck and Dual 300 mA LDO with Individual Enables in LFCSP



ADP5040 functional block diagram.

ADP5041: 1.2 A Buck and Dual 300 mA LDO, Supervisory, Watchdog, and Manual Reset in LFCSP

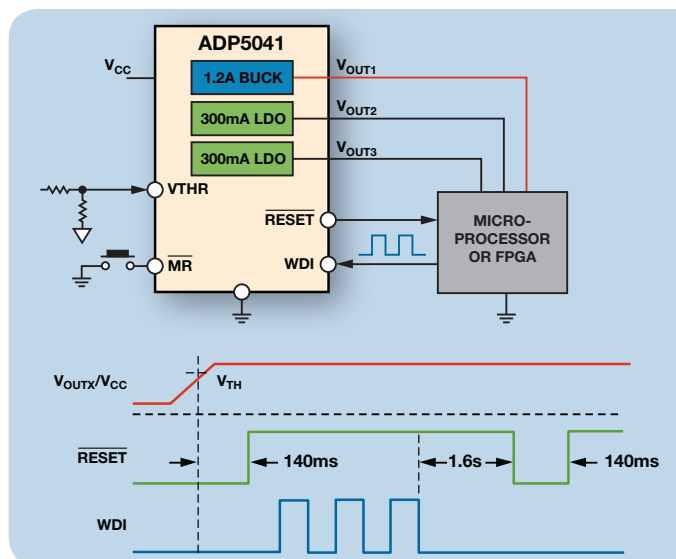


ADP5041 functional block diagram.

Key Features

- Input voltage range: 2.3 V to 5.5 V
- One 1.2 A buck regulator, fixed and adjustable output voltages, up to 96% efficiency
- Two 300 mA LDOs, fixed and adjustable outputs
- 20-lead, 4 mm × 4 mm LFCSP package
- Initial regulator accuracy: ±1%
- Overcurrent and thermal protection
- Soft start
- Undervoltage lockout
- Open-drain processor reset with external adjustable threshold monitoring
- ±1.5% threshold accuracy over the full temperature range
- Guaranteed reset output valid to $V_{CC} = 1 V$
- Manual reset input
- Watchdog refresh input
- 2 reset timeout options: 20 ms and 140 ms (minimum)
- 2 watchdog timeout options: 102 ms and 1600 ms (typical)

ADP5041 Delivers Improved System Reliability by Integrating Power-On Reset and Watchdog Functionality



±1.5% trip threshold accuracy to monitor low voltage core rails.

Multichannel Regulators Applications

- Portable medical devices
- Energy metering power supplies
- Single Li-Ion/Li-polymer battery-powered equipment
- PDAs, portable media players, portable instruments
- DSP, micro, and memory power supplies
- FPGA power supplies

Part Number	Product Description	V _{in} (V)	V _{out} (V)	Number of Outputs	Output Current (mA)	IC	Reset Trip Threshold (V)	Min Reset Timeout (ms)	Typ Watchdog Timeout (ms)	Key Features	Package	Price (\$U.S.)
ADP220/ADP221	Dual, 200 mA LDO	2.5 to 5.5	LD01: 1.1, 1.8, 2.6, 2.75, 2.8, 3.0, 3.3 LD02: 1.2, 1.8, 2.3, 2.7, 2.75, 2.8, 3.0	2 × LDO	300	—	—	—	—	40 dB PSRR at 1 MHz	6-lead WLCSOP	0.58
ADP222/ADP223	Dual, 300 mA LDO	2.5 to 5.5	LD01: 3.3, 2.8, 1.8, 1.5, 1.2; LD02: 3.0, 2.8, 2.7, 2.5, 1.8, 1.5V and adj (0.5 to 5)	2 × LDO	300	—	—	—	—	Noise 29 μ V rms, 40 dB PSRR at 1 MHz	8-lead LFCSP	0.49
ADP224/ADP225	Dual, 300 mA LDO	2.5 to 5.5	LD01: 2.8; LD02: 1.8 adj (0.5 to 5)	2 × LDO	300	—	—	—	—	Quick output discharge	8-lead LFCSP	0.49
ADP320	Triple, 200 mA LDO	1.8 to 5.5	LD01: 3.3; LD02: 1.8, 3.3; LD03: 1.5	3 × LDO	200	—	—	—	—	Fixed V _{out} options	16-lead LFCSP	0.54
ADP322	Triple, 200 mA LDO	1.8 to 5.5	LD01: 3.3, 2.8, 2.5; LD02: 2.8, 2.5, 1.8; LD03: 1.8, 1.5, 1.2	3 × LDO	200	—	—	—	—	Fixed V _{out} options	16-lead LFCSP	0.54
ADP323	Triple, 200 mA LDO	1.8 to 5.5	Adj (0.5 to 5)	3 × LDO	200	—	—	—	—	Adjustable V _{out} options	16-lead LFCSP	0.54
ADP2114	Dual buck regulator	2.7 to 5.5	0.8, 1.2, 1.5, 1.8, 2.5, 3.3 and adj	2 × buck	2000	—	—	—	—	SYNC pin, PGOOD pins	32-lead LFCSP	2.50
ADP2116	Dual buck regulator	2.7 to 5.5	0.8, 1.2, 1.5, 1.8, 2.5, 3.3 and adj	2 × buck	3000	—	—	—	—	SYNC Pin, PGOOD Pins	32-lead LFCSP	3.17
ADP2140	600 mA buck and 300 mA LDO	Bucks: 2.3 to 5.5 LDO: 1.65 to 5.5	Buck: 2.3, 2.5, 1.8, 1.5, 1.2; LDO: 3.3, 2.8, 2.5, 1.8, 1.5, 1.2	1 × buck 1 × LDO	600 300	—	—	—	—	Autosequencing, power good, power save mode	10-lead LFCSP	1.20
ADP5020	General-purpose PMU	Buck: 2.4 to 5.5	Buck1: 3.7, 3.3, 3.2, 2.9, 2.8, 2.5; Buck2: 1.8, 1.7, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1; LDO: 3.3, 3.2, 3.1, 3.0, 2.9, 2.8, 2.7, 2.6, 2.5, 2.4, 2.3, 2.2, 2.1, 2.0, 1.9, 1.8	2 × buck 1 × LDO	600, 300 150	Yes	—	—	—	IC, programmable outputs, supervisor, external sync	20-lead LFCSP	1.50
ADP5022	Dual, 3 MHz buck with 150 mA LDO	Buck: 2.3 to 5.5 LDO: 2.3 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8; LD0s: 3.3, 3.0, 2.9, 2.8, 2.7, 2.5, 2.0, 1.875, 1.8, 1.75, 1.7, 1.65, 1.6, 1.55, 1.5, 1.2	2 × buck 1 × LDO	600 150	—	—	—	—	Mode pin, individual enable pins	16-lead WLCSOP	1.80
ADP5023	Dual, 800 mA buck with 300 mA LDO	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	2 × buck 1 × LDO	800 300	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.59
ADP5024	Dual, 1.2 A buck with 300 mA LDO	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	2 × buck 1 × LDO	1200 300	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.79
ADP5030	Dual LDO with load switch	2.5 to 5.5	LD01: 1.2; LD02: 2.1.8	2 × LDO	200	—	—	—	—	Load switch and level shifters	16-lead WLCSOP	0.85
ADP5033	Dual, 3 MHz buck regulator with dual LDO	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8; LD0s: 3.3, 3.0, 2.9, 2.8, 2.7, 2.5, 2.0, 1.875, 1.8, 1.75, 1.7, 1.65, 1.6, 1.55, 1.5, 1.2	2 × buck 2 × LDO	800 300	—	—	—	—	Mode pin, two enable pins	16-lead LFCSP	1.90
ADP5034	Dual, 3 MHz buck regulator with dual LDO	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	2 × buck 2 × LDO	1200 300	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.99
ADP5037	Dual, 3 MHz, 800 mA buck regulator with dual 300 mA LDO	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	Bucks: 2.3 to 5.5 LDOs: 1.7 to 5.5	2 × buck 2 × LDO	800 300	—	—	—	—	Mode pin, individual enable pins	24-lead LFCSP	1.69
ADP5040	3 MHz buck regulator with dual LDO	Buck: 2.3 to 5.5 LDOs: 1.7 to 5.5	Buck: 2.3 to 5.5 LDOs: 1.7 to 5.5	1 × buck 2 × LDO	1200 300	—	—	—	—	Individual enable pins, mode pin	20-lead LFCSP	1.39
ADP5041	3 MHz buck regulator with dual LDO, supervisor, and watchdog timer	Buck: 2.3 to 5.5 LDOs: 1.7 to 5.5	Buck: 2.3 to 5.5 LDOs: 1.7 to 5.5	1 × buck 2 × LDO	1200 300	—	0.5 (adj)	20, 140	102, 1600	Individual enable pins and supervisor, WDI, mode pin and MR pin	20-lead LFCSP	1.79
ADP5042	3 MHz buck regulator with dual LDO, supervisor, and dual watchdog timers	Buck: 2.3 to 5.5 LDOs: 1.7 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8; LD0s: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1.0, 0.9, 0.8	1 × buck 2 × LDO	800 300	—	4.63, 3.08, 2.93, 2.63, 2.50, 2.35, 2.068, 1.692	20, 140	102, 1600	Individual enable pins and supervisor, WDI, WDI2, mode pin and MR pin	20-lead LFCSP	1.99
ADP5043	3 MHz buck regulator with LDO, supervisor, and dual watchdog timers	Buck: 2.3 to 5.5 LDO: 1.7 to 5.5	Buck: 3.3, 3.0, 2.8, 2.5, 2.3, 2.0, 1.82, 1.8, 1.6, 1.5, 1.4, 1.3, 1.2, 1.1, 1.0, 0.9, 0.8; LD0: 3.3, 3.0, 2.8, 2.5, 2.25, 2.0, 1.8, 1.7, 1.6, 1.5, 1.2, 1.1, 1.0, 0.9, 0.8	1 × buck 1 × LDO	800 300	—	4.63, 3.08, 2.93, 2.63, 2.50, 2.35, 2.068, 1.692	20, 140	102, 1600	Individual enable pins and supervisor, WDI, WDI2, mode pin and MR pin	20-lead LFCSP	1.79
ADP5045	Boost, buck-boost, triple buck, and dual LDO	2.5 to 5.5	Buck: 3.8 to 5.3 3.19 to 3.33 0.98 to 2.5, adj 1.5 to 3.5	1 × boost 1 × buck-boost 3 × buck 2 × LDO	1200 900 1800, 900 150, 50	Yes	—	—	—	Programmable power sequencing, soft start, output voltages and RTC; 25 mA LED driver	64-ball WLCSOP	4.99

IC refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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www.analog.com/power

Analog Devices, Inc.
Worldwide Headquarters
 Analog Devices, Inc.
 Three Technology Way
 P.O. Box 9106
 Norwood, MA 02062-9106
 U.S.A.
 Tel: 781.329.4700
 (800.262.5643,
 U.S.A. only)
 Fax: 781.461.3113

Analog Devices, Inc.
Europe Headquarters
 Analog Devices, Inc.
 Wilhelm-Wagenfeld-Str. 6
 80807 Munich
 Germany
 Tel: 49.89.76903.0
 Fax: 49.89.76903.157

Analog Devices, Inc.
Japan Headquarters
 Analog Devices, KK
 New Pier Takeshiba
 South Tower Building
 1-16-1 Kaigan, Minato-ku,
 Tokyo, 105-6891
 Japan
 Tel: 813.5402.8200
 Fax: 813.5402.1064

Analog Devices, Inc.
Southeast Asia Headquarters
 Analog Devices
 22/F One Corporate Avenue
 222 Hu Bin Road
 Shanghai, 200021
 China
 Tel: 86.21.2320.8000
 Fax: 86.21.2320.8222

