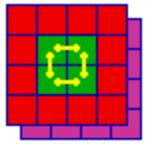
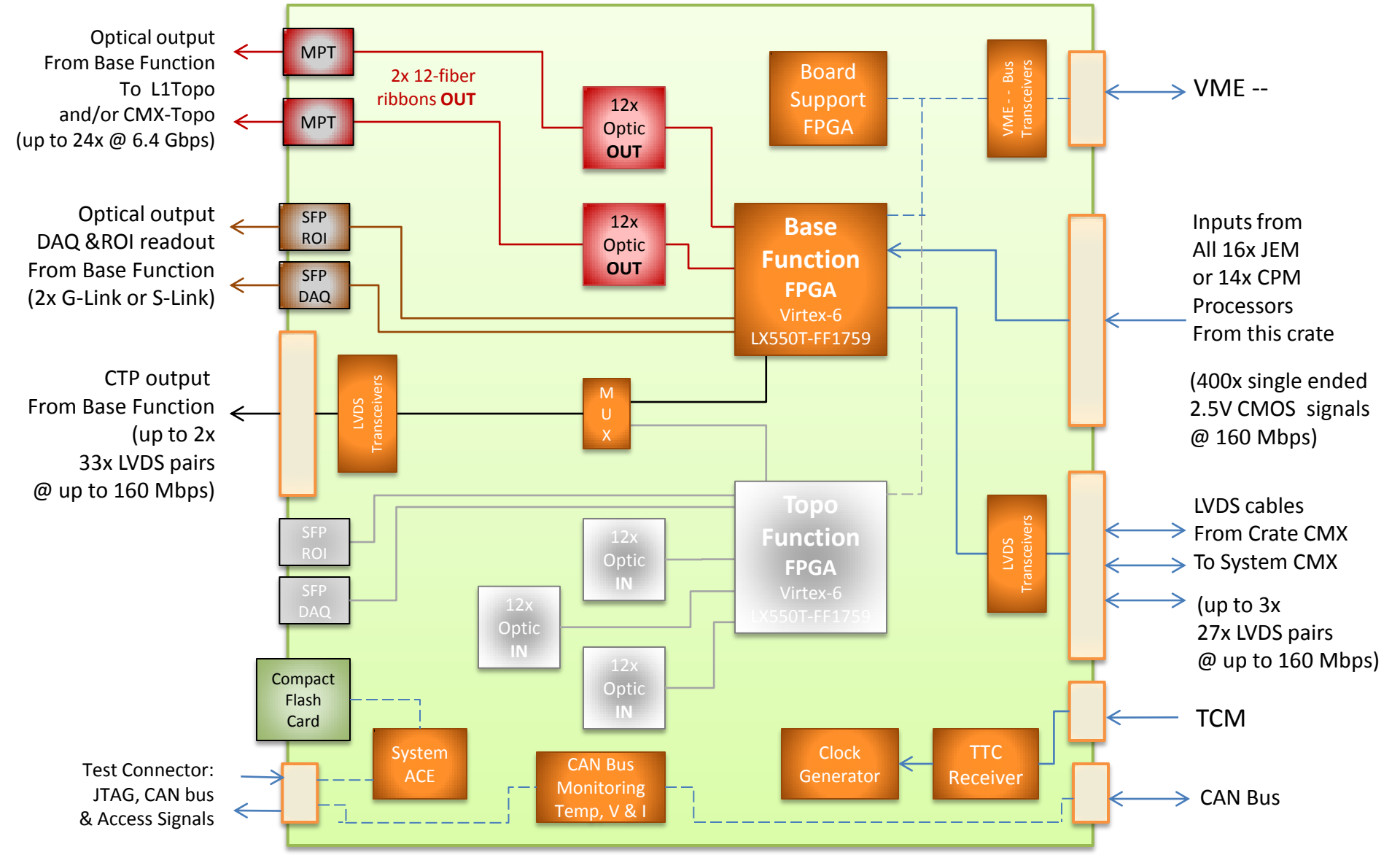


CMX

Collection file for current diagrams

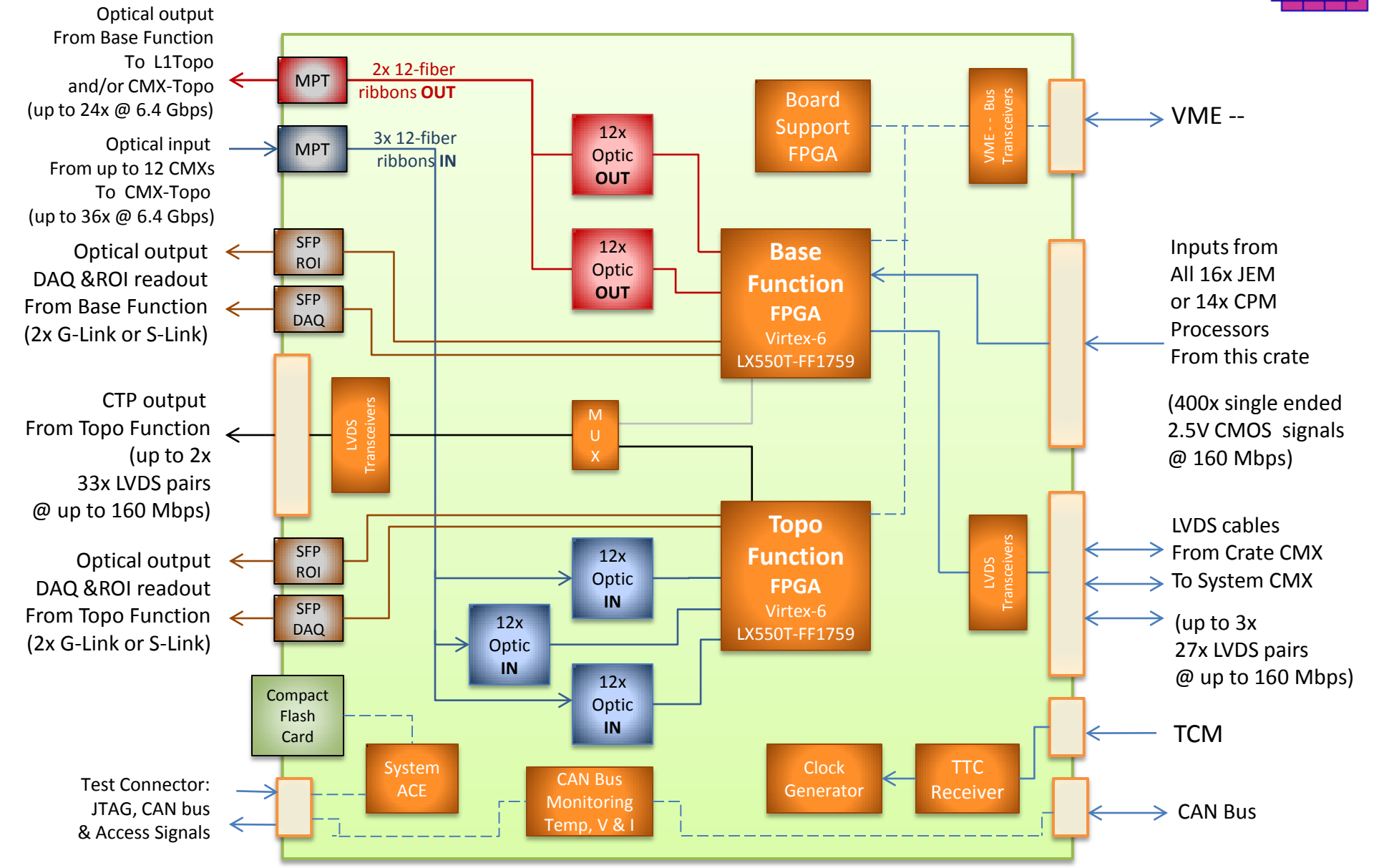
CMX Card with Base-CMX functionality only



MICHIGAN STATE UNIVERSITY

30-Apr-2014

CMX Card with Base-CMX functionality and TP-CMX capability



MICHIGAN STATE UNIVERSITY

30-Apr-2014

IO Banks available on Virtex6 LX550T

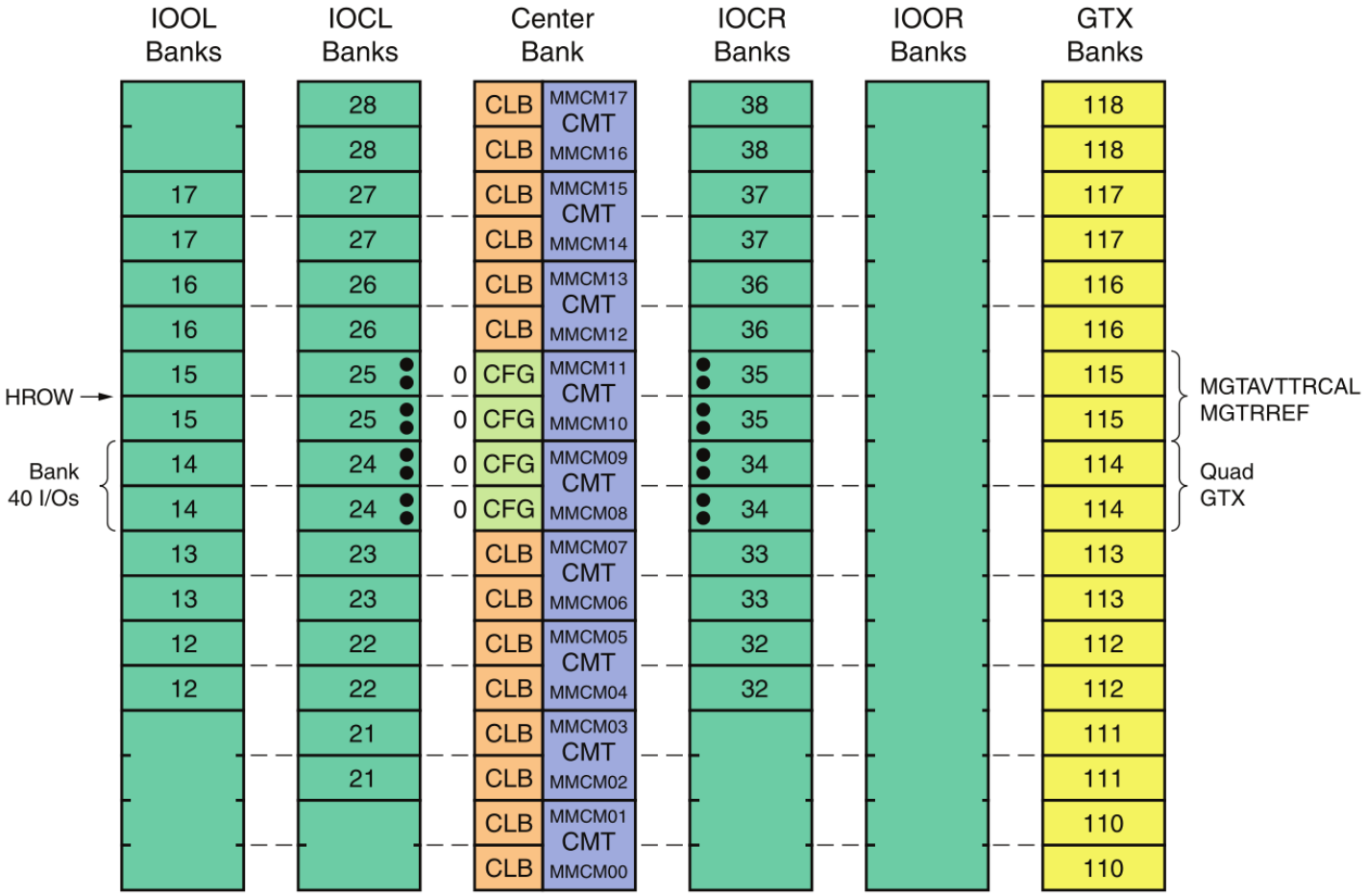
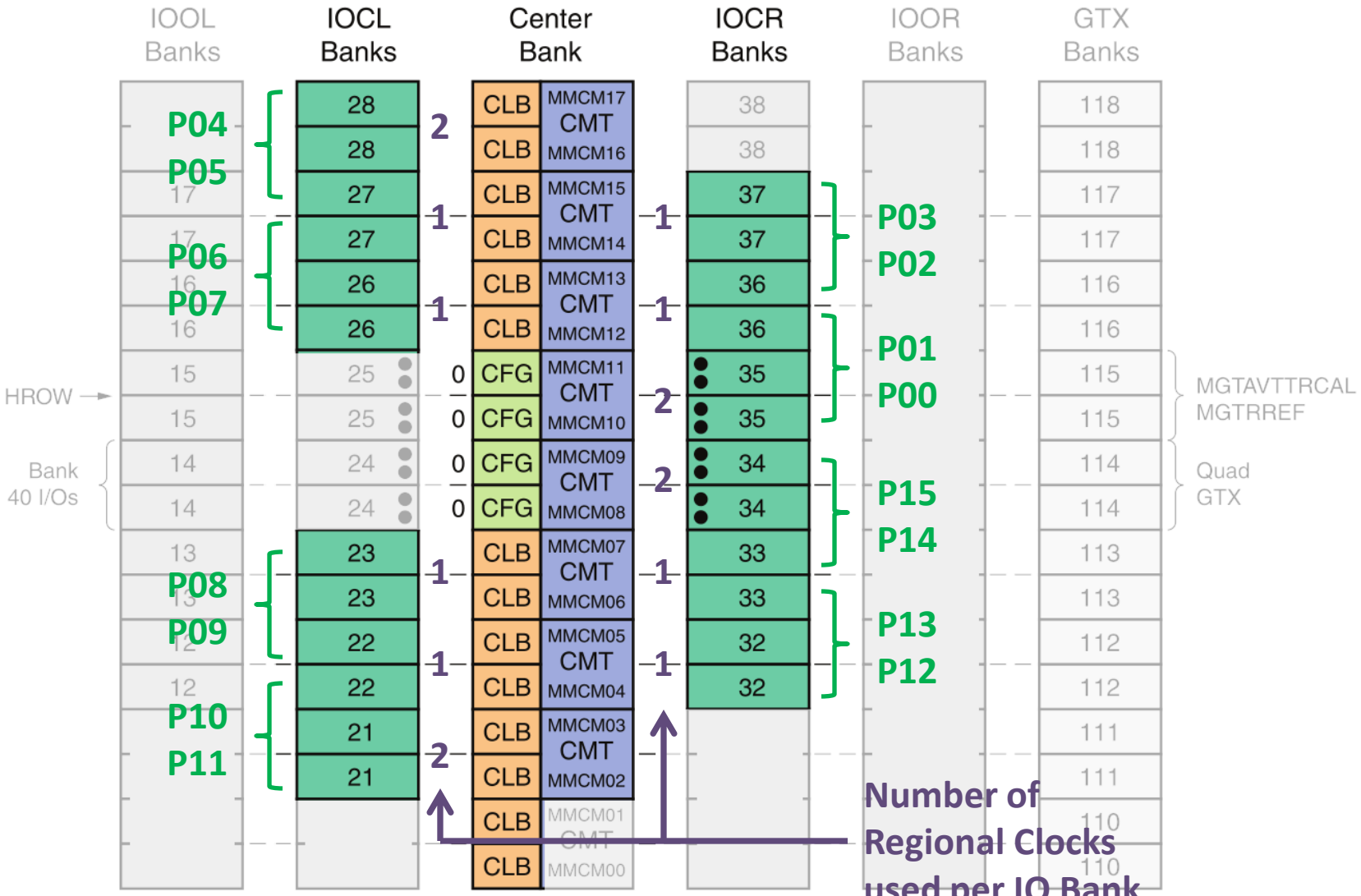


Figure 1-6: **XC6VLX550T Banks**

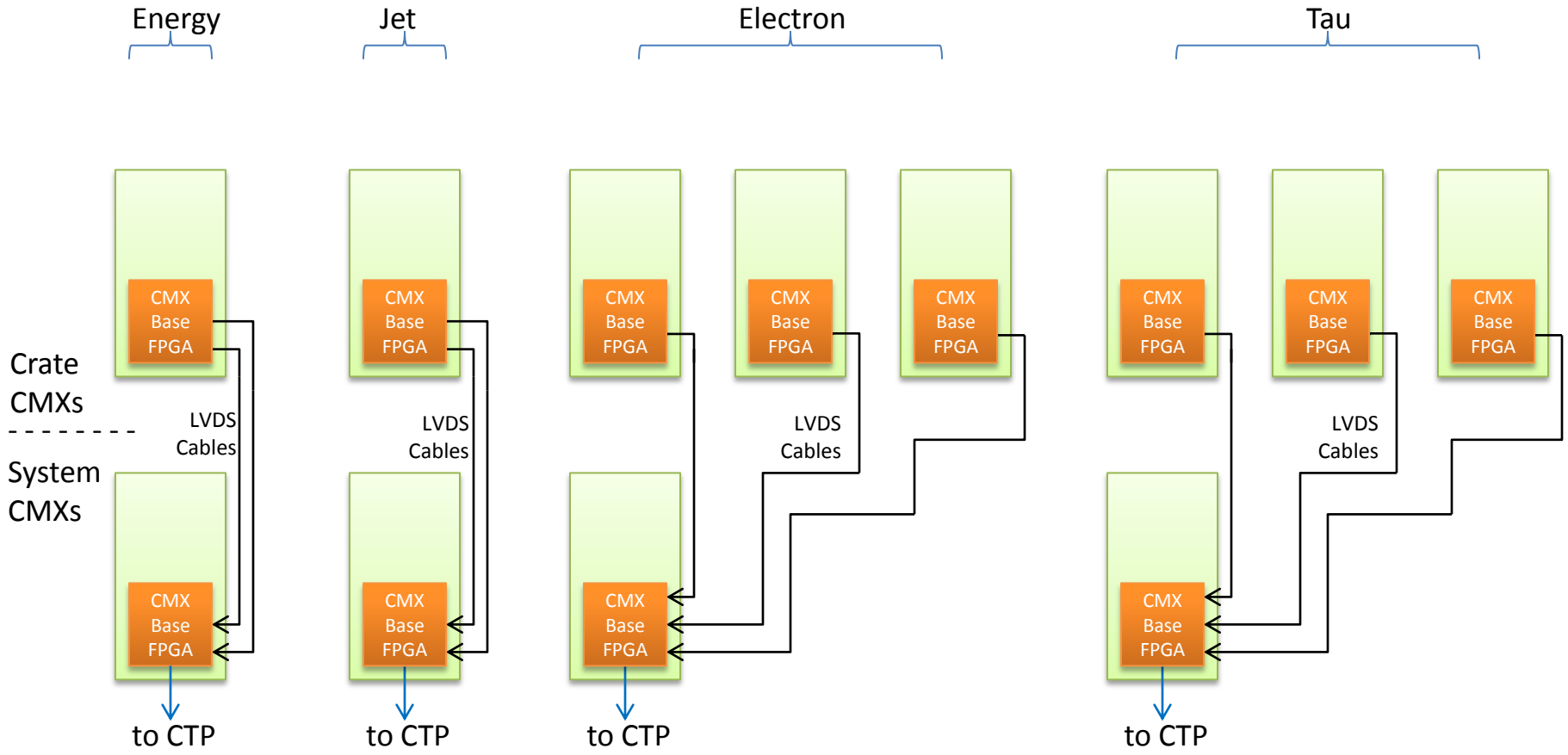
Figure 1-6 shows the I/O and transceiver banks for the XC6VLX550T. The black dots denote the global clock banks.

CMX IO Bank Assignment for Processor Inputs

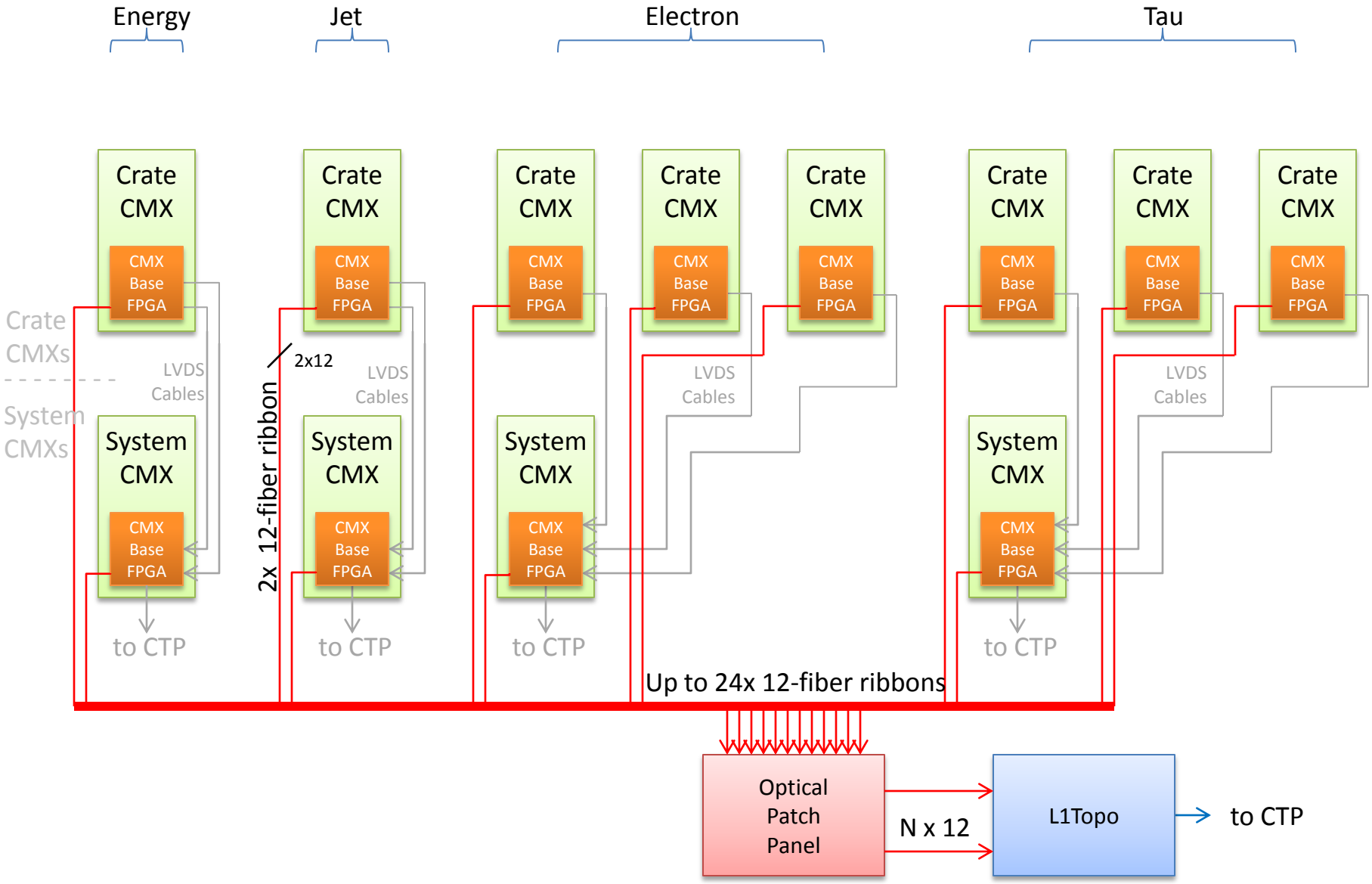
(using only Inner Columns and exactly two Regional Clocks per Horizontal Row)

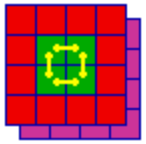


CMX emulation of CMM functionality (no TP involved)



L1topo receives Zero-Suppressed data from all CMXs



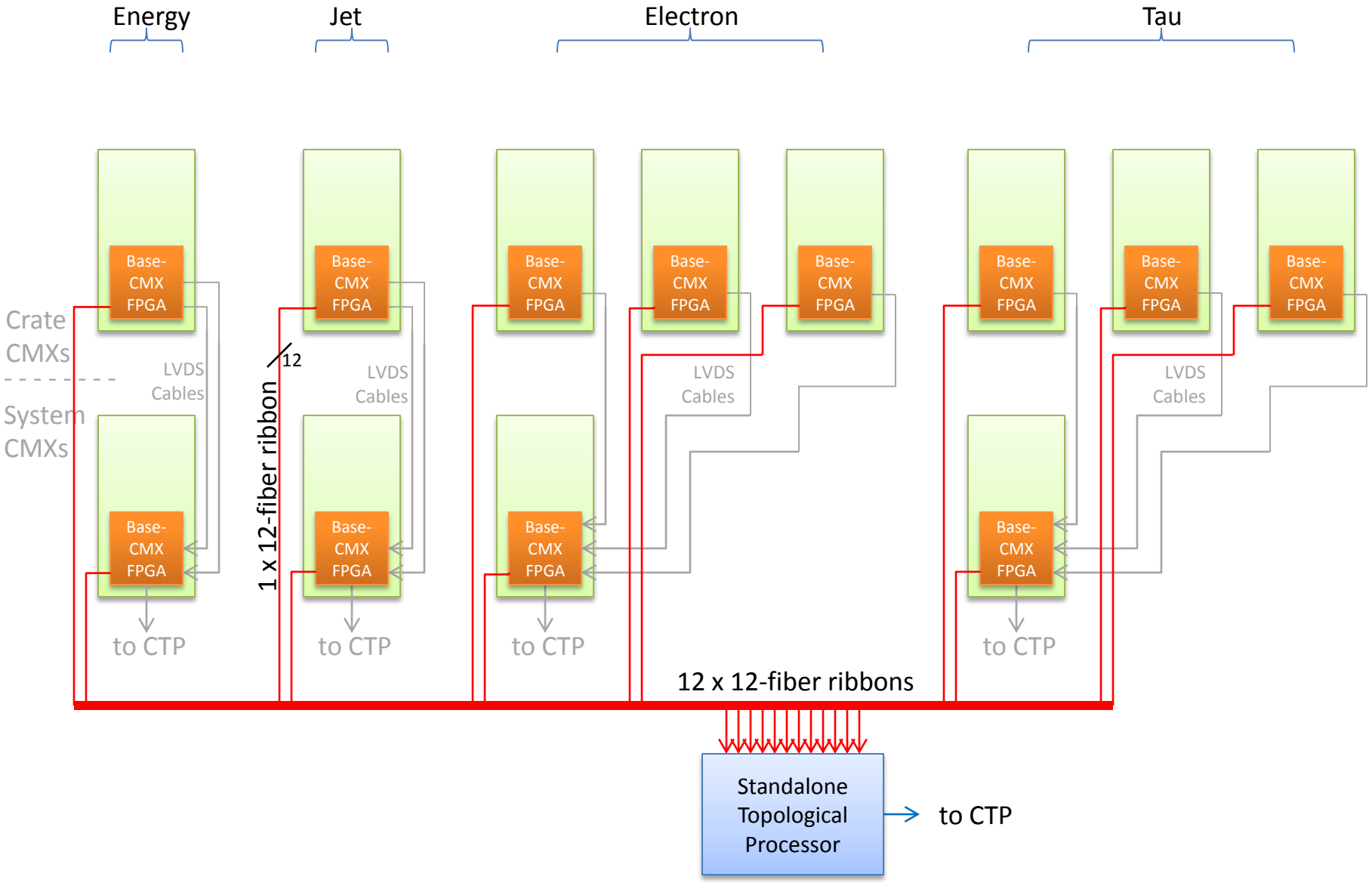


Older CMX Diagrams

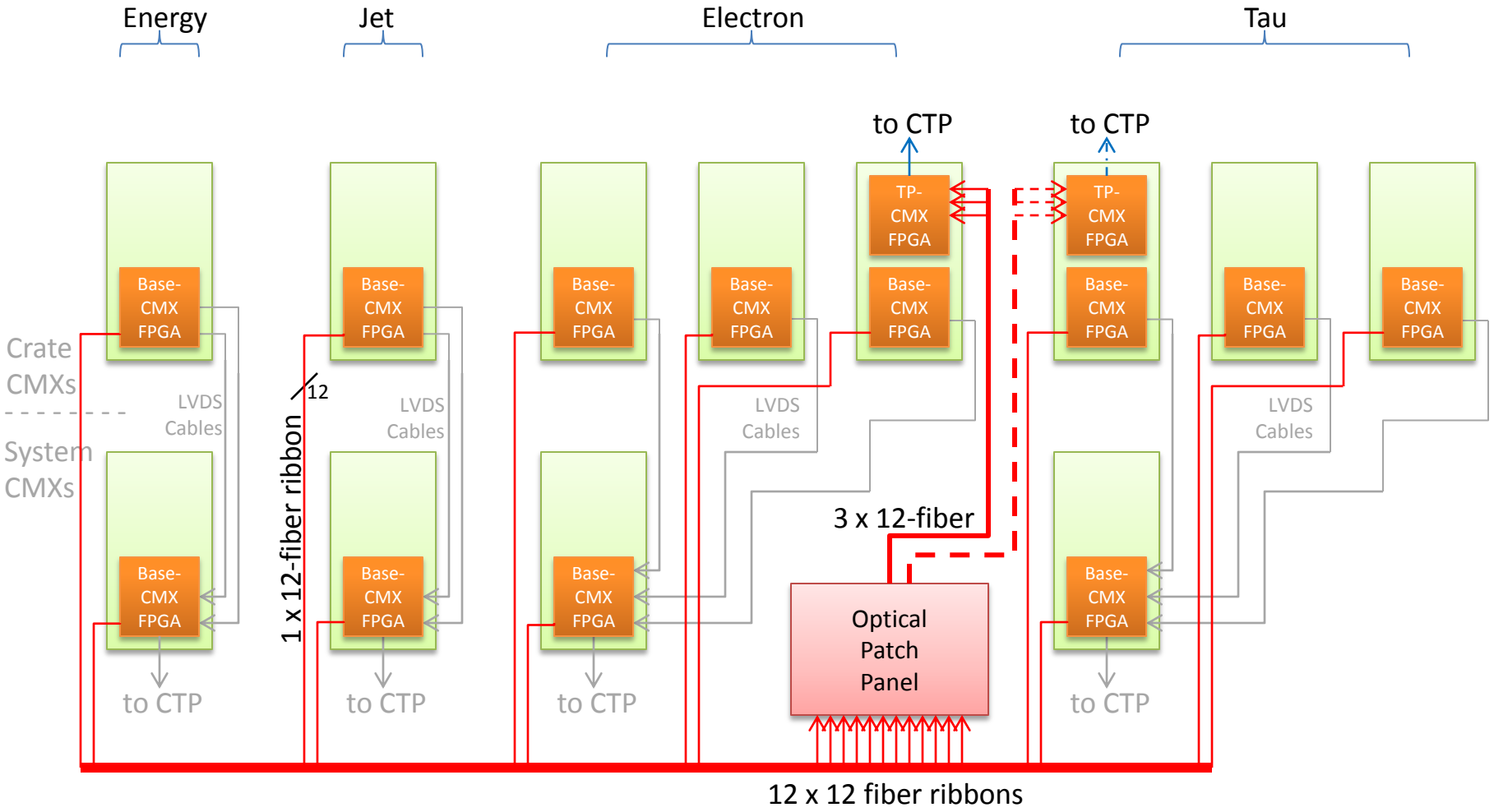
Historical repository

Some still valid or may need editing

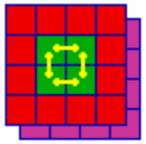
2. Standalone TP receiving Raw CMX Inputs

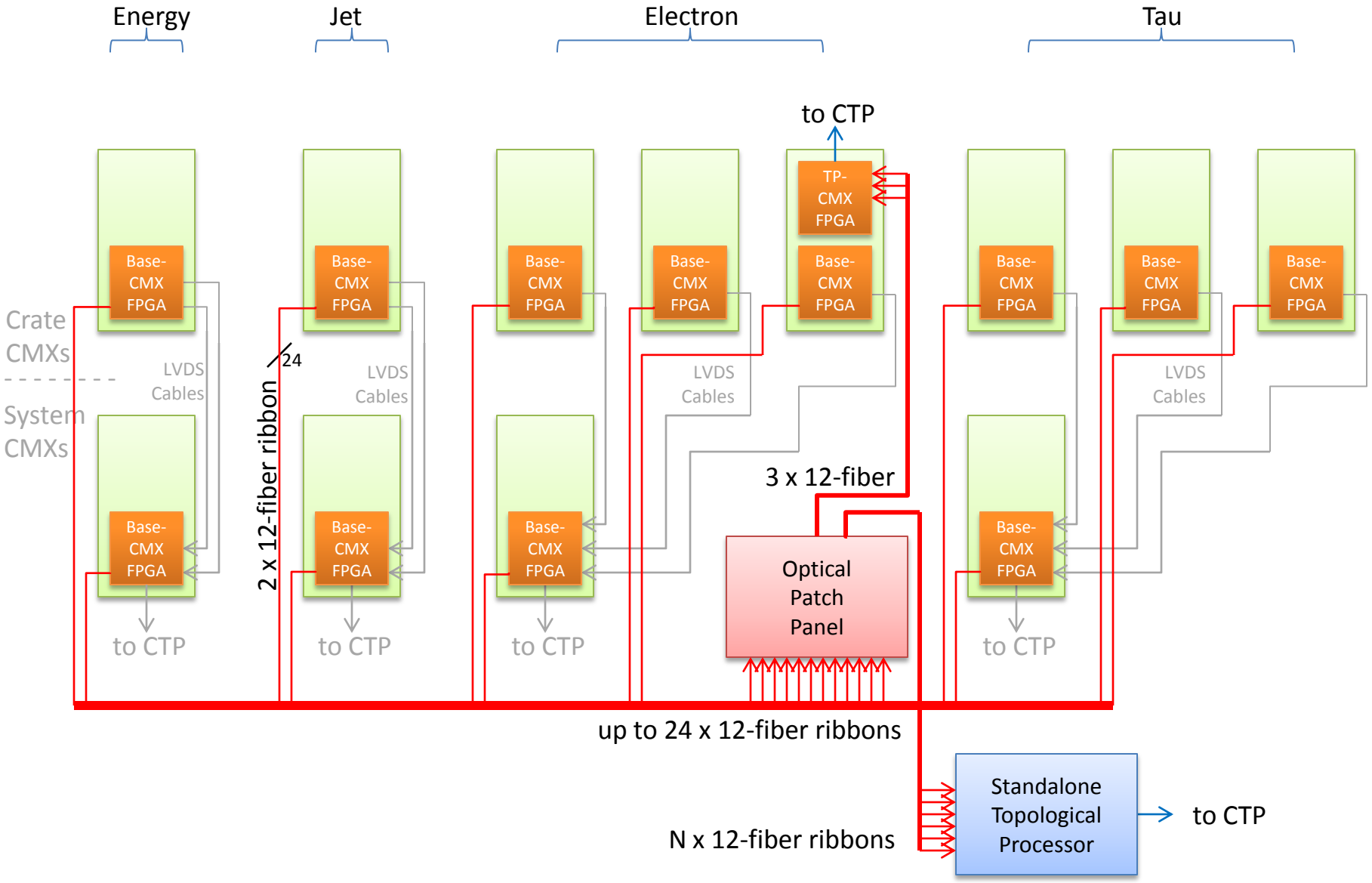


4. One (or more) CMX TP receiving Zero-Suppressed Inputs



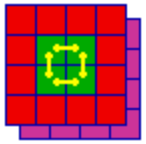
5. CMX TP & Standalone TP receiving Zero-Suppressed Inputs

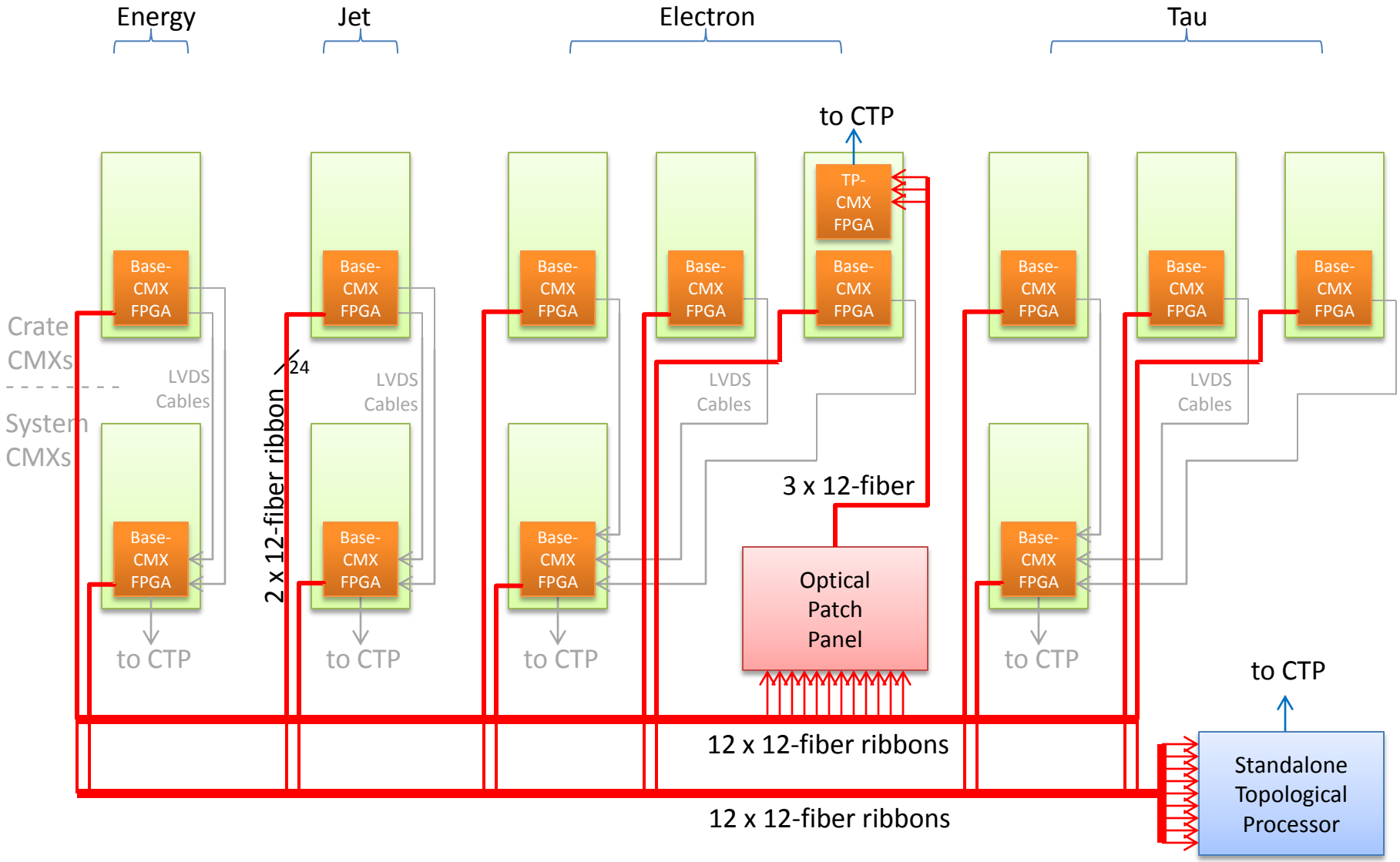




MICHIGAN STATE UNIVERSITY

6. CMX TP receiving Zero-Suppressed & Standalone TP raw inputs





MICHIGAN STATE UNIVERSITY

7. Example of TP-CMX FPGA in Crate to System communication