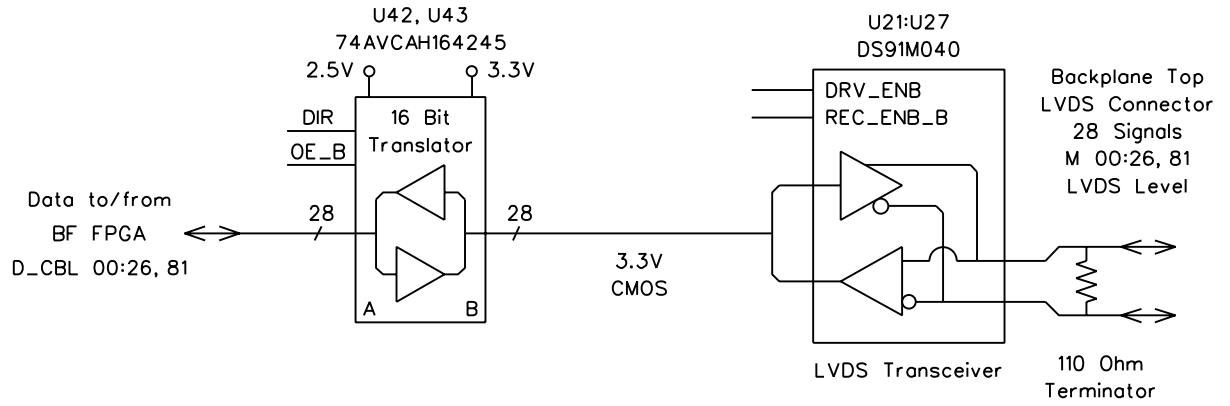
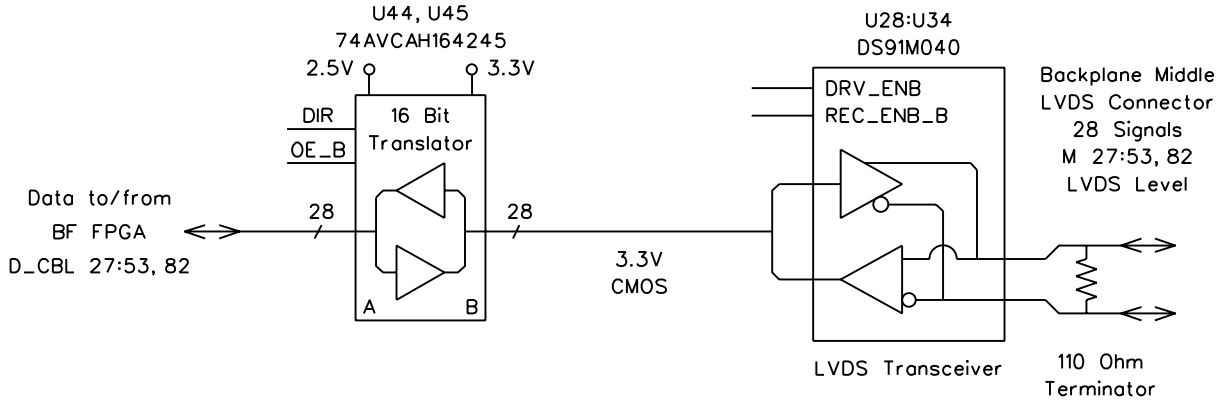
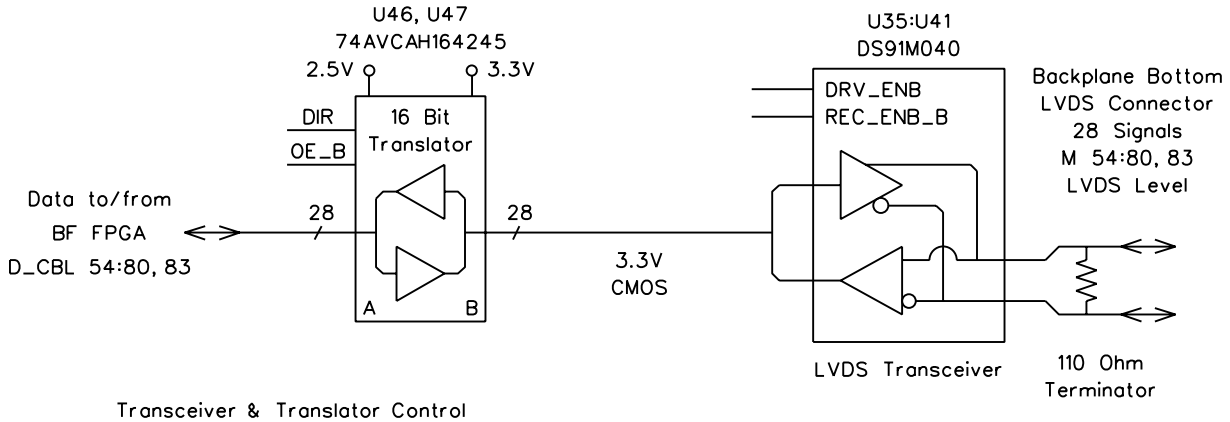
Backplane LVDS Cable Transceivers

2.5V CMOS Data
from/to the
Base Function FPGA
I/O Banks: 15, 16, 17

Backplane LVDS
Cable Connections







Transceiver & Translator Control Signals: DRV_ENB, REC_ENB_B, DIR, and OE_B Come from a Combination of BF and BSPT FPGA Signals with Hardwired Oversight Logic

The Direction of Data Flow Is Independently Controllable for the 3 Backplane LVDS Cables.

DIR Hi --> A is an Input
B is an Output

The LVDS Transceiver Master Enable and Failsafe Pins Are Controlled by Separate Jumpers for the Top, Middle, and Bottom LVDS Cables.

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