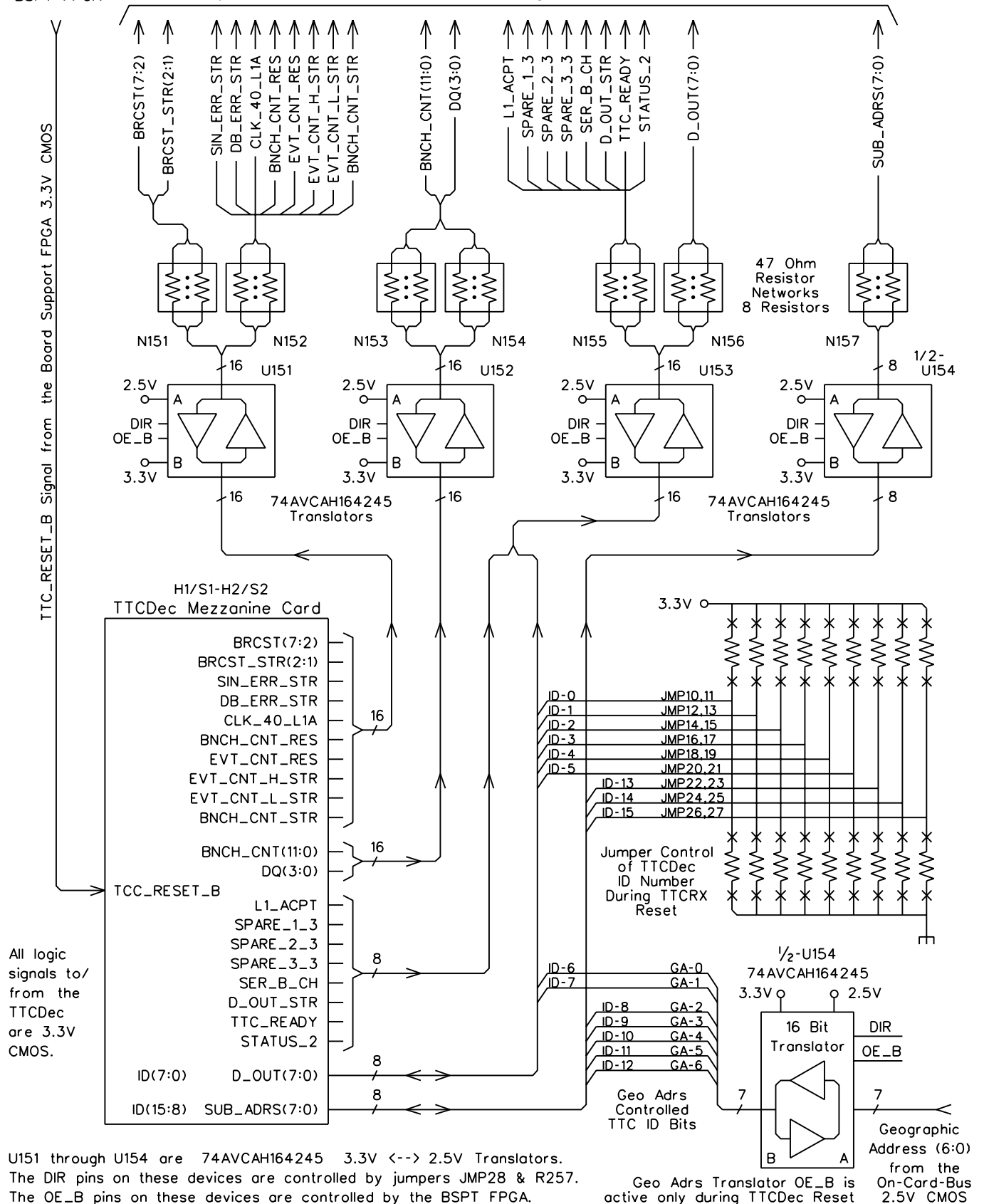


TTCDec Data Distribution

Rev. 25-Sept-2013

TCC_RESET_B
from the
BSPT FPGA

TTCDEC Output Signals Back Terminated 2.5V CMOS
All Signals go to the Board Support and Topological Processor FPGAs
Only L1_ACPT and BNCH_CNT_RES go to the Base Function FPGA



U151 through U154 are 74AVCAH164245 3.3V <-> 2.5V Translators. The DIR pins on these devices are controlled by jumpers JMP28 & R257. The OE_B pins on these devices are controlled by the BSPT FPGA.

Geo Adrs Translator OE_B is active only during TTCDec Reset

Geographic Address (6:0) from the On-Card-Bus 2.5V CMOS