VME-OCB Management Logic in the BSPT

Clock 40.08 MHz

Hold VME-- Adrs Receivers transparent until after OCB_DS_B falls. Immediately return them to being transparent when OCB_DS_B returns HI.

Clock the D Flip-Flop at the output of the "That's Me" decoder only after OCB_DS_B has fallen, the OCB Adrs lines are stable, and the decoder output has settled.

VME_ADRS_RECVR_LE

OCB_DS_B

CLK

D   Q

RESET

"This Cycle is for Me"

OCB_GEO_ADRS(6:0)

OCB_A(23:0)

VME-- Address Range Decoder

aka the CMX card's "That's Me" Decoder

OCB_SYS_RESET_B

OR

RESET

Q

SET

BSPT_SEND_VME_DTACK_B

Delay for the cycle to take place on the CMX card

BSPT_VME_D_BUS_TRNCVR_OE_B

OCB_D_BUS_TRNSLT_OE_B

VME_D_BUS_TRNCVR_DIR

AND

OCB_WRITE_B

OCB_D_BUS_TRNSLT_DIR

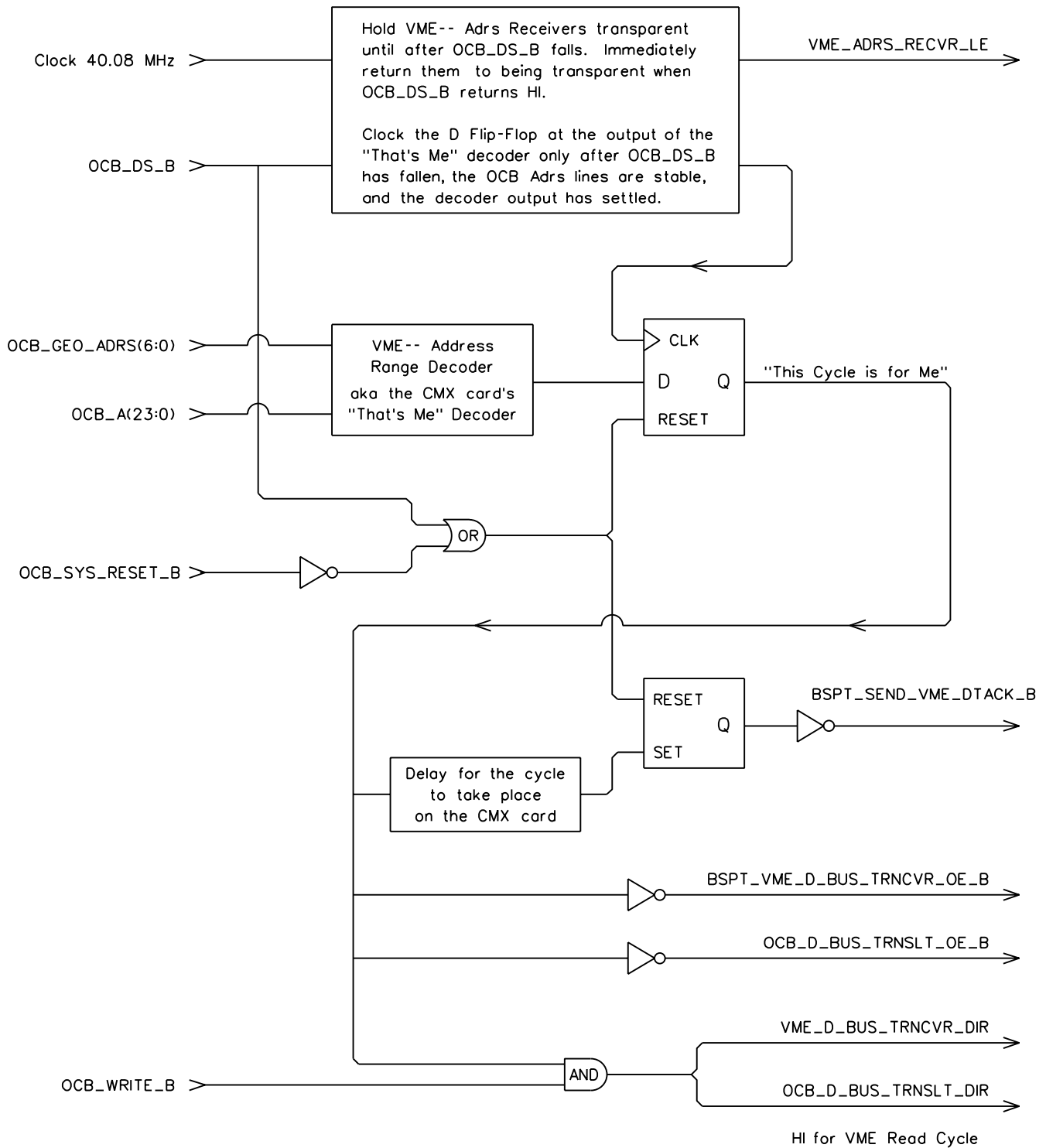HI for VME Read Cycle

Logic in the BSPT's VME/OCB management section may set the following signals to static levels. For normal VME-- bus operation these signals do not need to switch levels:
   VME_ADRS_AND_CTRL_RECVR_OE_B   always Low
   OCB_ADRS_AND_CTRL_TRNSLT_DIR   always Low
   VME_CTRL_RECVR_LE   always Hi
   BSPT_OCB_ADRS_AND_CTRL_TRNSLT_OE_B   once the
         Virtex FPGAs are Configured then always Low

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