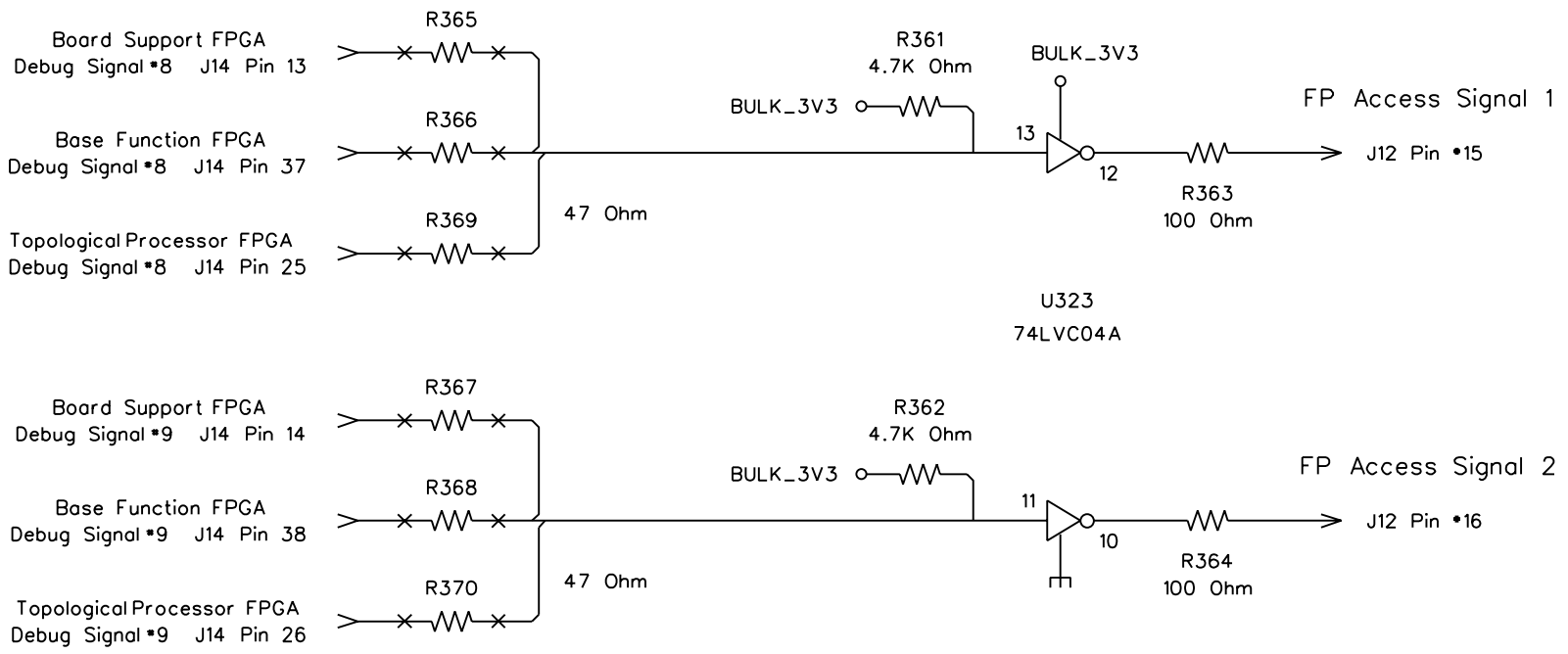
Two Access Signals on the Front Panel



Front panel connector J12 pins 15 and 16 provide access to two buffered signals from either the: Board Support FPGA, the Base Function FPGA, or the Topological Processor FPGA.

These two front panel access signals can be used e.g.: clock monitoring, S-Link Busy, scope or logic analyzer trigger.

All J12 odd numbered pins 1 through 9 are grounds.
The 74LVC04A buffer can provide 20 mA max output.
The 74LVC04A has a logic Hi input minimum of 2.0 volts.
The Xilinx 2.5V CMOS output logic Hi is a minimum of 2.1 volts.
The Xilinx I/O pin clamp diode can handle 10 mA max.

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