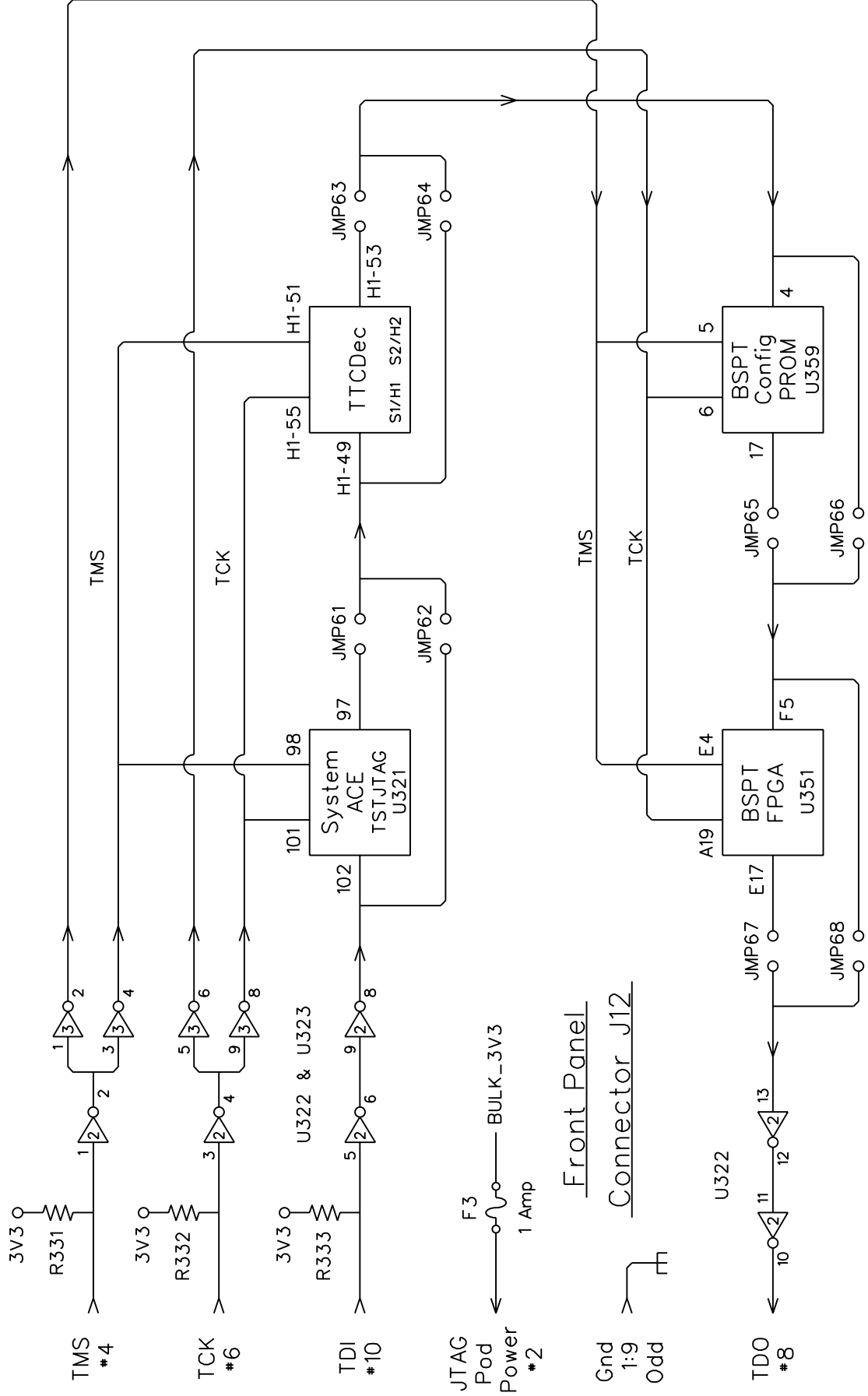
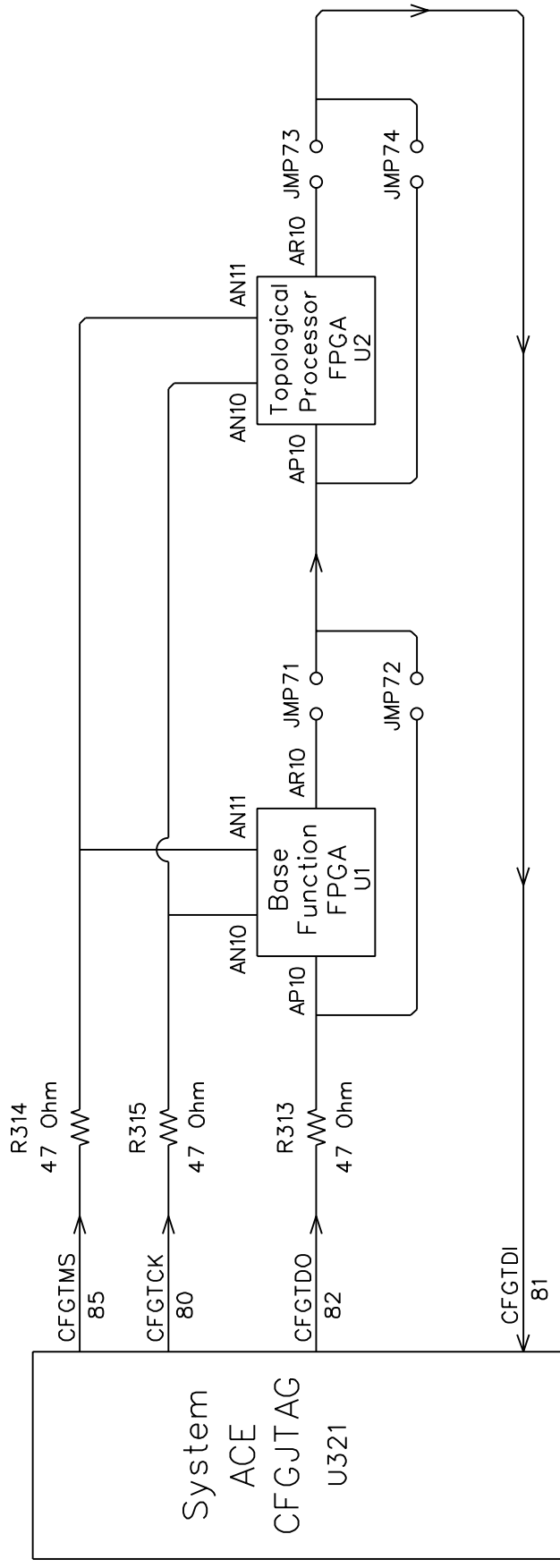


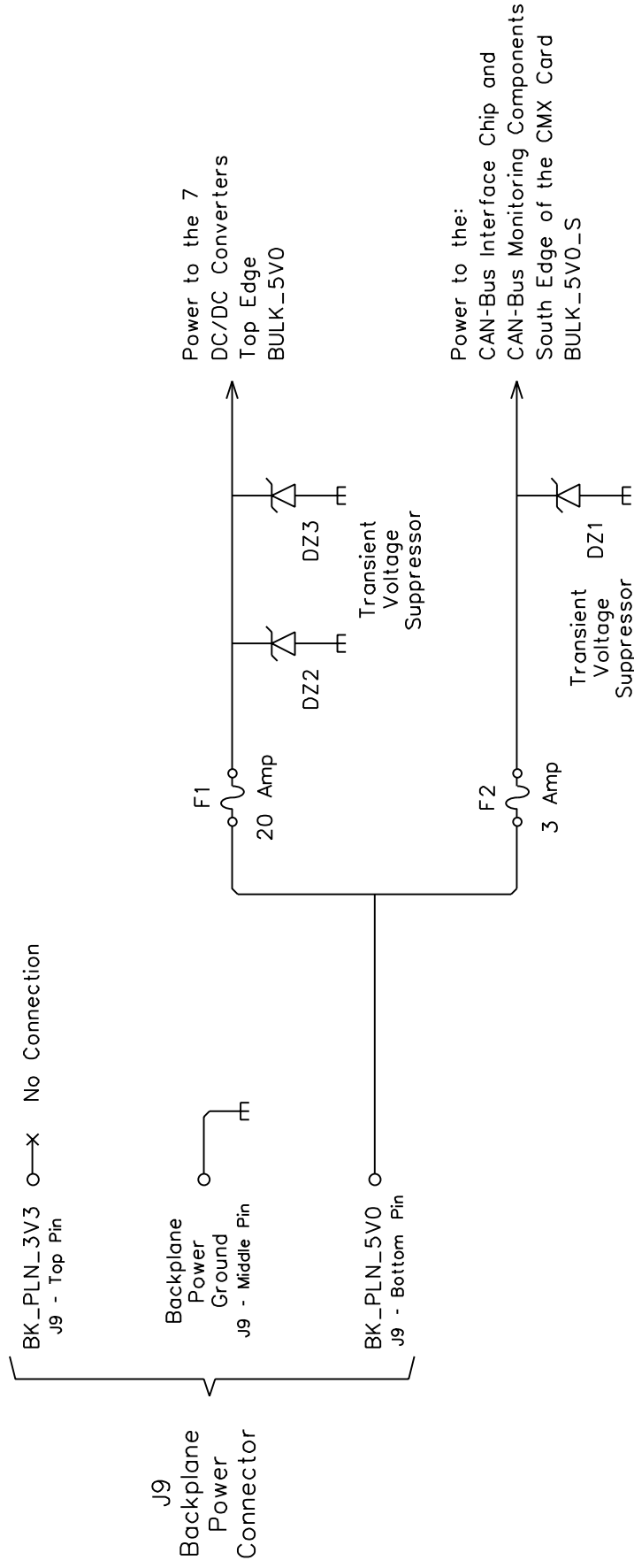
CMX TEST JTAG Chain



CMX CONFIGURATION JTAG Chain

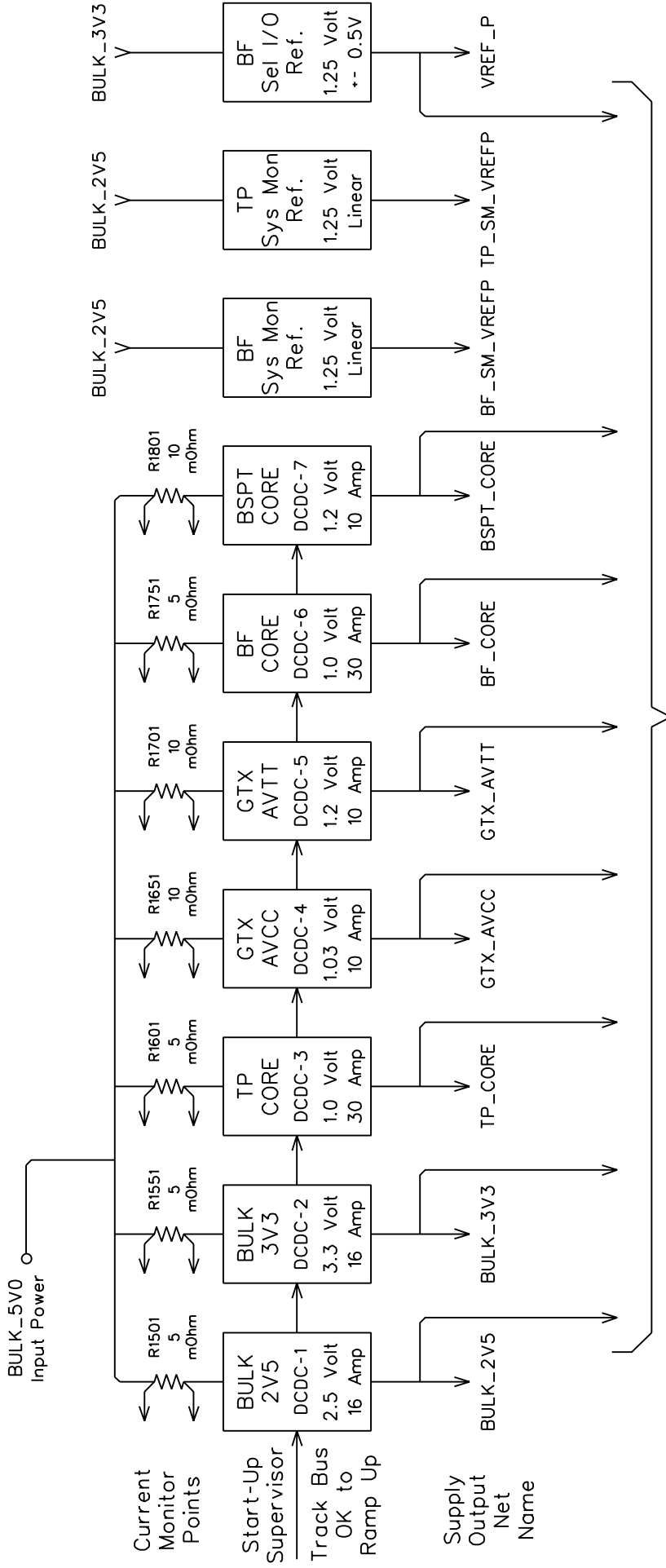


5 Volt Power Entry and Distribution



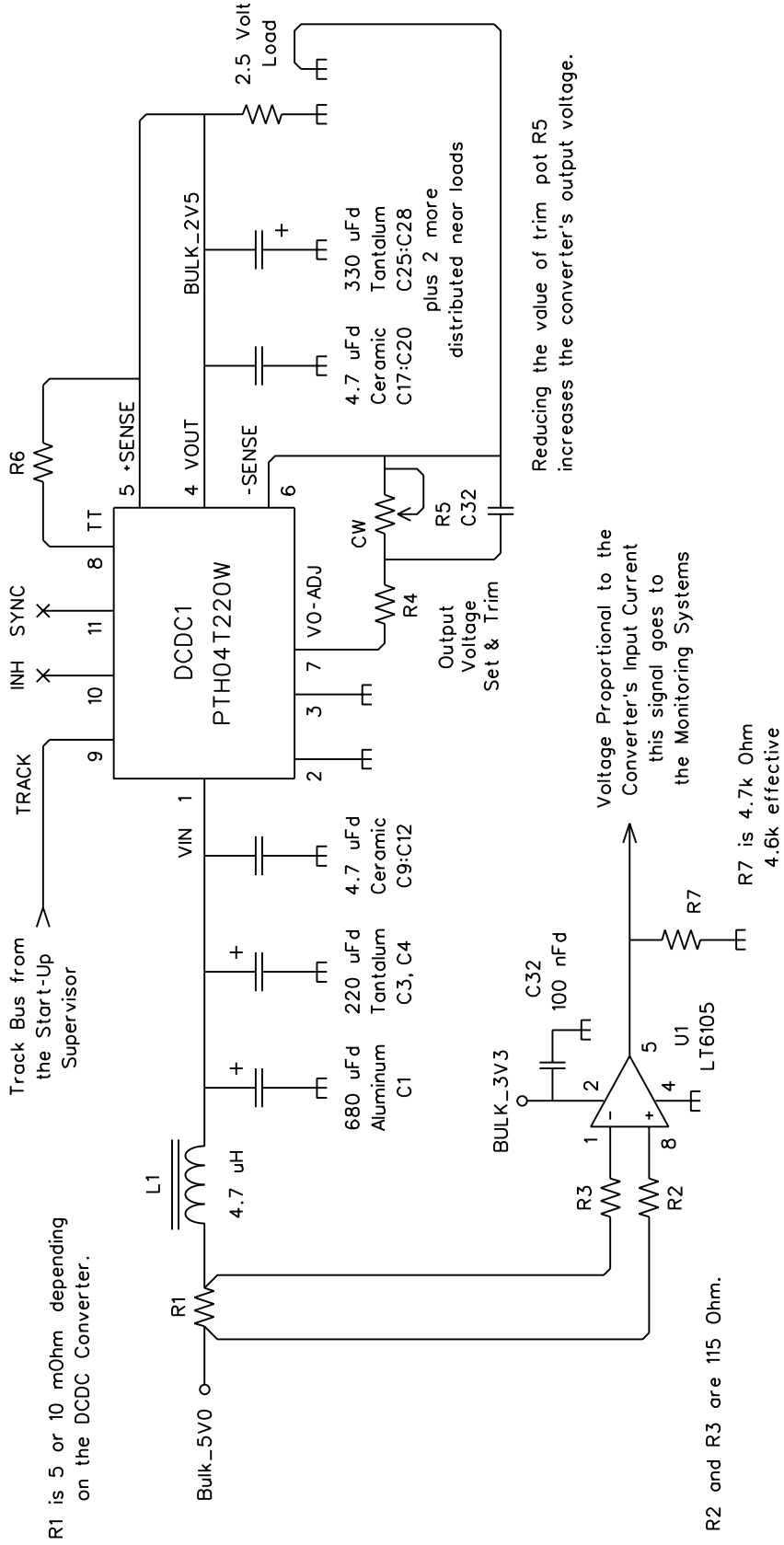
Note: On board SMD fuse F3 is mounted near the bottom front panel connector J12. It is in the JTAG Pod power circuit.

CMX On Card Power Supplies



Voltage Monitor Points to BF System Monitor, CAN-Bus Monitor, Hi/Low Supervisor, and Monitor Header J13

DC-DC Converter Design

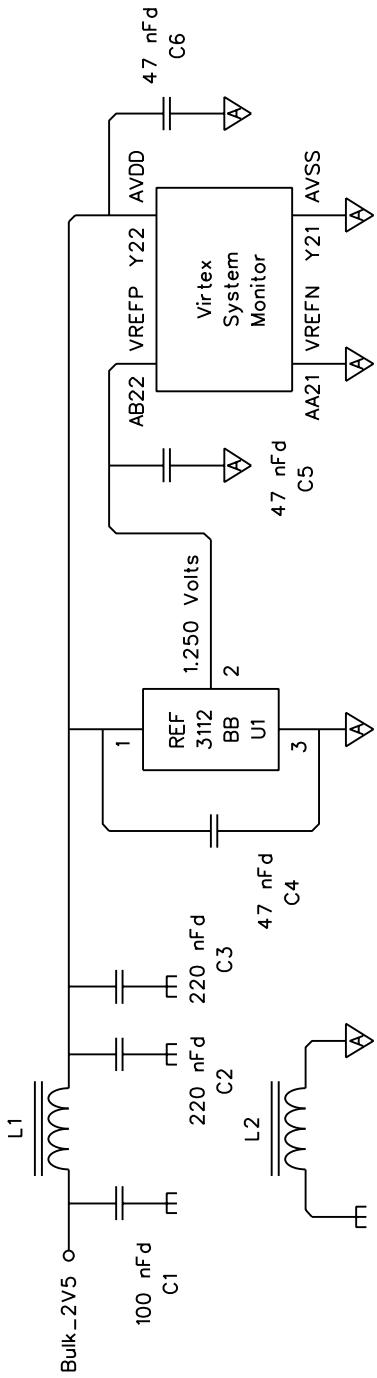


The BULK_2V5 DC/DC Converter is shown. The other 6 converters are similar in design. Actual reference designators are larger by 1500. Reference designators increment by 50 from one converter to the next.

The TP_CORE converter includes disable jumpers. The GTX_AVCC and GTX_AVTT converters include separate LC output filters for both their BF and TP loads.

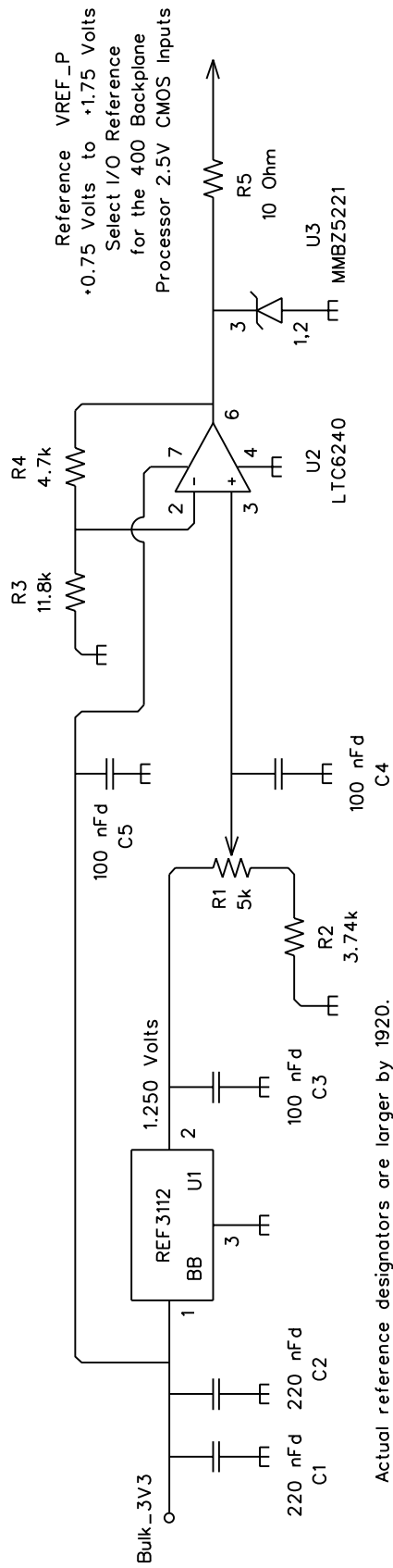
CMX Reference Supplies

BF and TP Virtex System Monitor References



The BF System Monitor Reference is shown. The TP reference design is the same. Actual reference designators are larger by 1900. TP reference designators increment by 10.

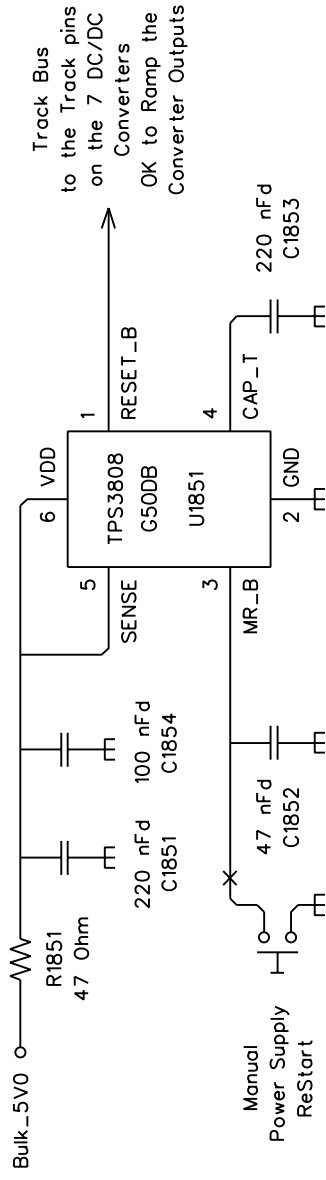
BF Select I/O Variable Reference for Backplane Signals



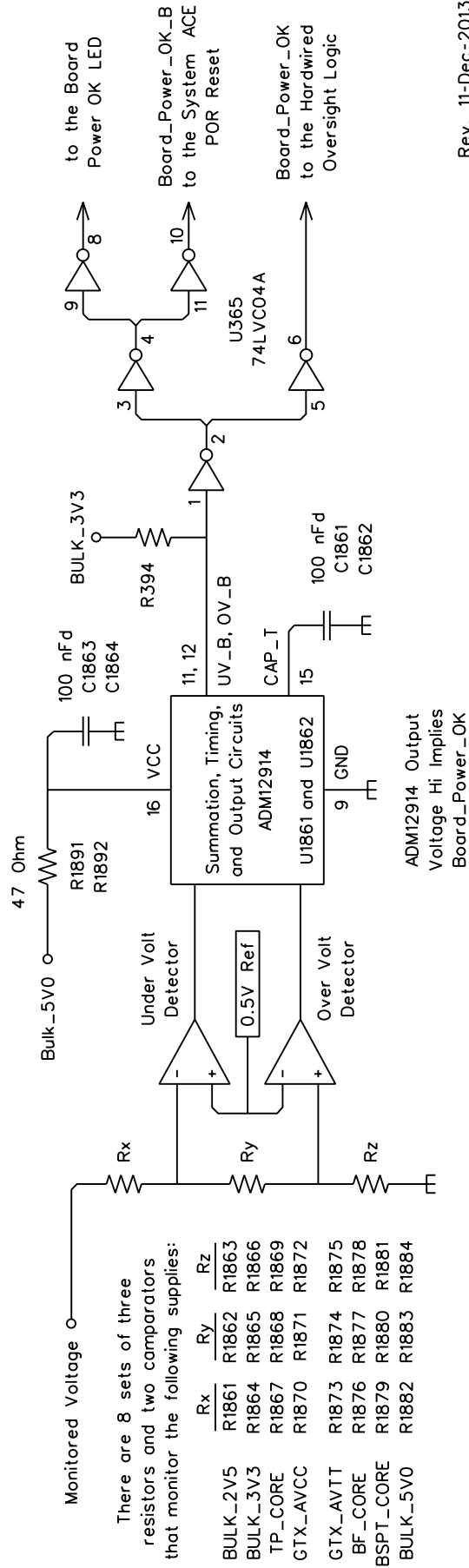
Actual reference designators are larger by 1920.

CMX Power Supply Supervisors

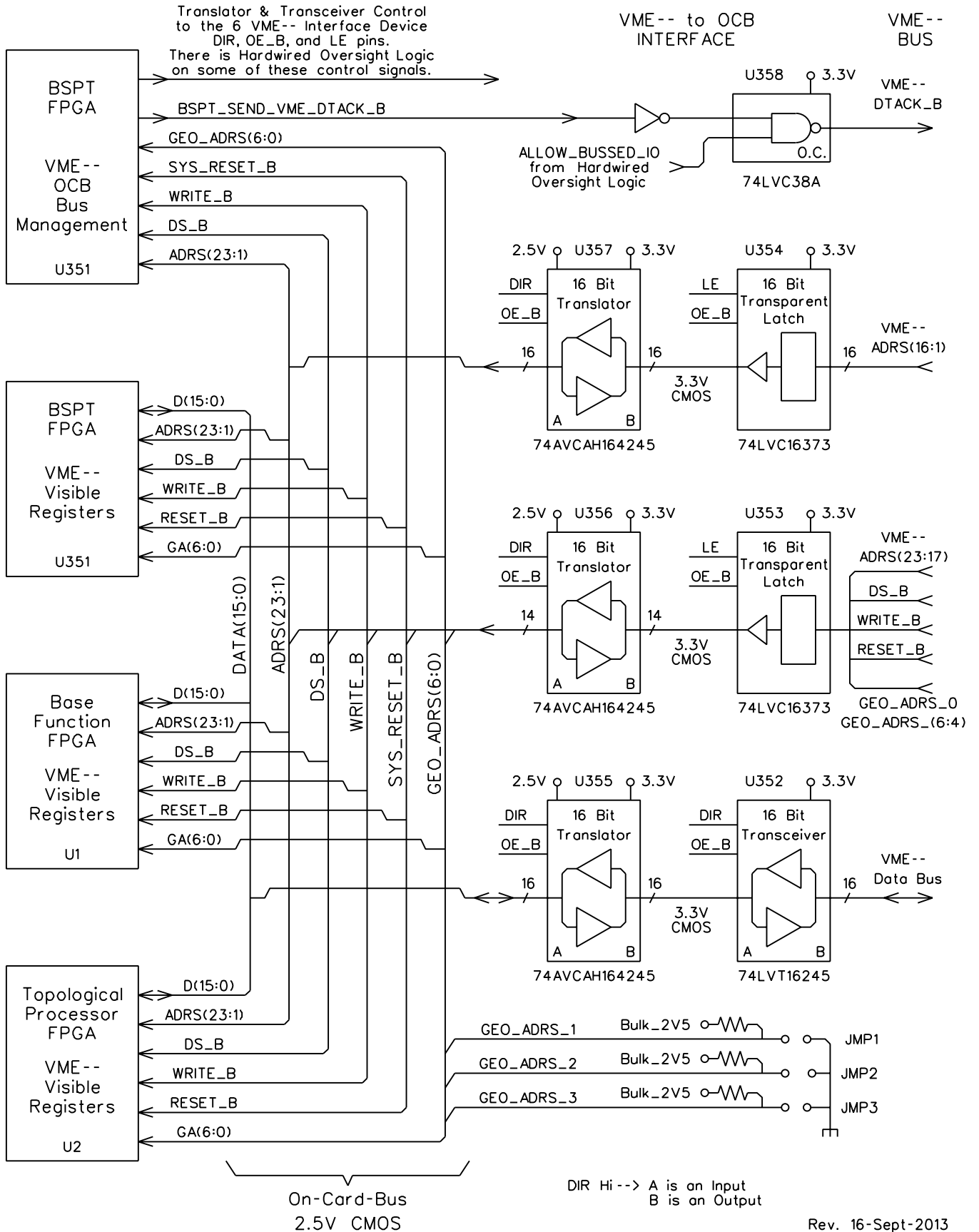
Converter Startup Supervisor



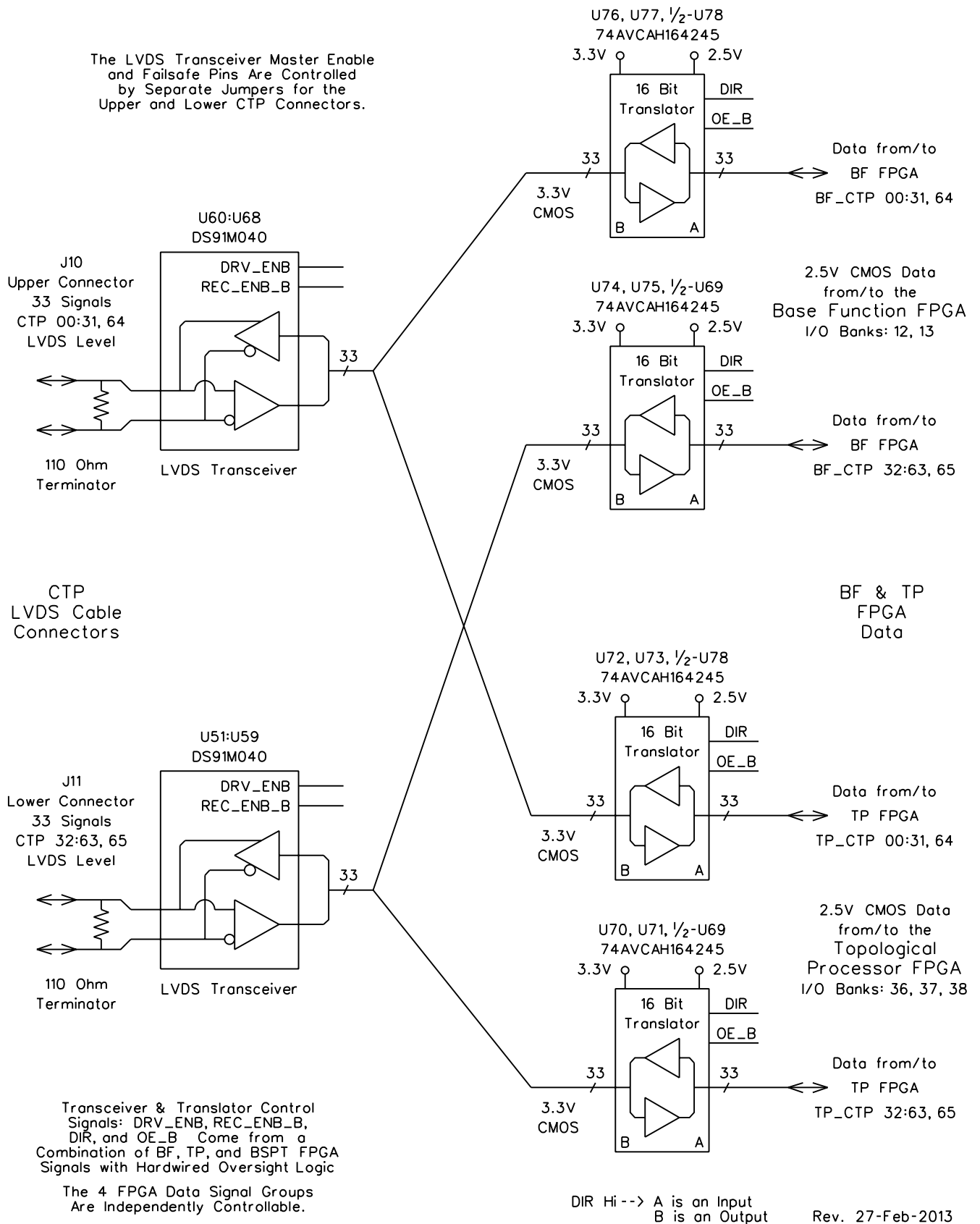
Hi/Low Board-Power-Ok Supervisor



On-Card-Bus and VME-- Interface



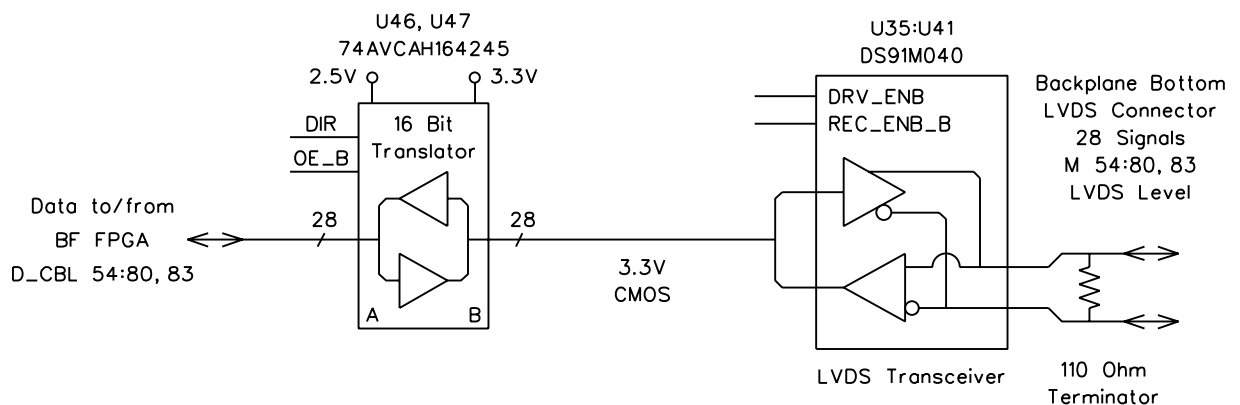
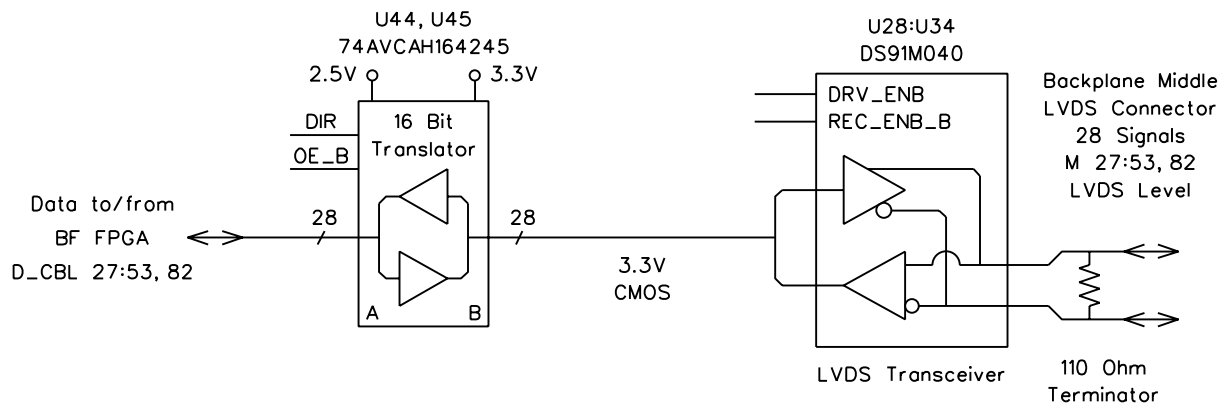
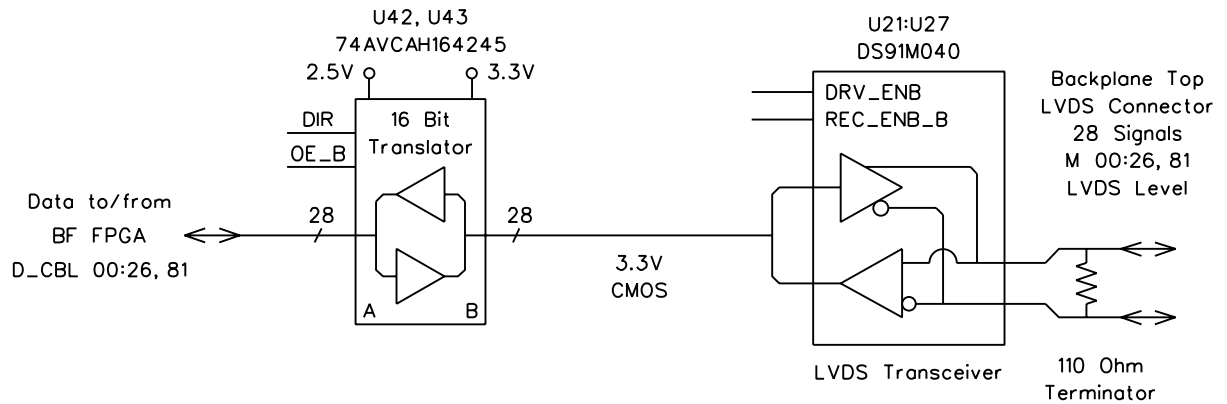
CTP Front Panel LVDS Transceivers



Backplane LVDS Cable Transceivers

2.5V CMOS Data
from/to the
Base Function FPGA
I/O Banks: 15, 16, 17

Backplane LVDS
Cable Connections



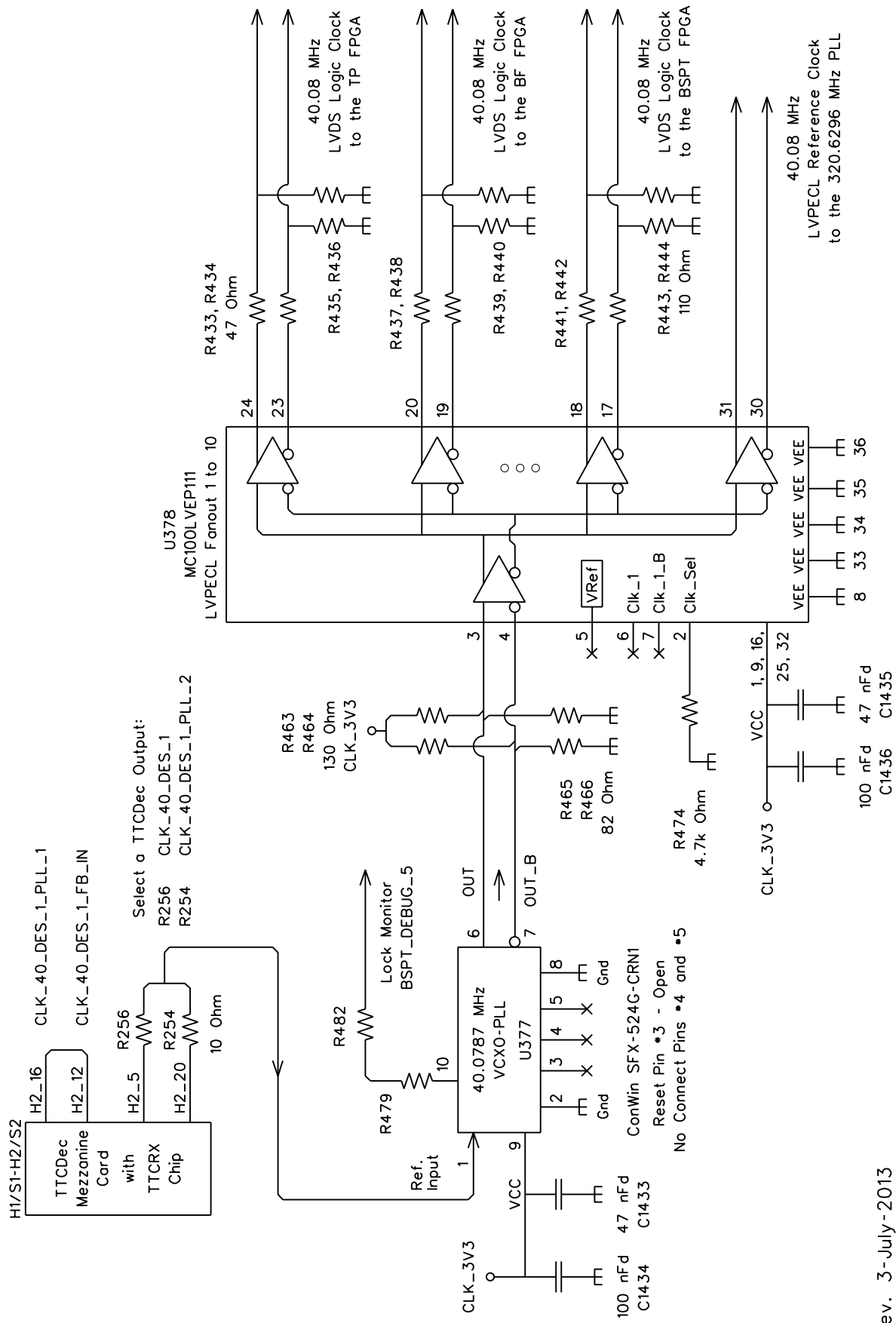
Transceiver & Translator Control
Signals: DRV_ENB, REC_ENB_B,
DIR, and OE_B Come from a
Combination of BF and BSPT FPGA
Signals with Hardwired Oversight Logic

The Direction of Data Flow Is
Independently Controllable for
the 3 Backplane LVDS Cables.

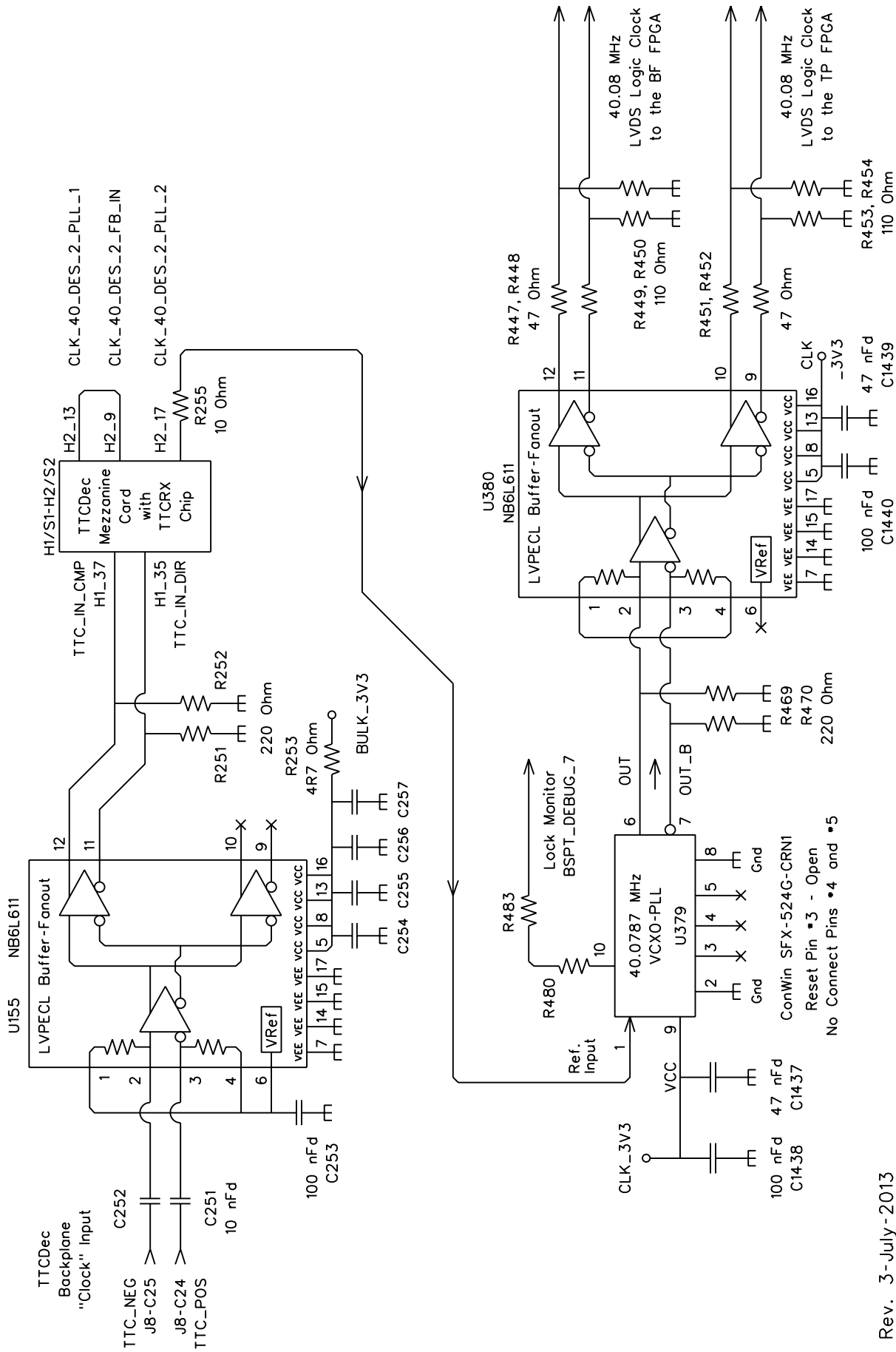
DIR Hi--> A is an Input
B is an Output

The LVDS Transceiver Master Enable
and Failsafe Pins Are Controlled
by Separate Jumpers for the
Top, Middle, and Bottom LVDS Cables.

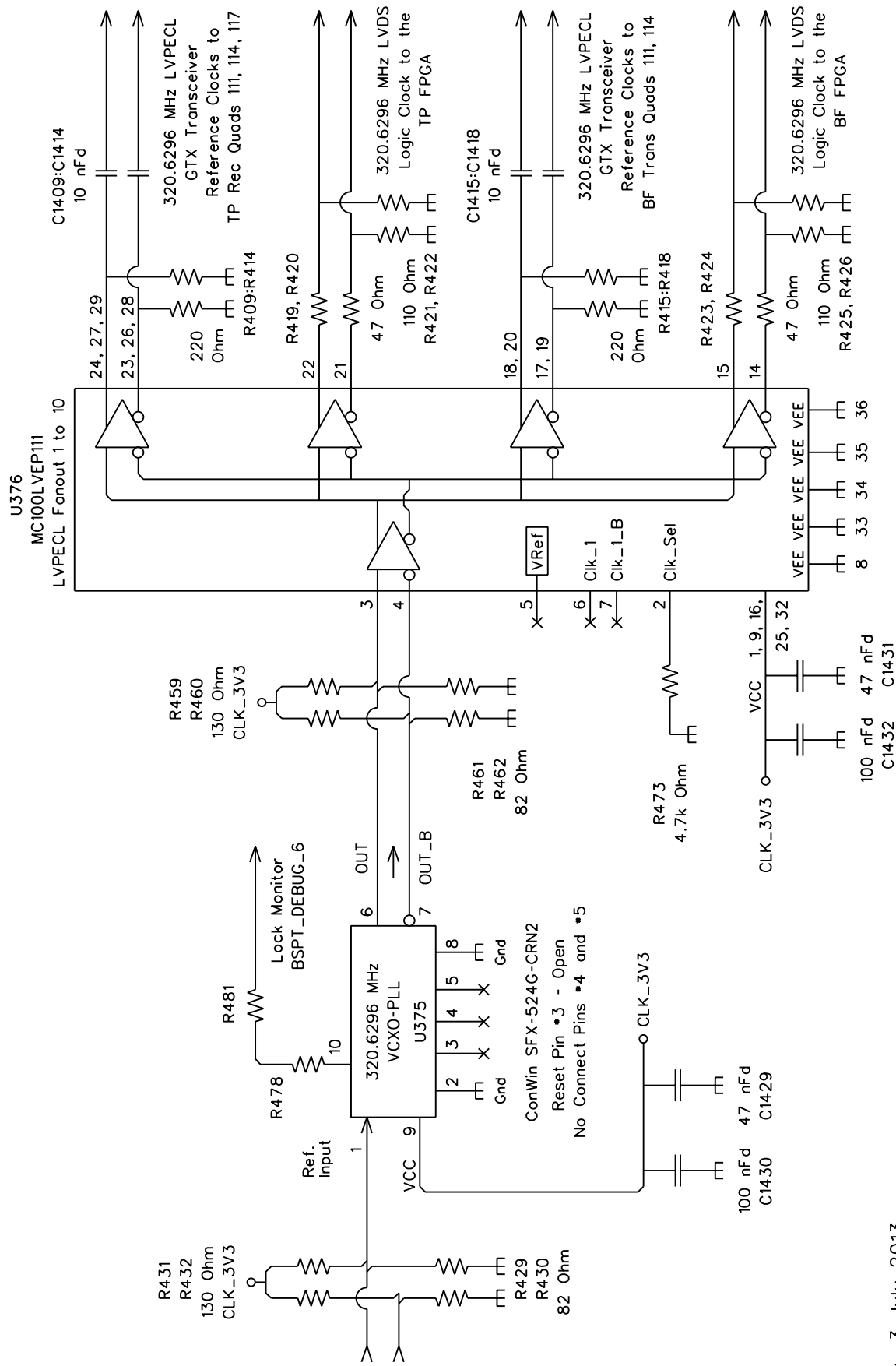
CMX 40.08 MHz Deskew-1 LHC Clock



CMX 40.08 MHz DeSkew-2 LHC Clock

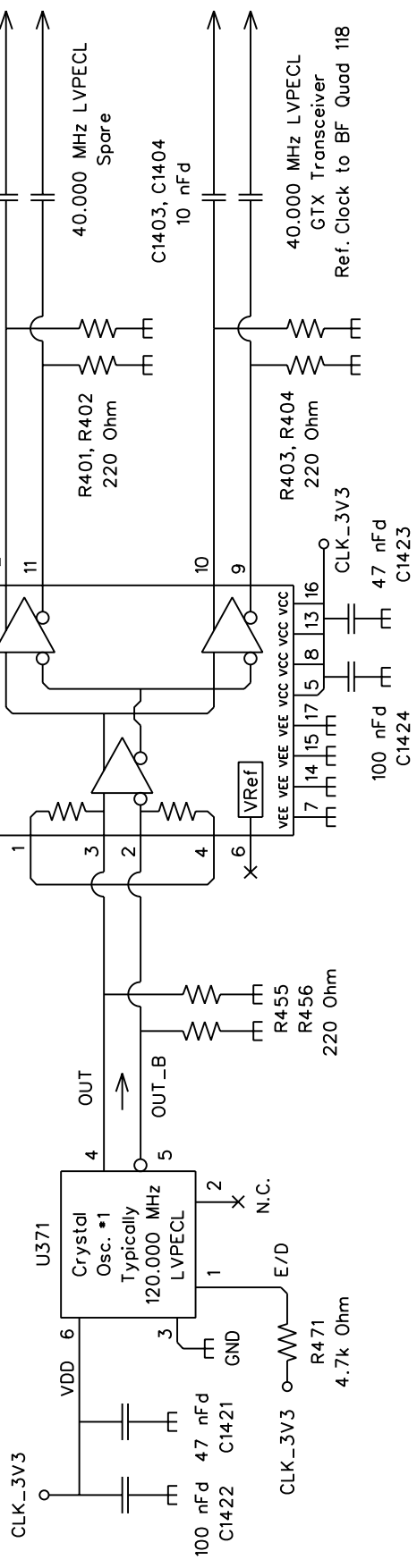


CMX 320.6296 MHz LVPECL LHC Clock

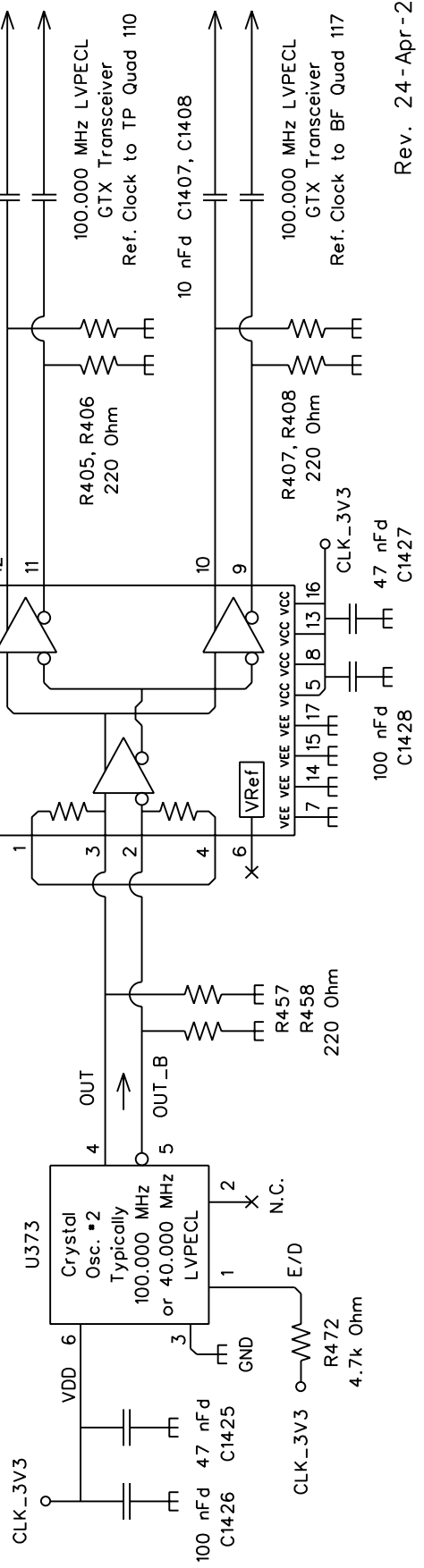


CMX Crystal Oscillator #1 and #2

Crystal Oscillator #1



Crystal Oscillator #2

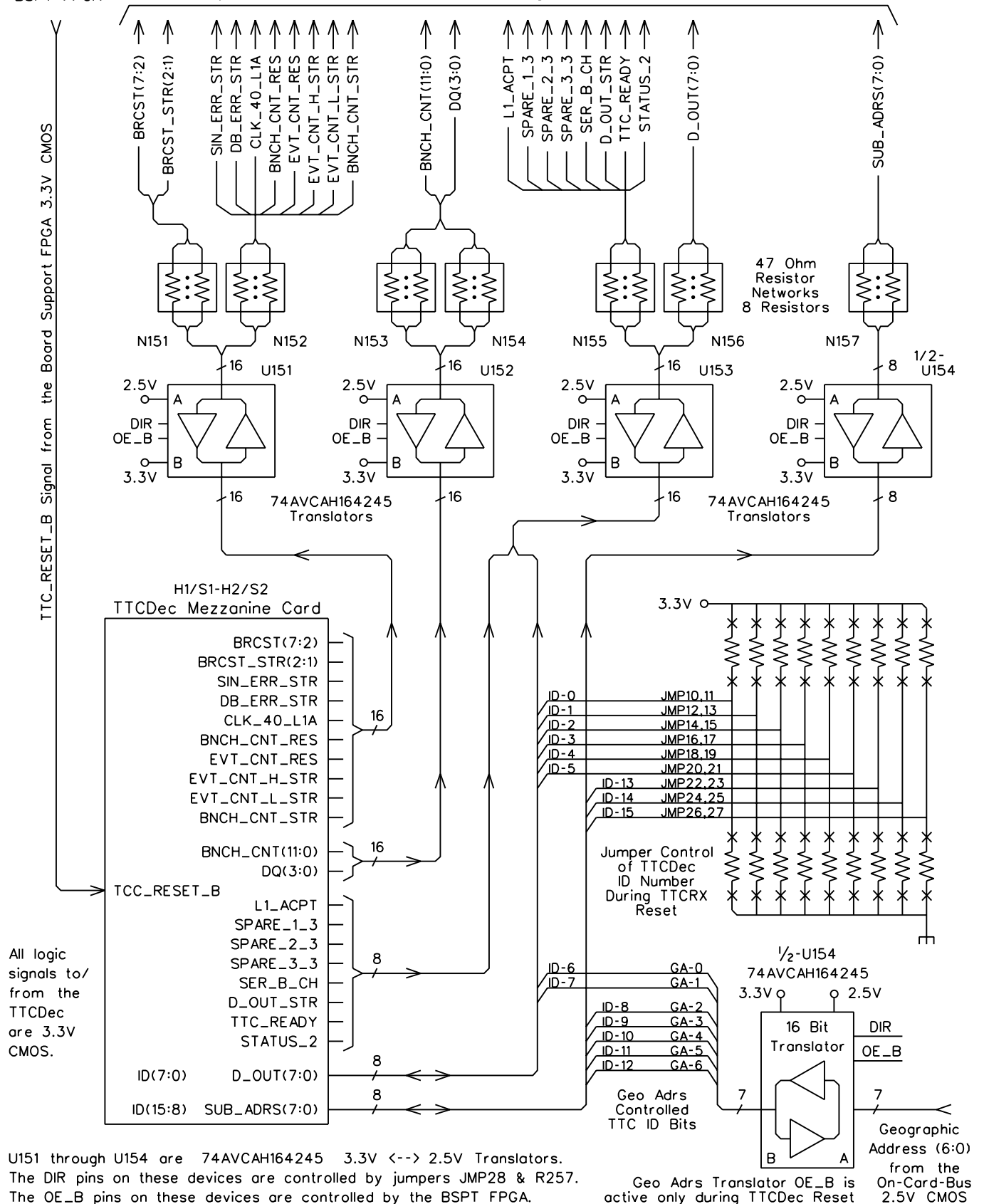


TTCDec Data Distribution

Rev. 25-Sept-2013

TCC_RESET_B
from the
BSPT FPGA

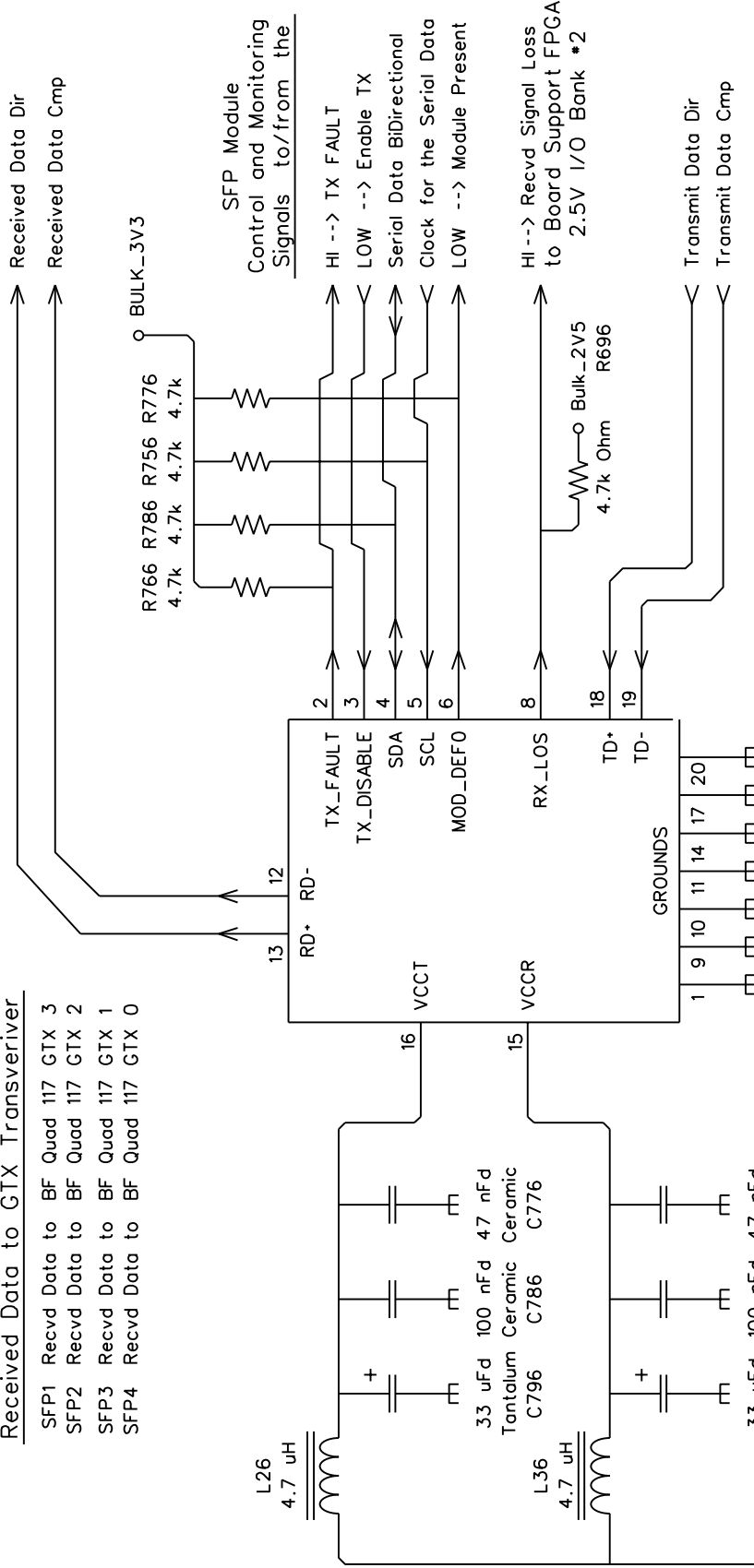
TTCDEC Output Signals Back Terminated 2.5V CMOS
All Signals go to the Board Support and Topological Processor FPGAs
Only L1_ACPT and BNCH_CNT_RES go to the Base Function FPGA



SFP Low-Speed Optical Transceivers

Received Data to GTX Transceiver

- SFP1 Recvd Data to BF Quad 117 GTX 3
- SFP2 Recvd Data to BF Quad 117 GTX 2
- SFP3 Recvd Data to BF Quad 117 GTX 1
- SFP4 Recvd Data to BF Quad 117 GTX 0



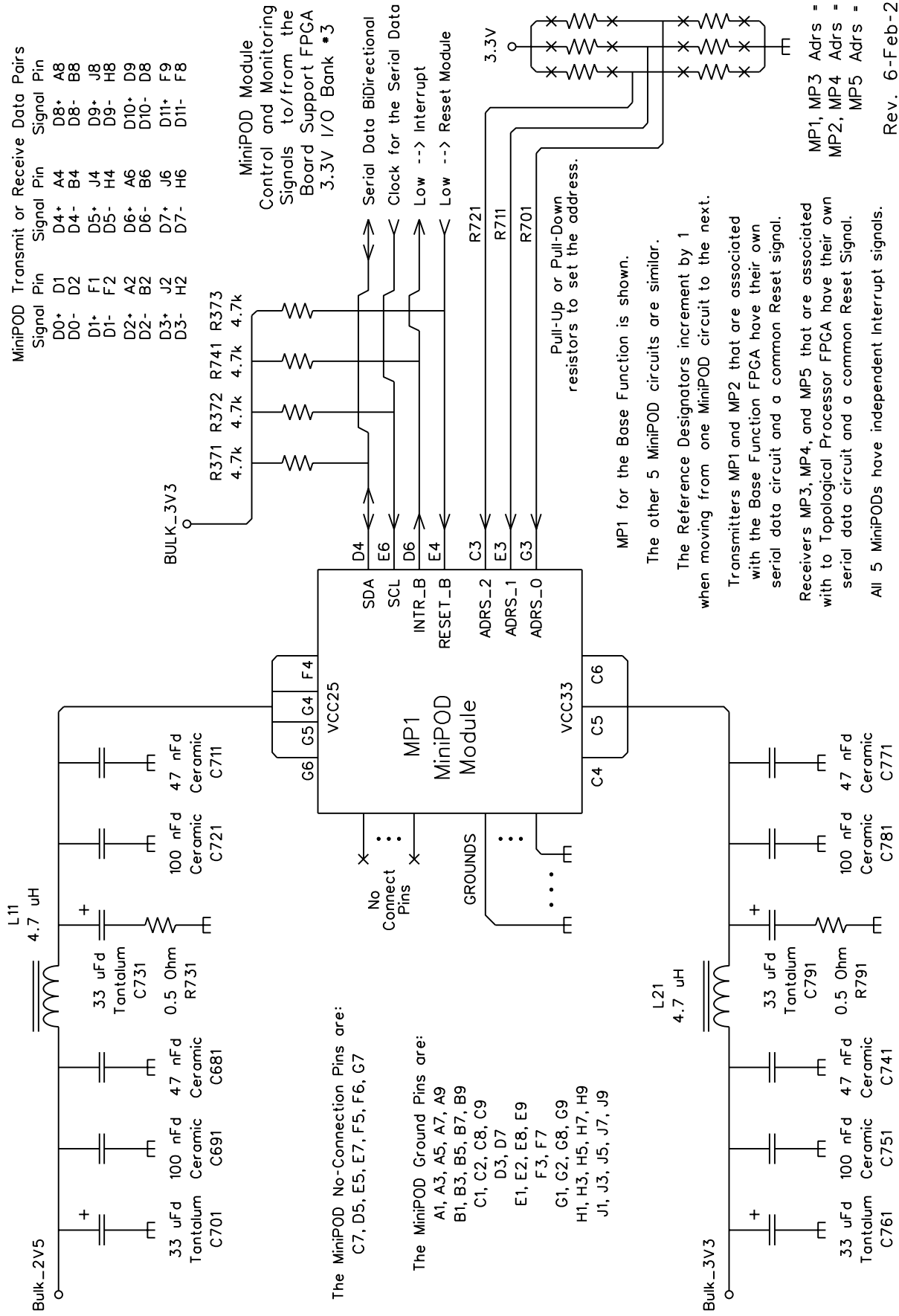
Transmit Data from GTX Transceiver

- SFP1 BF DAQ Data from BF Quad 118 GTX 3
- SFP2 BF ROI Data from BF Quad 118 GTX 2
- SFP3 TP DAQ Data from TP Quad 110 GTX 1
- SFP4 TP ROI Data from TP Quad 110 GTX 0

SFP Pin #7 is not connected.

SFP1 for the Base Function DAQ is shown.
The other 3 SFP circuits are similar.
The Reference Designators increment by 1 when moving from one SFP circuit to the next.

MiniPOD Hi-Speed Optical Components



System-ACE Connections

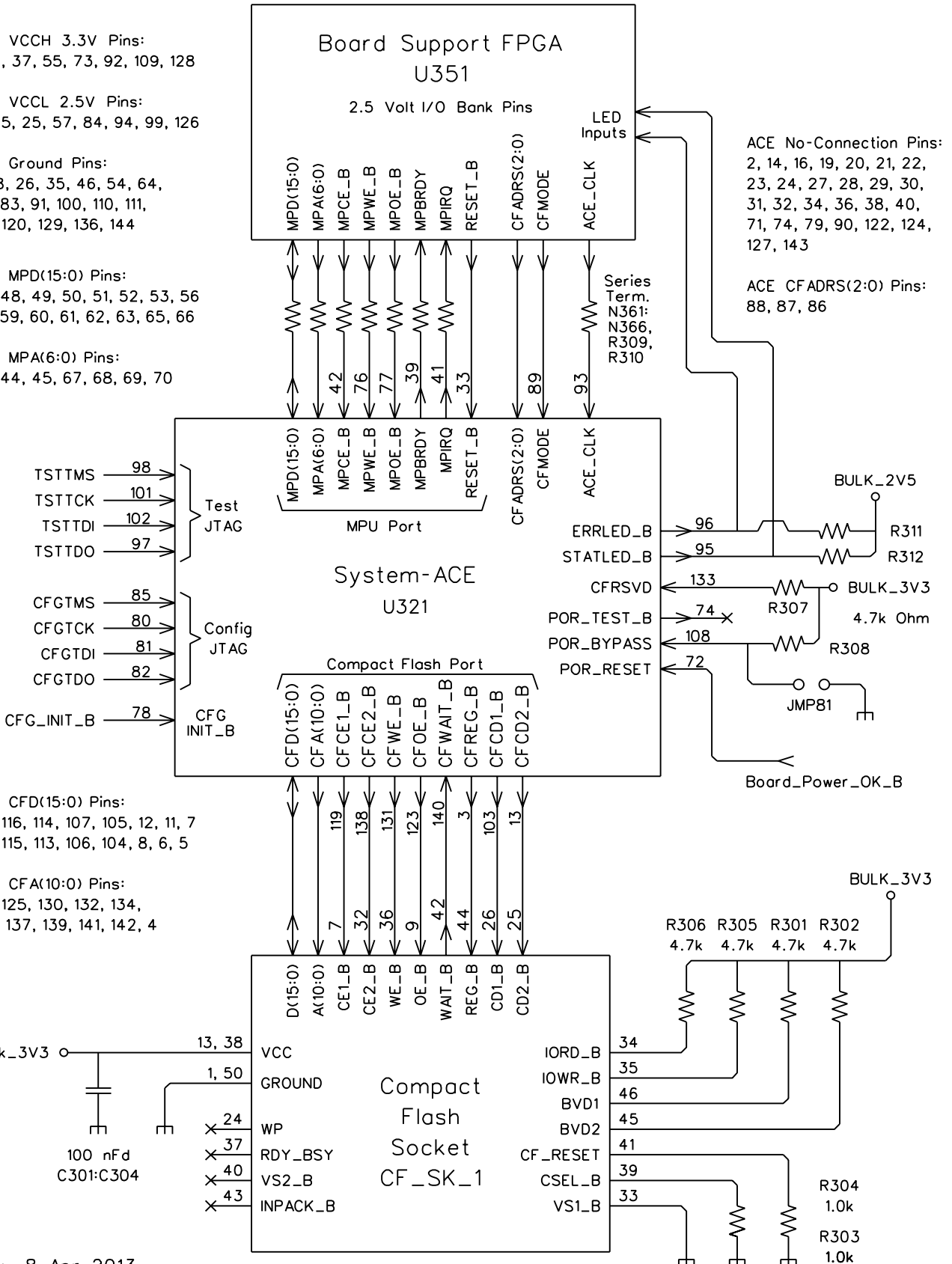
ACE VCCH 3.3V Pins:
1, 17, 37, 55, 73, 92, 109, 128

ACE VCCL 2.5V Pins:
10, 15, 25, 57, 84, 94, 99, 126

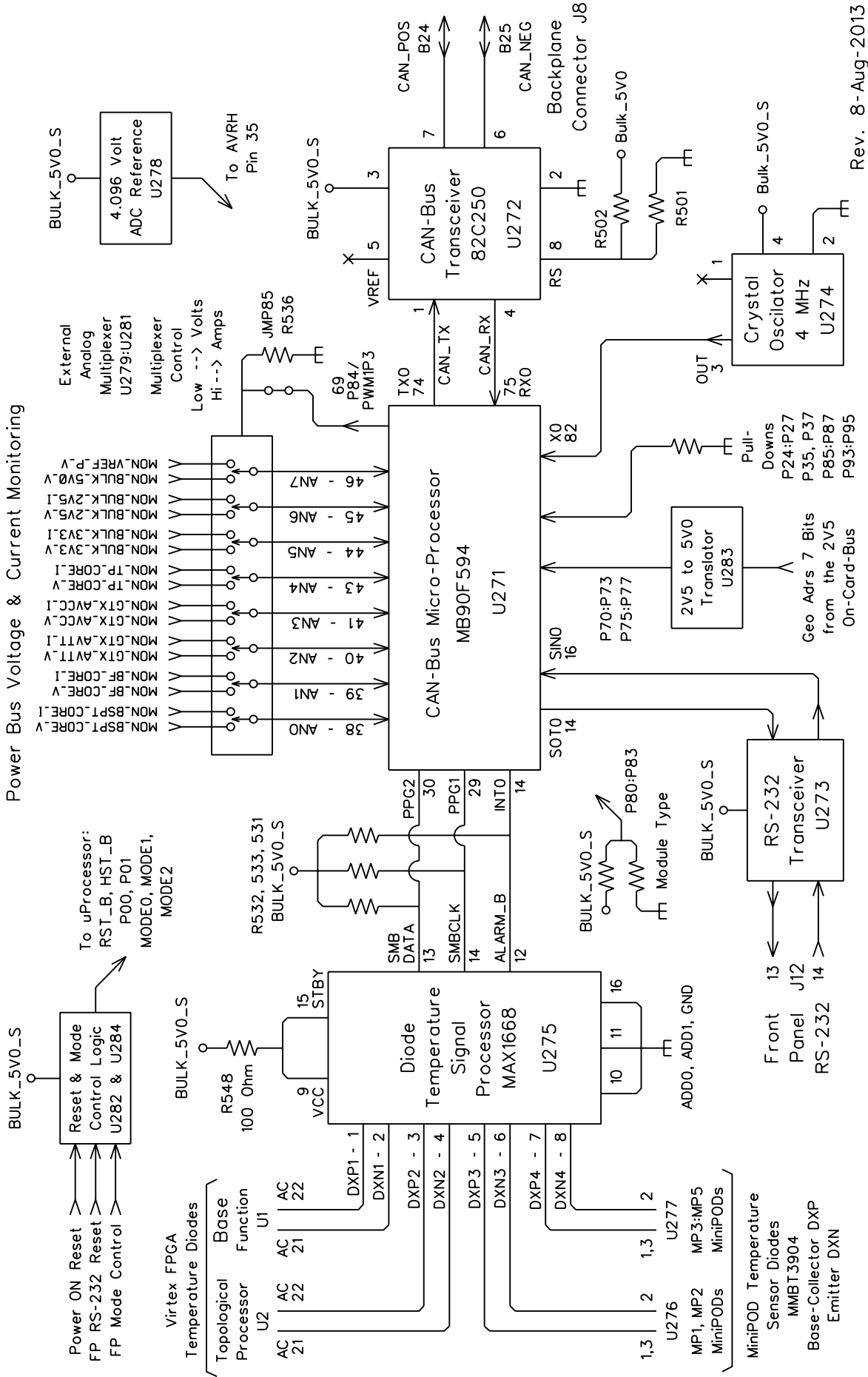
ACE Ground Pins:
9, 18, 26, 35, 46, 54, 64,
75, 83, 91, 100, 110, 111,
112, 120, 129, 136, 144

ACE MPD(15:0) Pins:
47, 48, 49, 50, 51, 52, 53, 56
58, 59, 60, 61, 62, 63, 65, 66

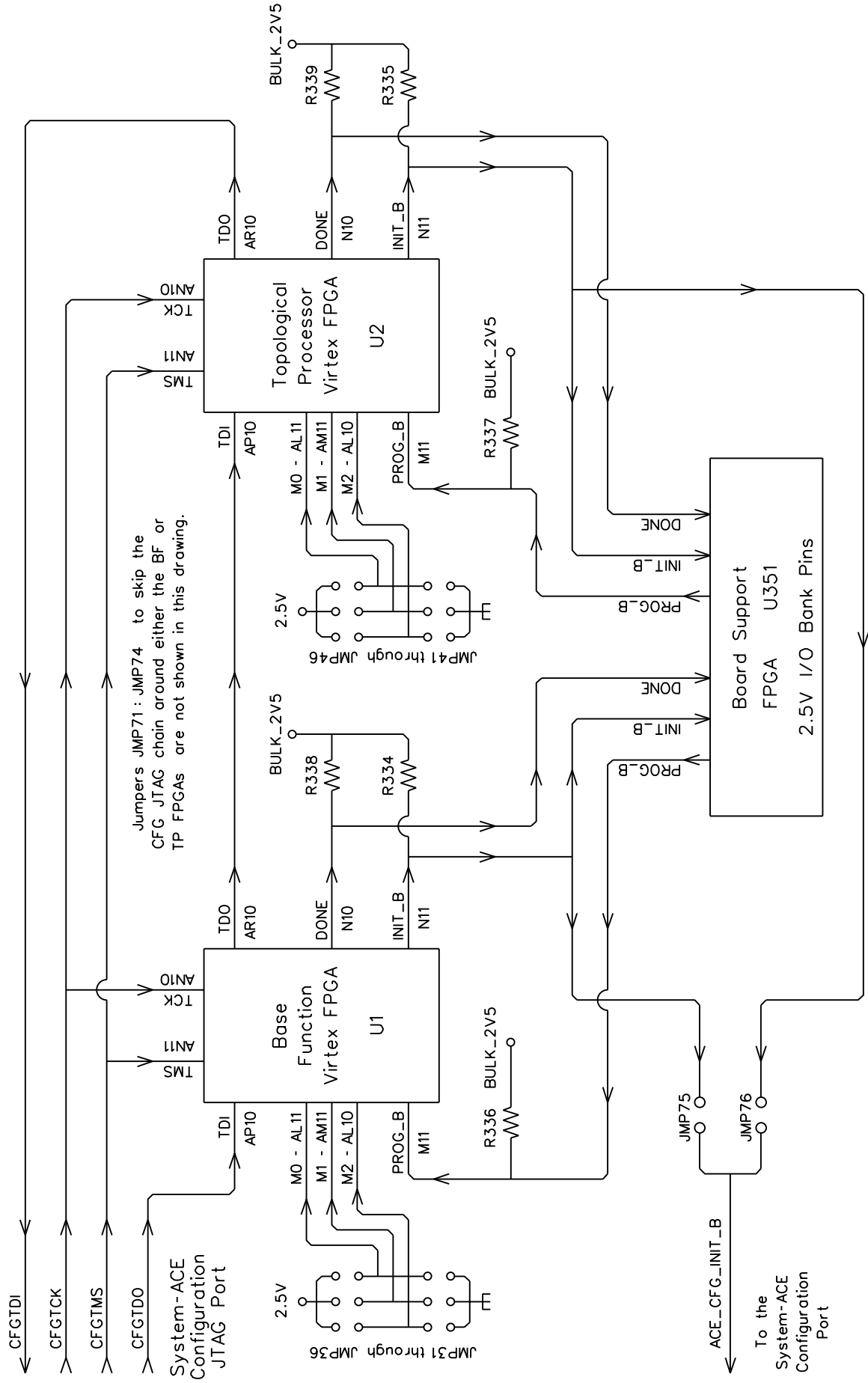
ACE MPA(6:0) Pins:
43, 44, 45, 67, 68, 69, 70



CAN-Bus Monitoring

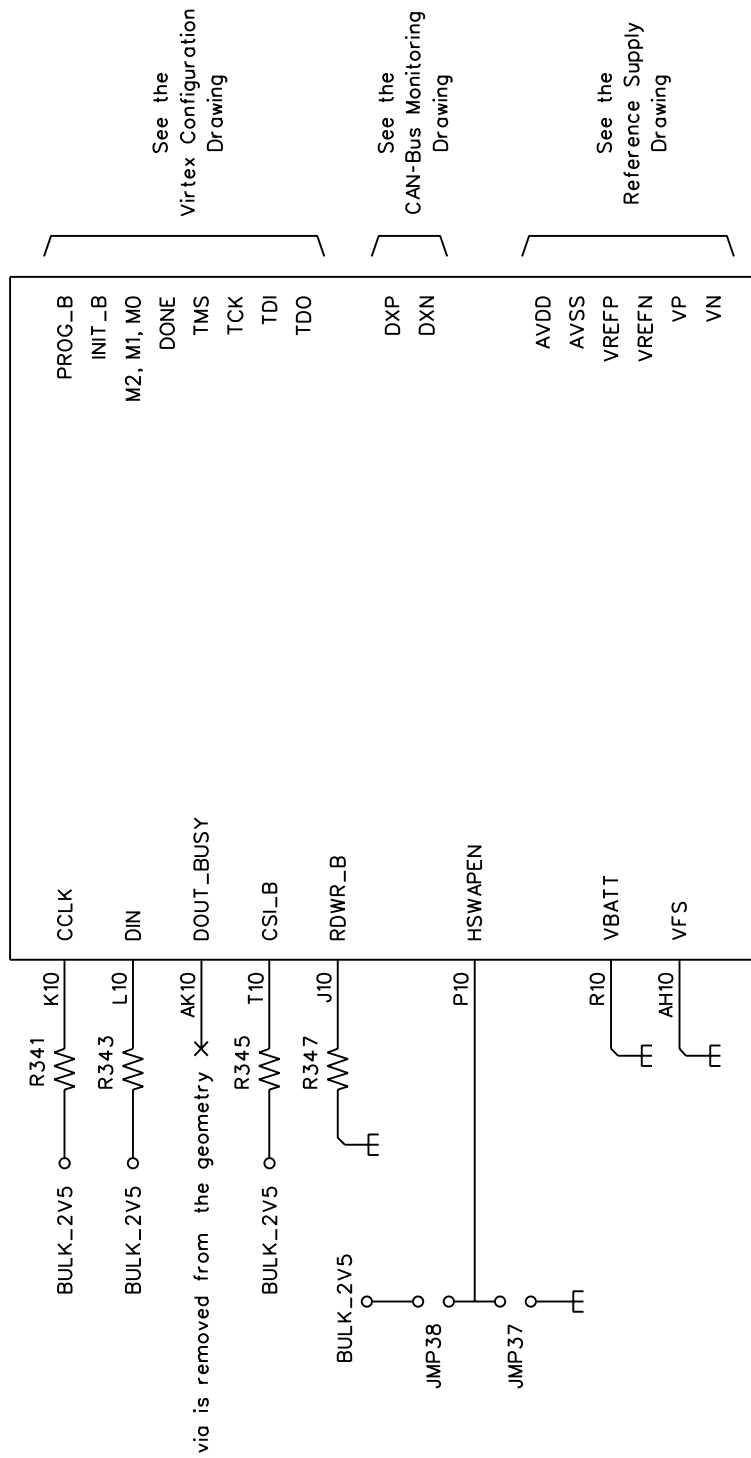


CMX Virtex FPGA Configuration

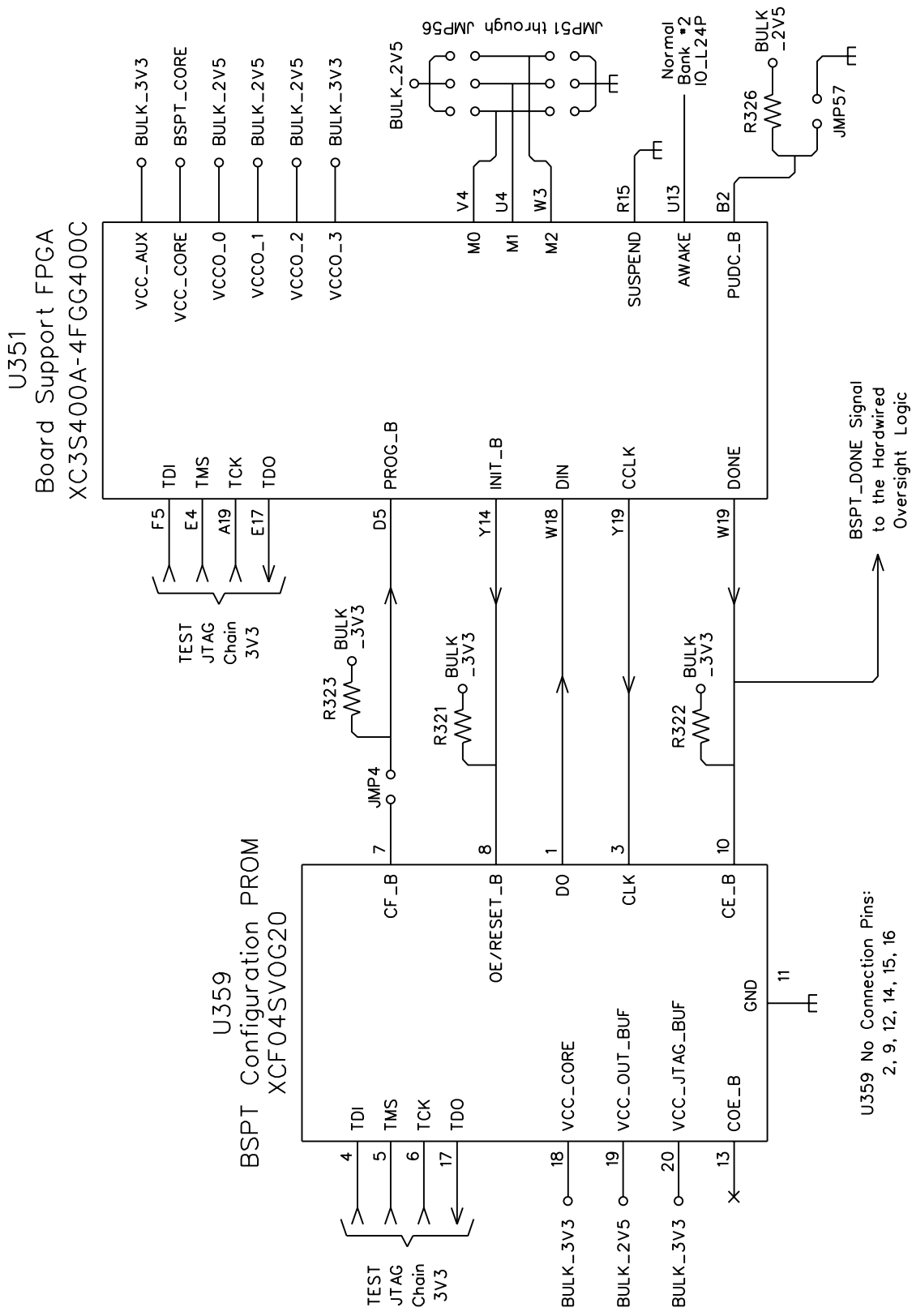


CMX Virtex FPGA Bank #0

Virtex-6 FPGA
Bank #0 Pins
U1 and U2
26 Pins on each



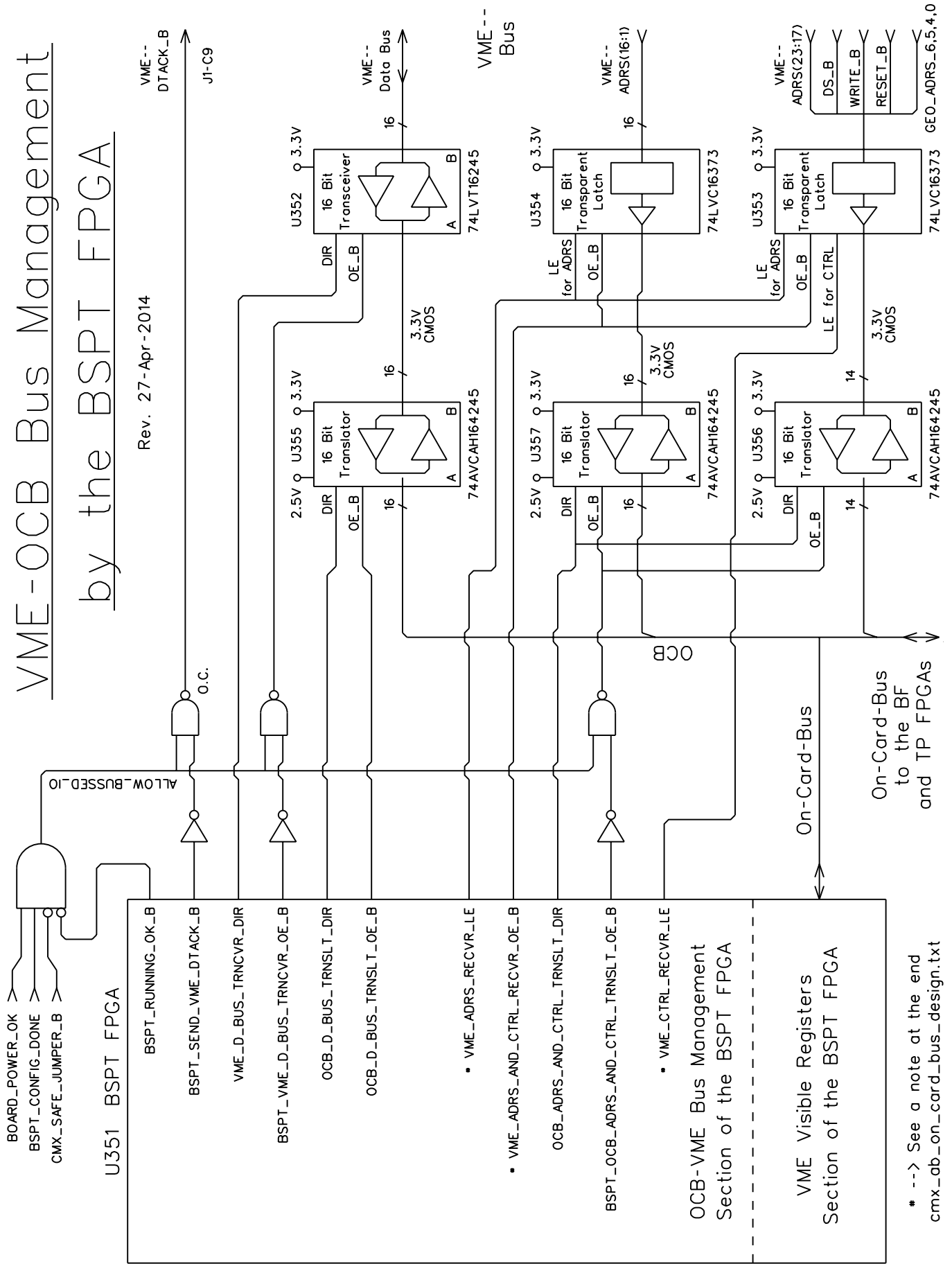
CMX Board Support FPGA Configuration



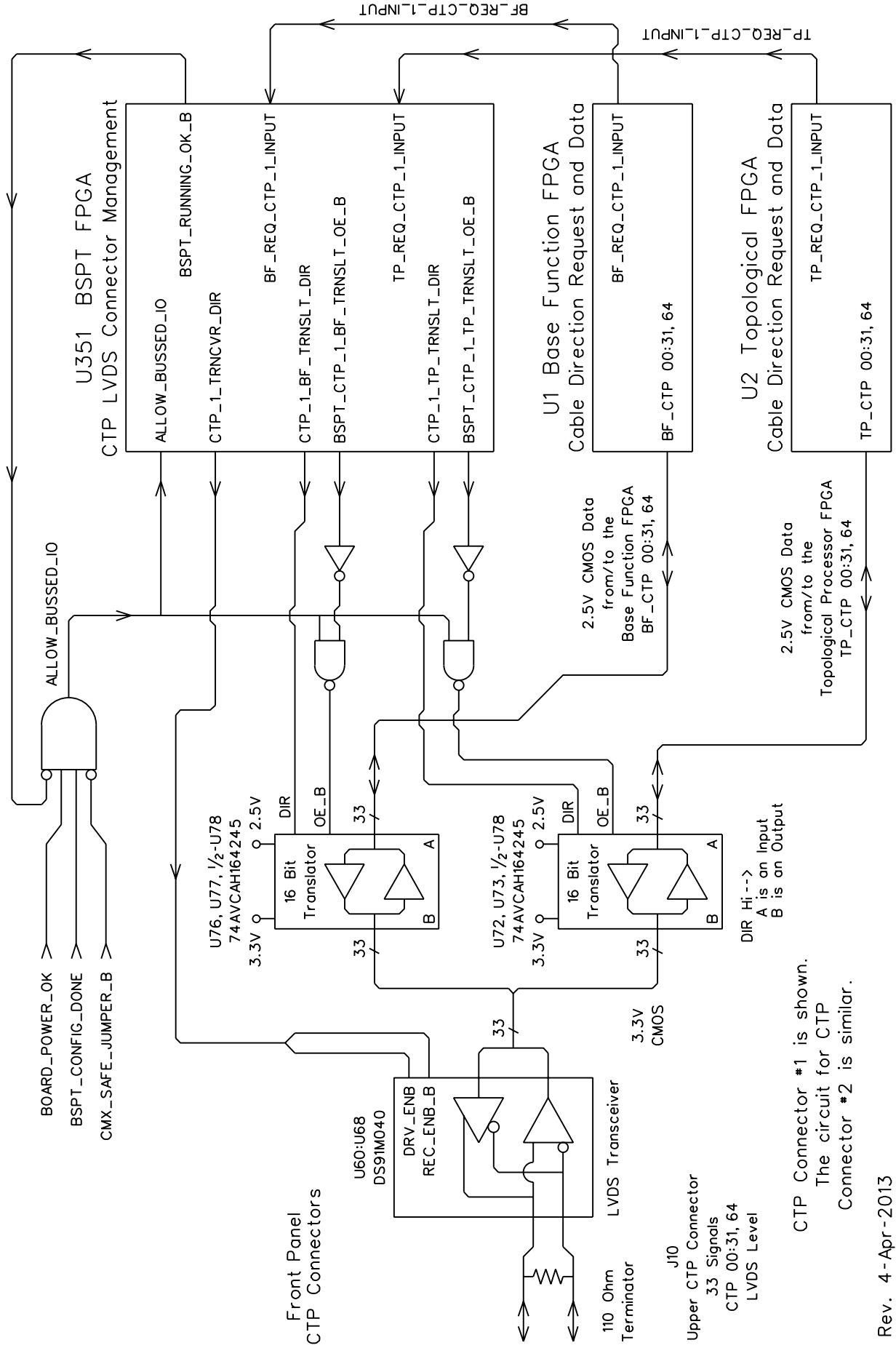
VME-OCB Bus Management

by the BSPT FPGA

Rev. 27-Apr-2014



CTP LVDS Connector Management

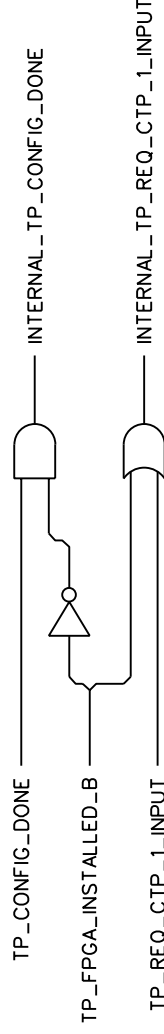


CTP Connector #1 is shown.
The circuit for CTP Connector #2 is similar.

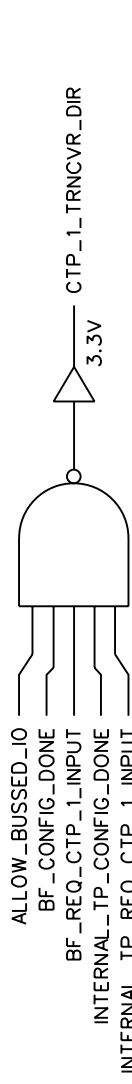
CTP Connector Management Logic in the BSPT FPGA

CTP Connector Management Rules

When the "TP Installed Jumper" says that the TP FPGA is NOT installed on this CMX card then: force the INTERNAL_TP_CONFIG_DONE signal Low force the INTERNAL_TP_REQ_CTP_1_INPUT signal Hi.

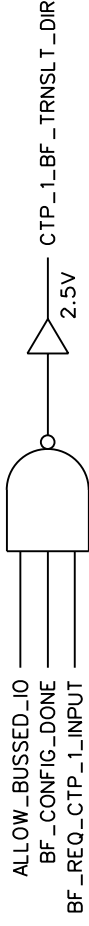


The LVDS Transceiver direction is is Output unless both the BF and TP request the direction to be Input.



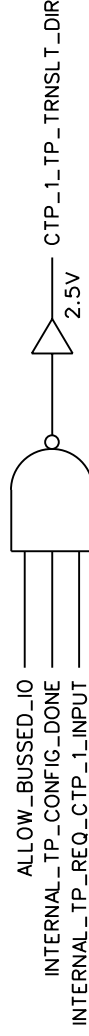
Hi --> Output to CTP
Low --> Receive from CTP

Never enable the Translator Output Drivers unless the associated FPGA (BF or TP) is Configured.

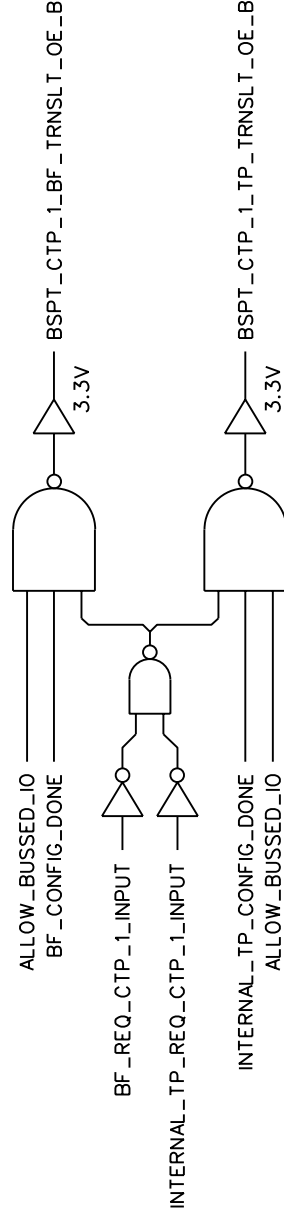


Hi --> Output to CTP
Low --> Receive from CTP

When both the BF and TP FPGAs are Configured you may Enable both the BF and the TP Translator Output Drivers except when both the BF and TP have requested the Direction to be Output. In that case disable both the BF and the TP Translator Output Drivers.



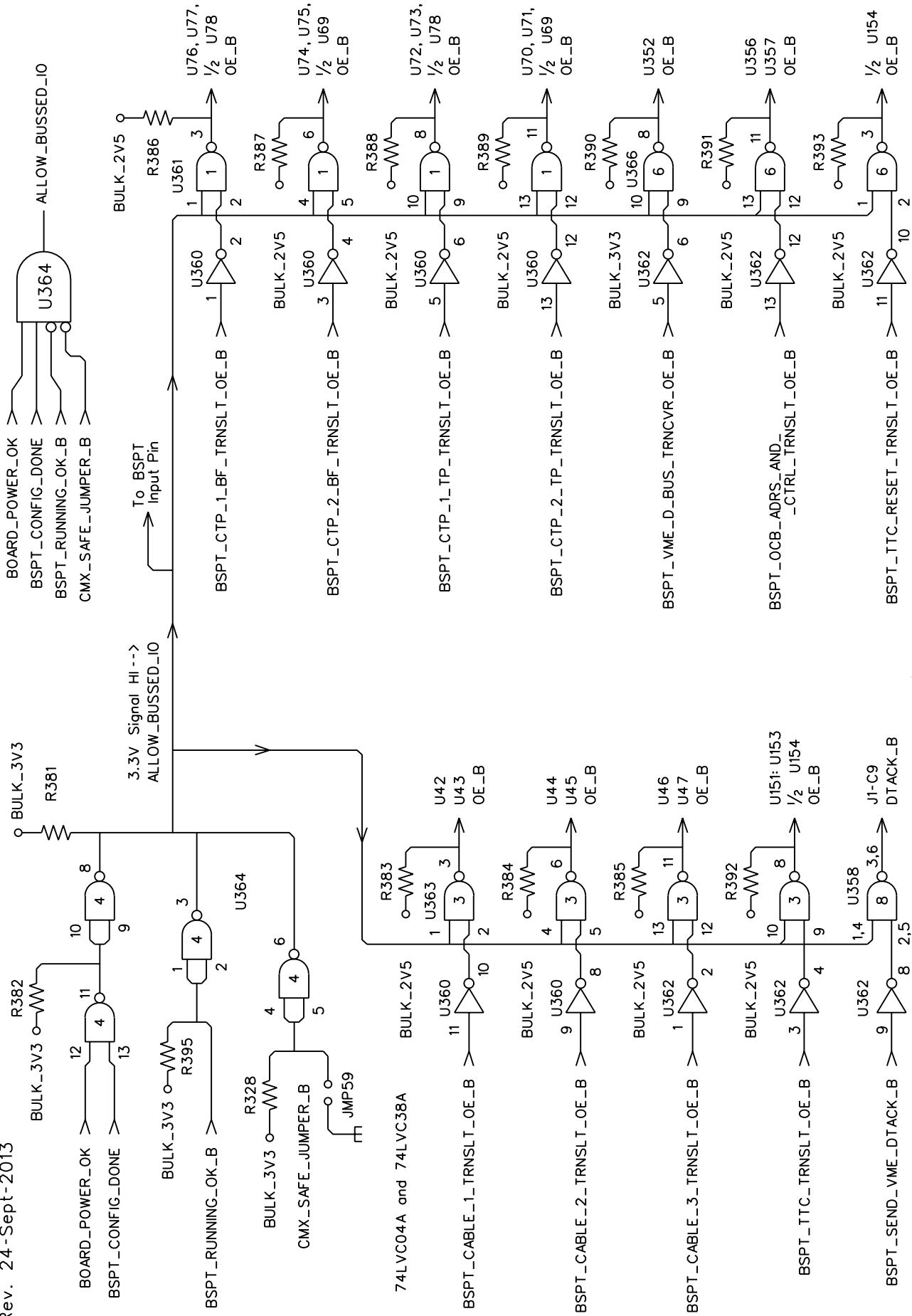
It is an Error Condition when both the BF and TP are requesting the Direction to be Output.



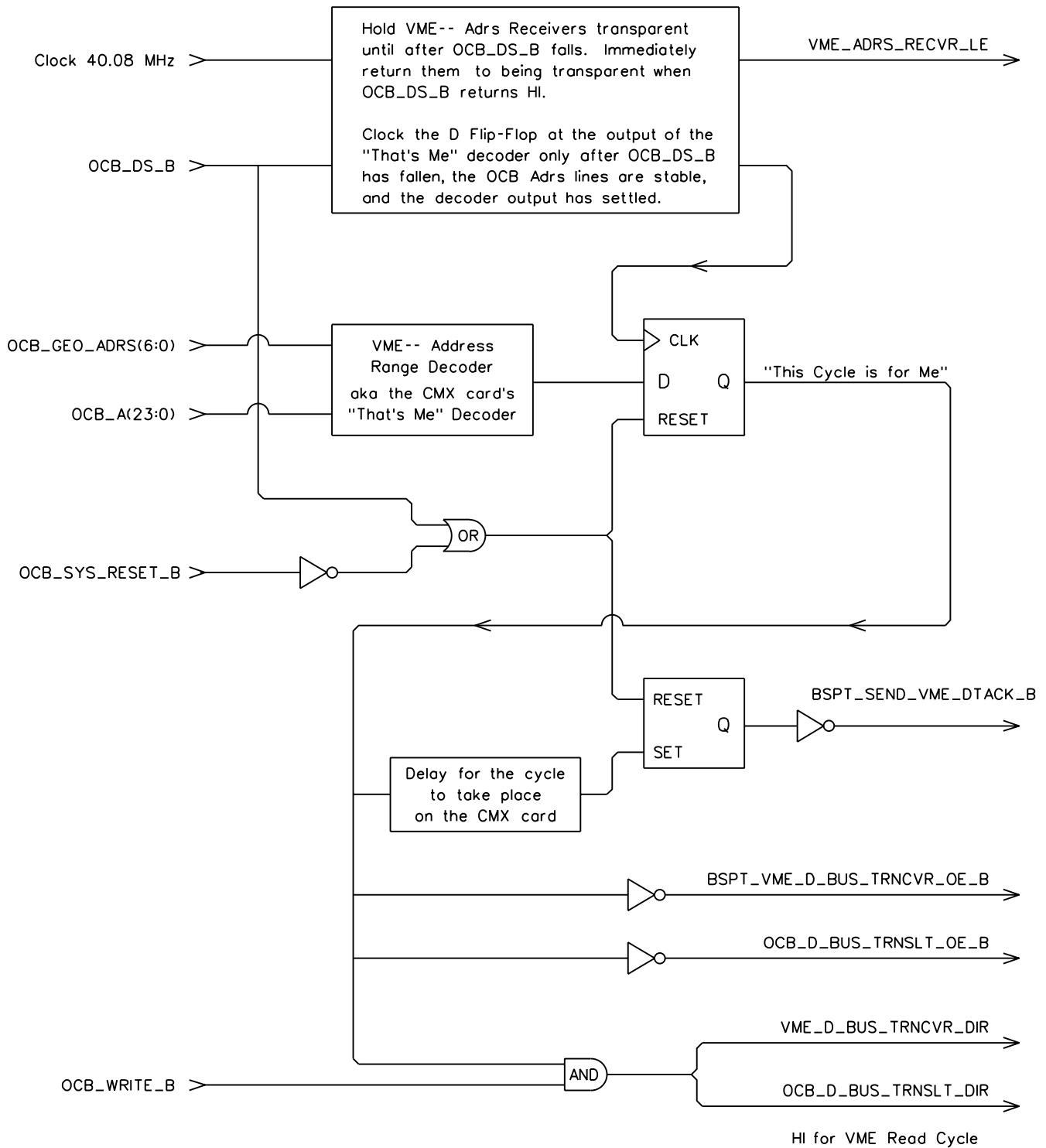
The logic for CTP Connector #1 is shown. The logic for CTP Connector #2 is similar.

Hardwired Oversight Logic - the Full System

Rev. 24-Sept-2013



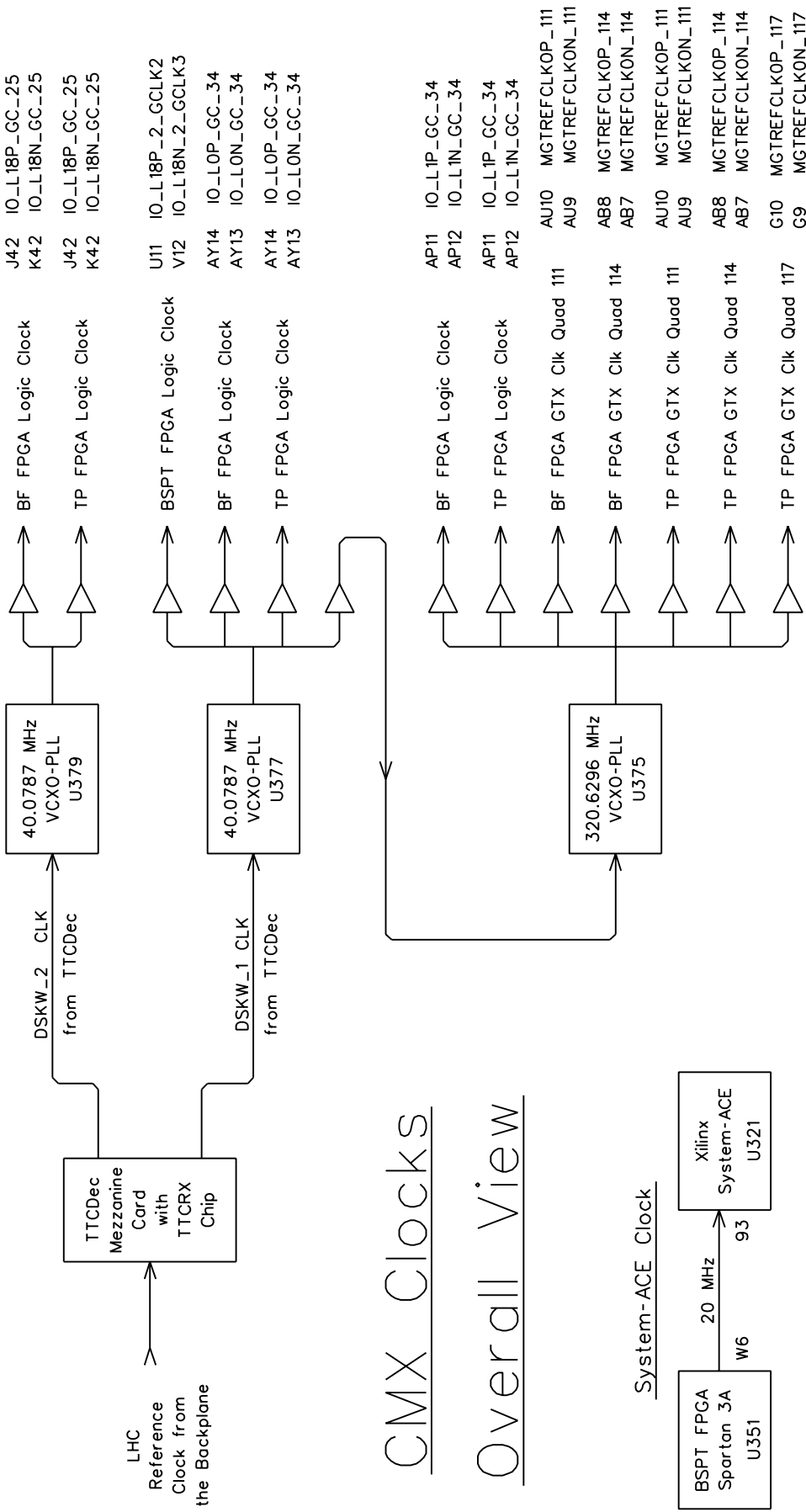
VME-OCB Management Logic in the BSPT



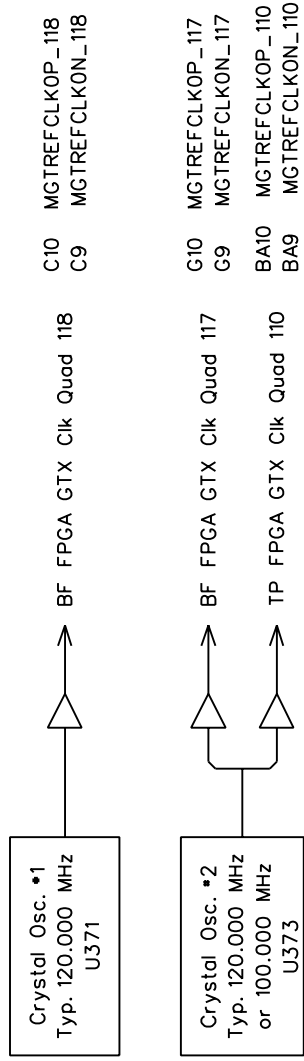
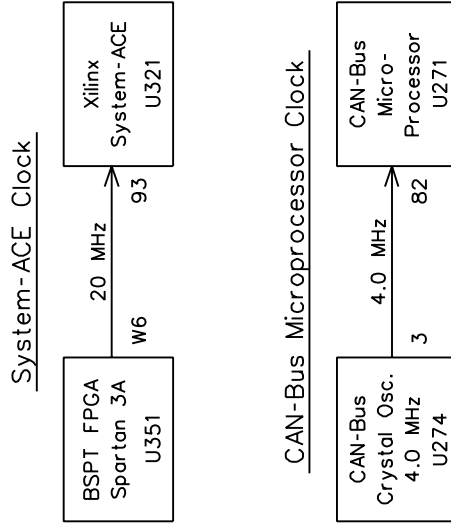
Logic in the BSPT's VME/OCB management section may set the following signals to static levels. For normal VME-- bus operation these signals do not need to switch levels:

- VME_ADRS_AND_CTRL_RECVR_OE_B always Low
- OCB_ADRS_AND_CTRL_TRNSLT_DIR always Low
- VME_CTRL_RECVR_LE always Hi
- BSPT_OCB_ADRS_AND_CTRL_TRNSLT_OE_B once the Virtex FPGAs are Configured then always Low

Source Fan-Out FPGA Logic Clocks & GTX Clocks



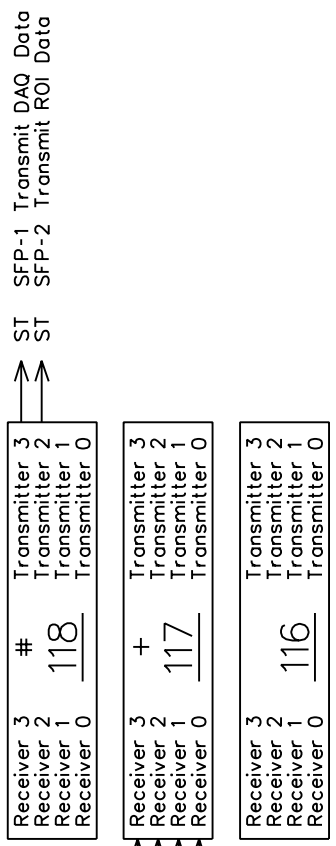
CMX Clocks
Overall View



GTX Transceivers - Base Function FPGA

QUAD

Base Function
Readout to
DAQ and ROI



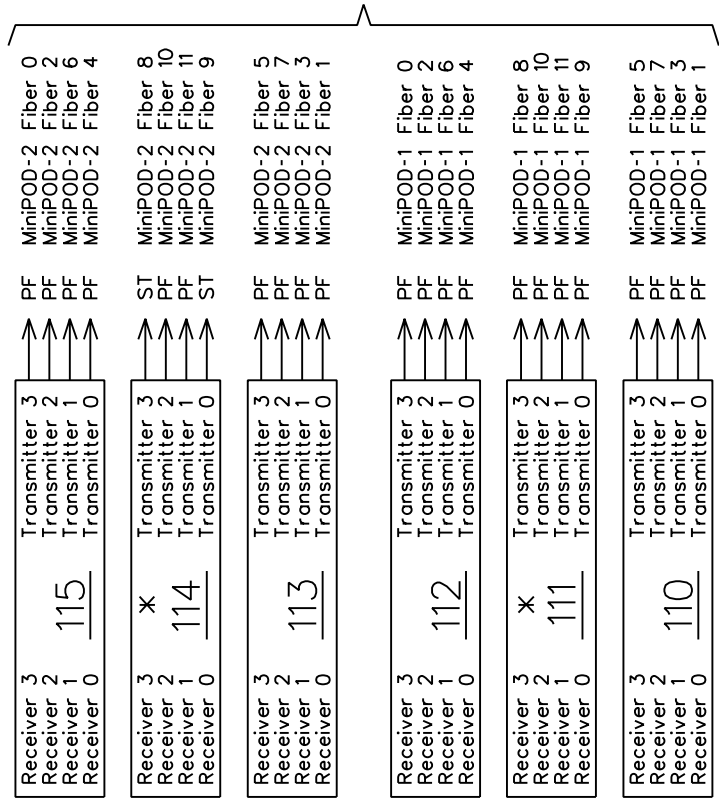
For Possible Use with S-Link Control Signals

- SFP-1 Received Data
- SFP-2 Received Data
- SFP-3 Received Data
- SFP-4 Received Data

Base Function FPGA

GTX Reference Clock Notes:

- # → This Quad receives the Crystal Oscillator #1 reference clock which is typically 120.000 MHz.
- + → This Quad receives the Crystal Oscillator #2 reference clock which is typically 120.000 MHz or 100.000 MHz
- * → These Quads receive the LHC locked 320.6296 MHz reference clock.

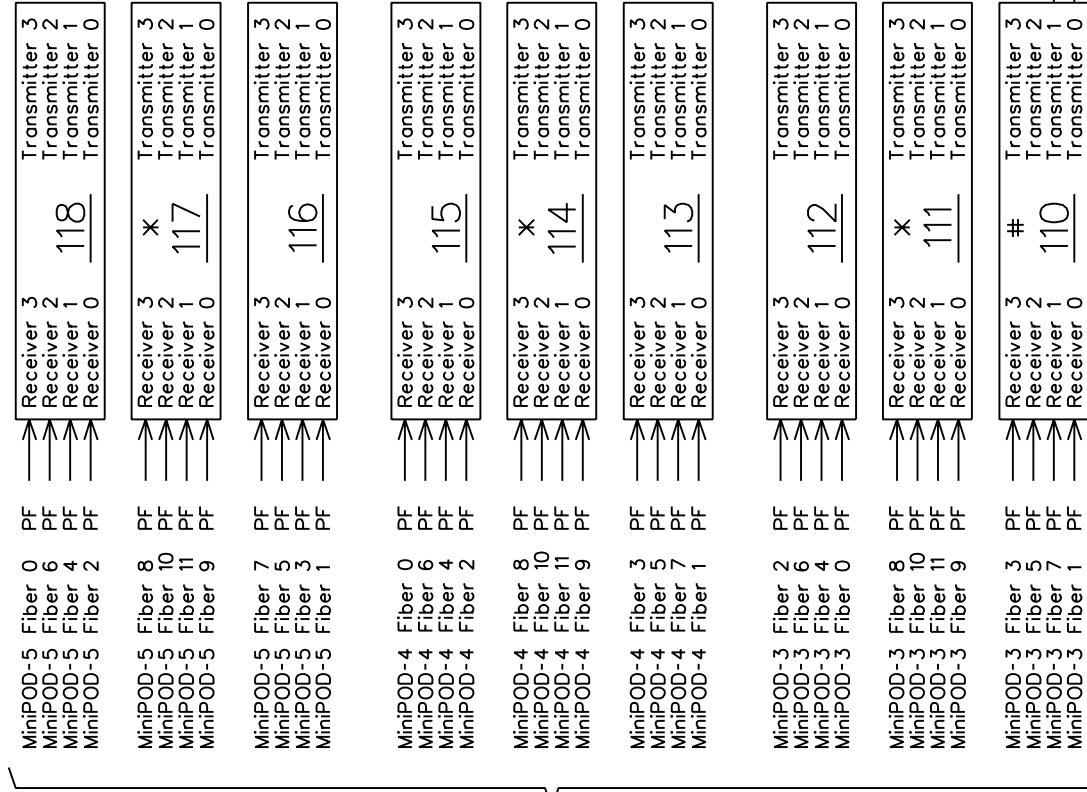


Transmit
Base Function
Data to
L1Topo

PF → Polarity Flip
ST → Straight Through

GTX Transceivers - Topological FPGA

QUAD



Input Data
When the
CMX Acts as
an L1Topo

Topological Processor FPGA
GTX Reference Clock Notes:

* → These Quads receive the LHC locked 320.6296 MHz reference clock.

→ This Quad receives the Crystal Oscillator #2 reference clock which is typically 120.000 MHz or 100.000 MHz

PF → Polarity Flip

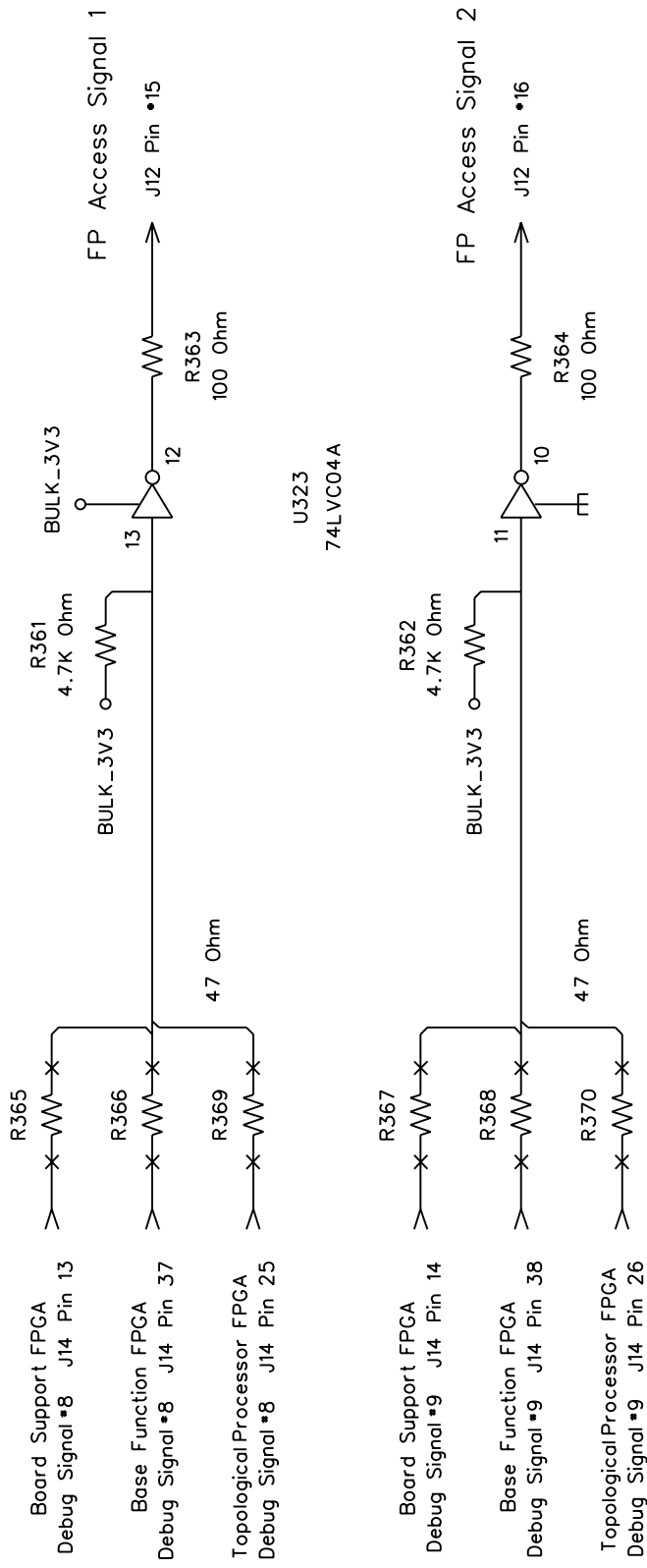
ST → Straight Through

Topological
Processor FPGA
Readout to
DAQ and ROI
via G-Link or
Possibly S-Link

SFP-3 Transmit DAQ Data
SFP-4 Transmit ROI Data

PF PF

Two Access Signals on the Front Panel

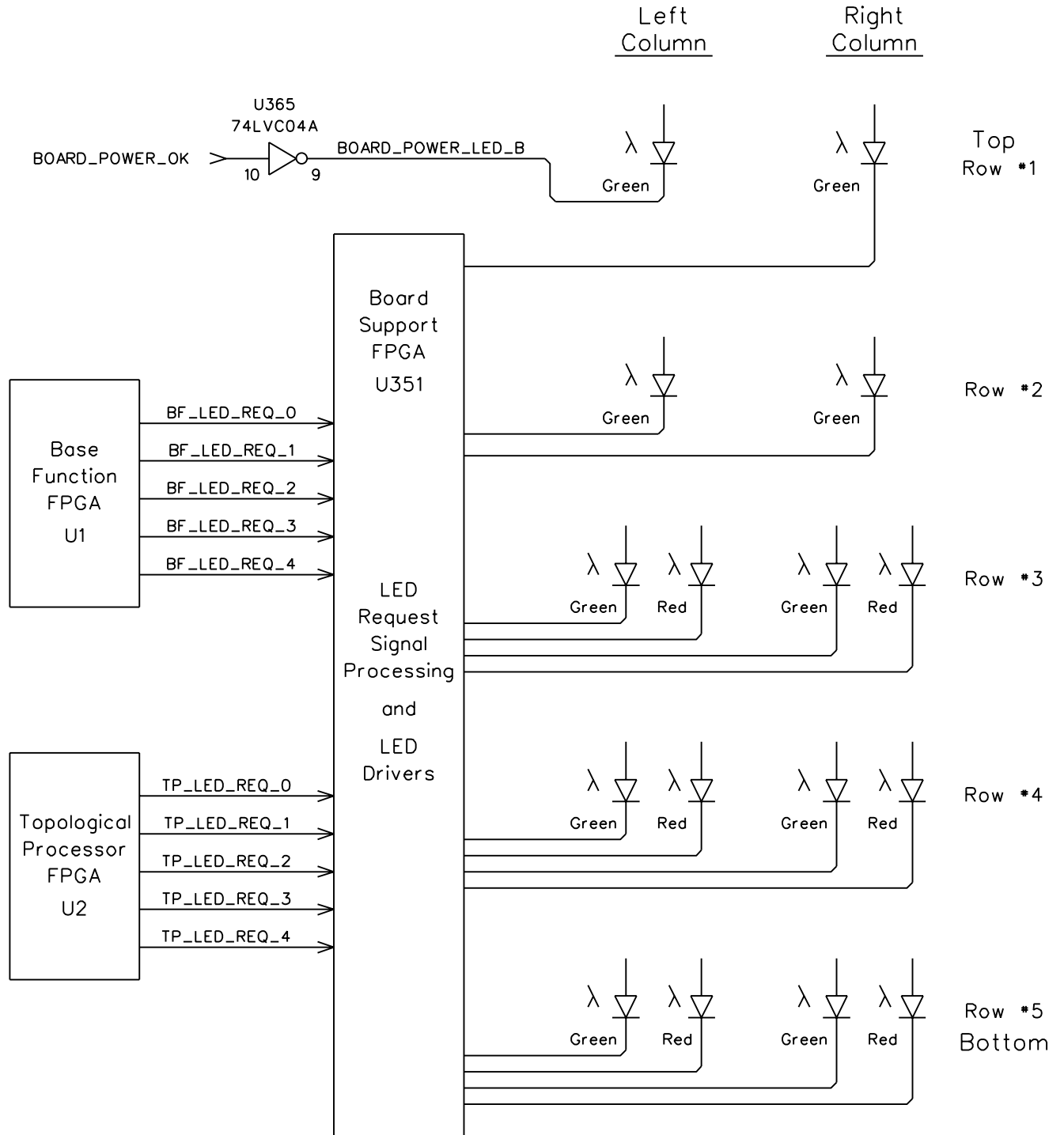


Front panel connector J12 pins 15 and 16 provide access to two buffered signals from either the: Board Support FPGA, the Base Function FPGA, or the Topological Processor FPGA.

These two front panel access signals can be used e.g.: clock monitoring, S-Link Busy, scope or logic analyzer trigger.

All J12 odd numbered pins 1 through 9 are grounds. The 74LVC04A buffer can provide 20 mA max output. The 74LVC04A has a logic Hi input minimum of 2.0 volts. The Xilinx 2.5V CMOS output logic Hi is a minimum of 2.1 volts. The Xilinx I/O pin clamp diode can handle 10 mA max.

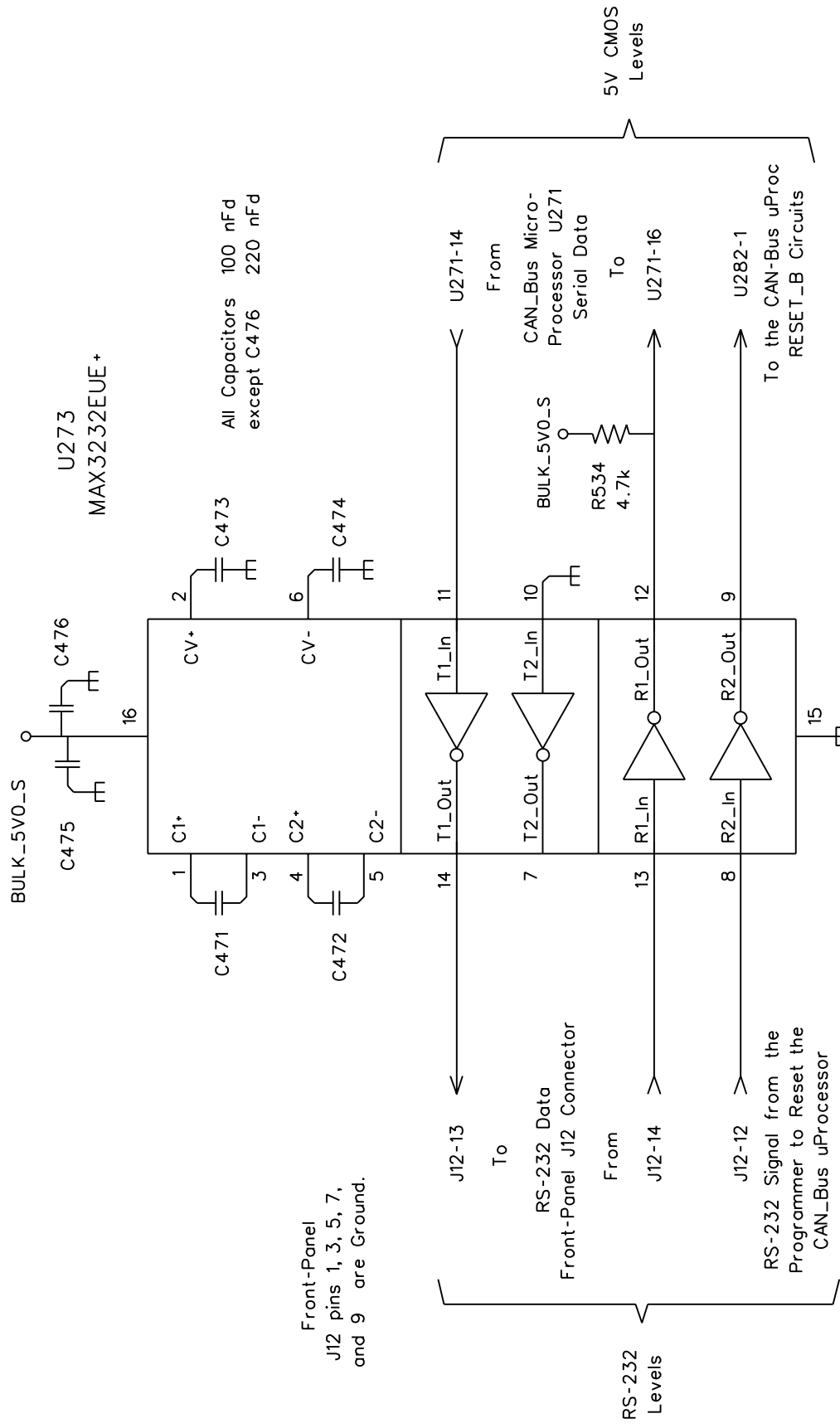
Front Panel Dual-LEDs



All LED Anodes are connected to BULK_3V3 through 680 Ohm Resistors.

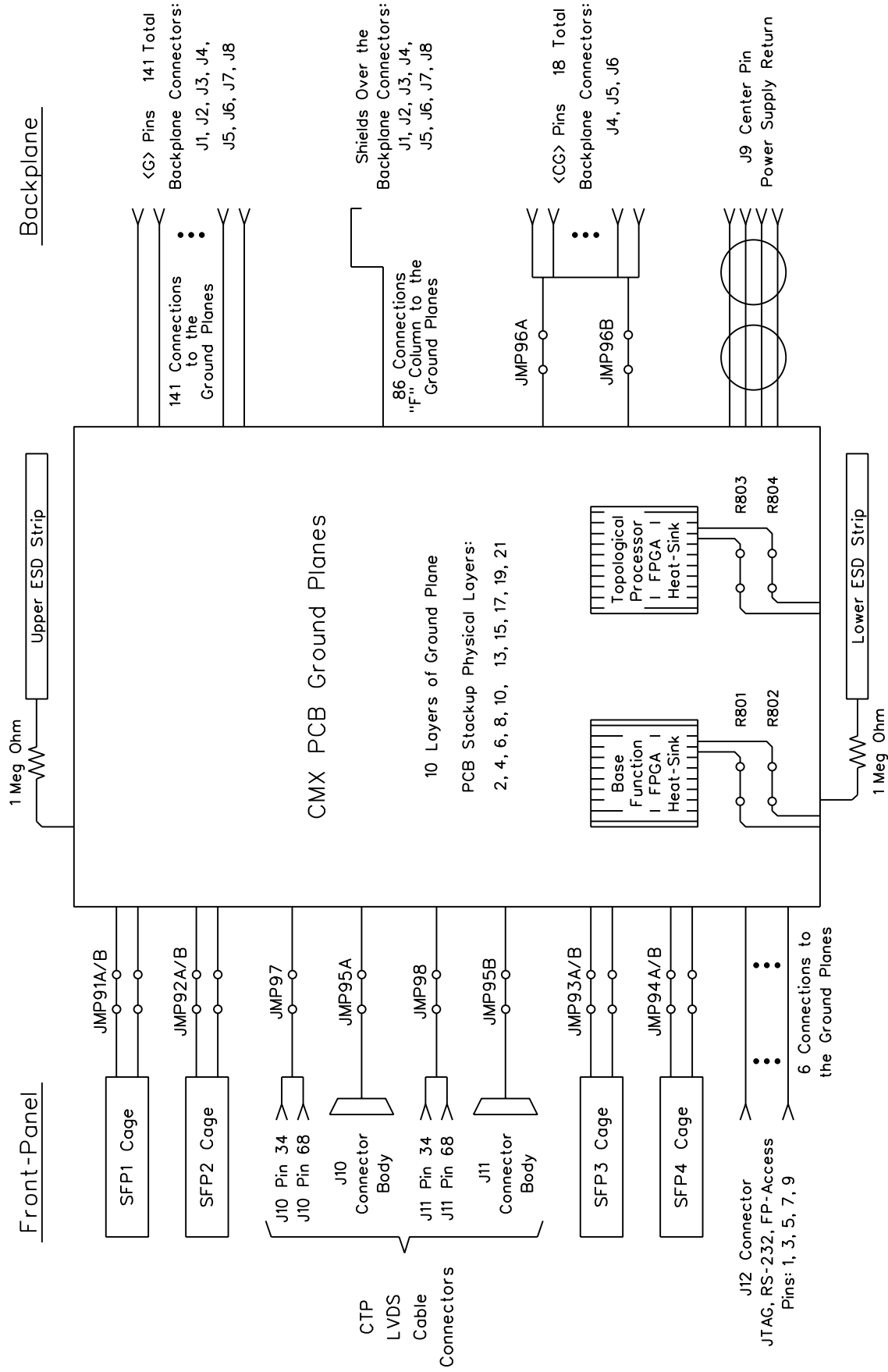
Rev. 1-July-2013

RS-232 Interface to the CAN-Bus Micro-Controller



Both the transmitters and receivers are level inverting.
The receiver inputs have internal 5k Ohm pull-down resistors.

Ground Connections on the CMX Card



The front-panel, stiffener bars, and guide pin receptacle are electrically connected to the bodies of connectors J10 and J11. During assembly the SFP Cages may be electrically connected to or insulated from the front-panel.

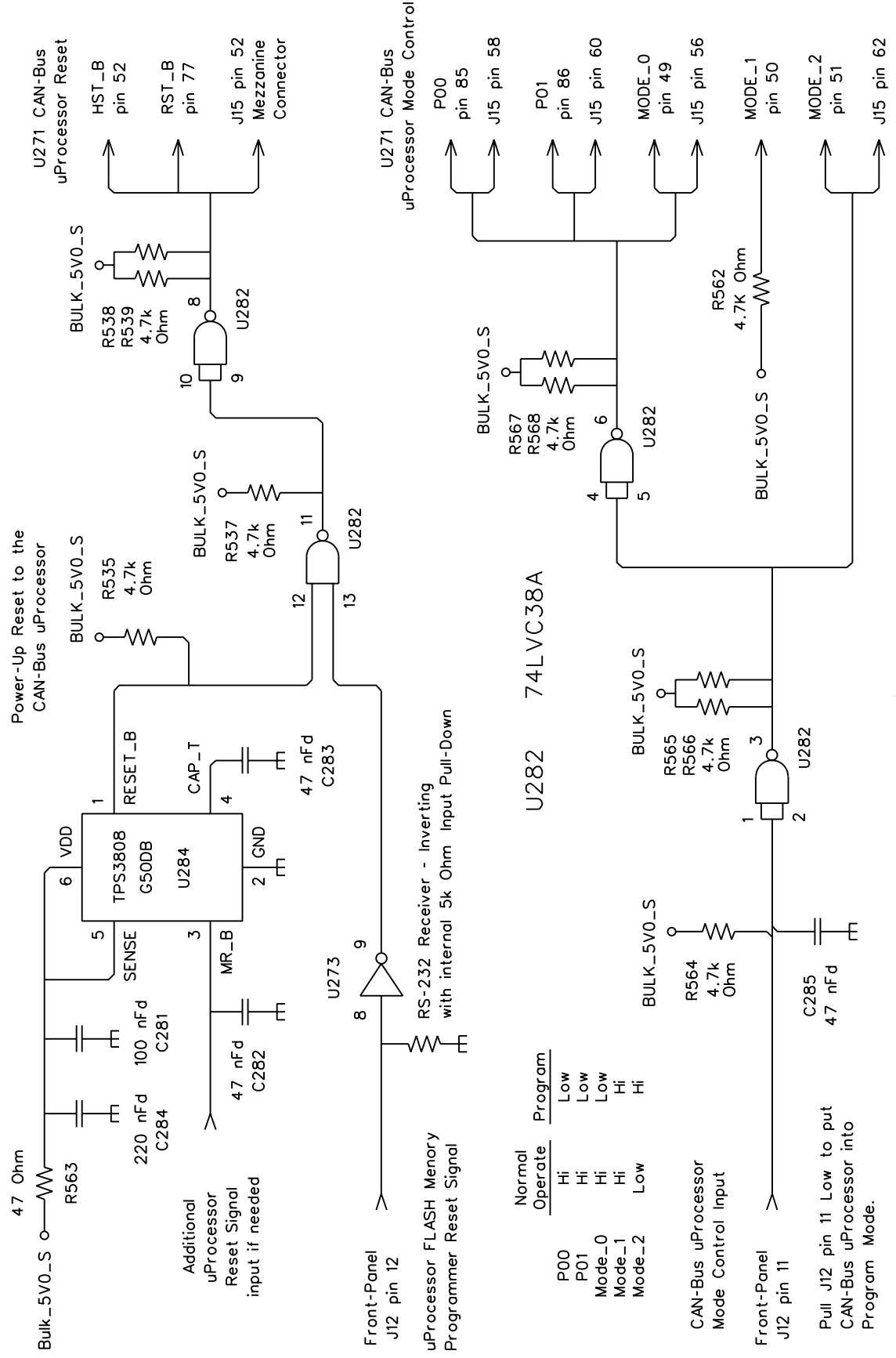
All jumpers shown in this drawing may be: open circuits, Zero-Ohm jumpers, or appropriate value 0805 resistors as required to control ground loops.

Rev. 14-Aug-2013

CAN-Bus uProcessor Reset and Mode Signals

CAN-Bus uProcessor Startup Supervisor

Rev. 3-Aug-2013



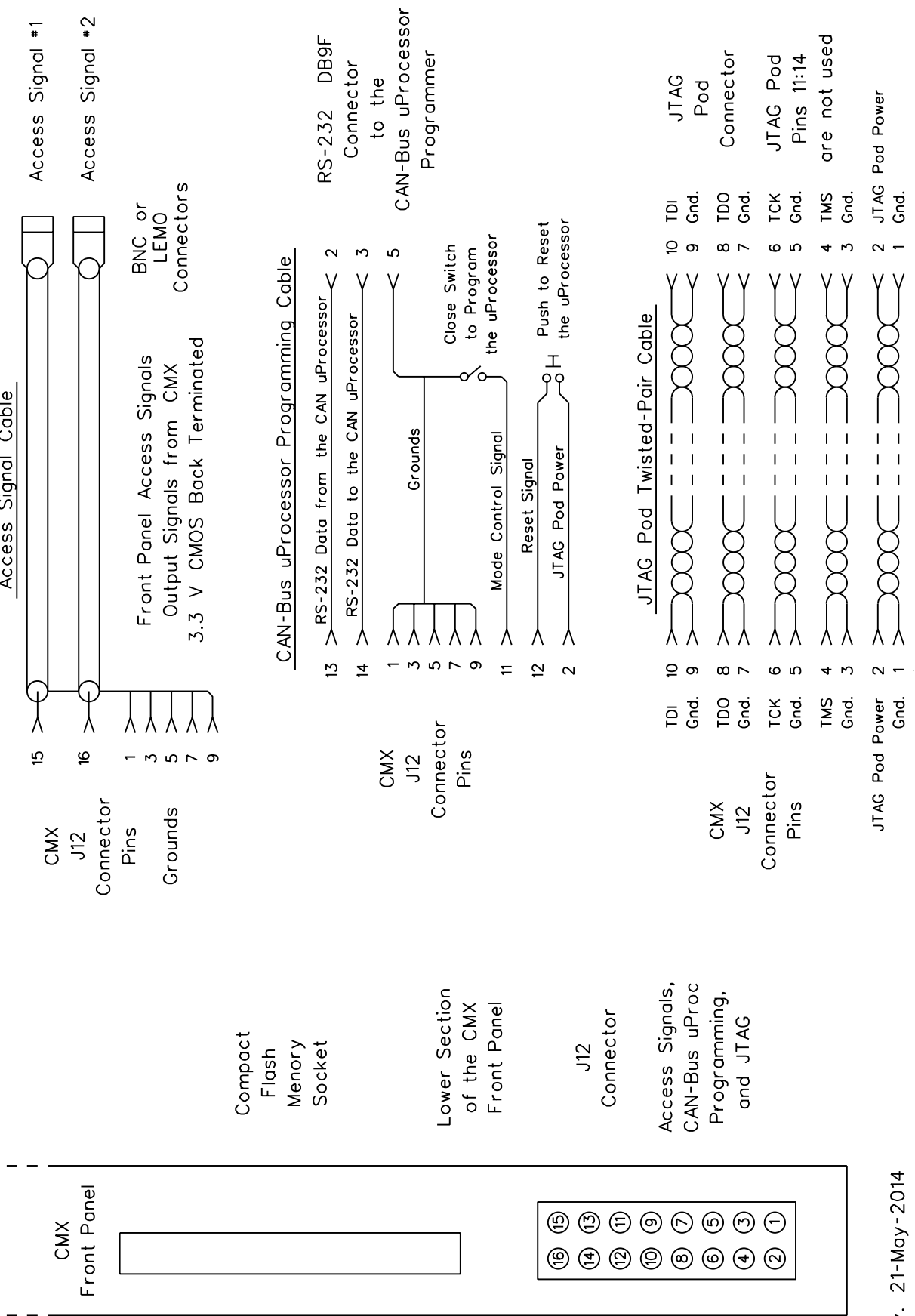
Normal Operate	Program
P00	Low
P01	Low
Mode_0	Low
Mode_1	Hi
Mode_2	Hi

CAN-Bus uProcessor Mode Control Input

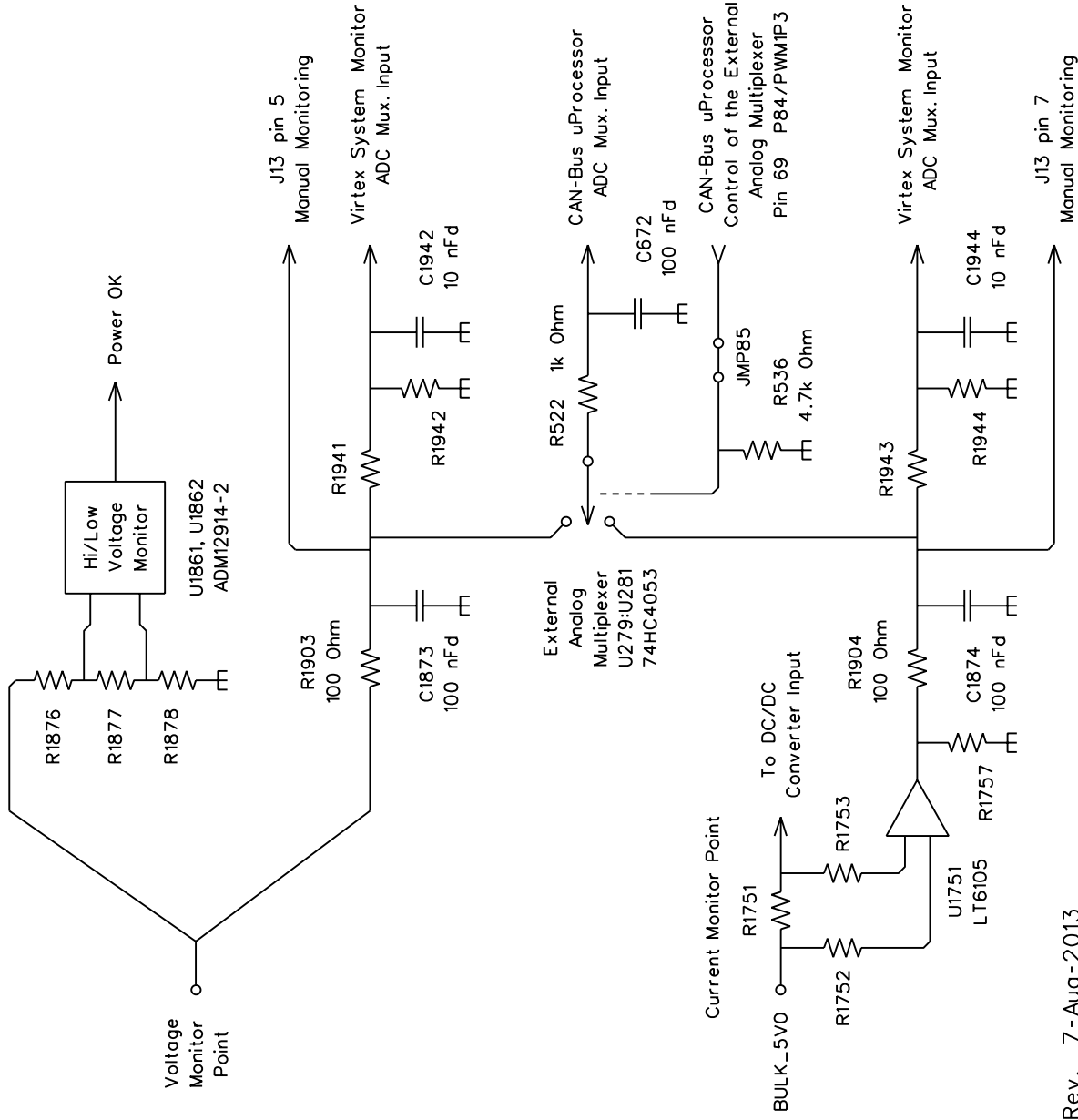
Front-Panel J12 pin 11

Pull J12 pin 11 Low to put CAN-Bus uProcessor into Program Mode.

Front Panel J12 Connector and Cables



Voltage and Current Monitoring Analog Circuits



Notes:

The reference designators and pin numbers shown are for the Base Function FPGA Core power supply.

The Voltage and Current Monitoring of the other 6 power supplies is similar.

ADC inputs to the CAN-Bus uProcessor are 4.096 Volts full-scale.

The ADC inputs to the Virtex System Monitor are 1.0 Volts full-scale. R1941 through R1944 must scale the monitored signal to fit within this 1.0V ADC input range.

R1751, R1752, R1753, and R1757 together set the calibration of the current monitoring signal.

R1752 must equal R1753. Monitor signal voltage equals Amps into the DC/DC Converter times R1751 times R1757 divided by R1752.

LT6105 maximum output current is 1 mA.

R1876, R1877, and R1878 together set the Hi and Low thresholds of the BF_CORE component of the overall CMX Power OK signal.

The ADM12914-2 Hi/Low Supervisor comparators have an internal 0.500 Volt reference.

With jumper JMP85 installed the external Analog Multiplexer is controlled by the signal from the CAN-Bus uProcessor.

With jumper JMP85 removed the External Analog Multiplexer defaults to the Voltage Monitor signals