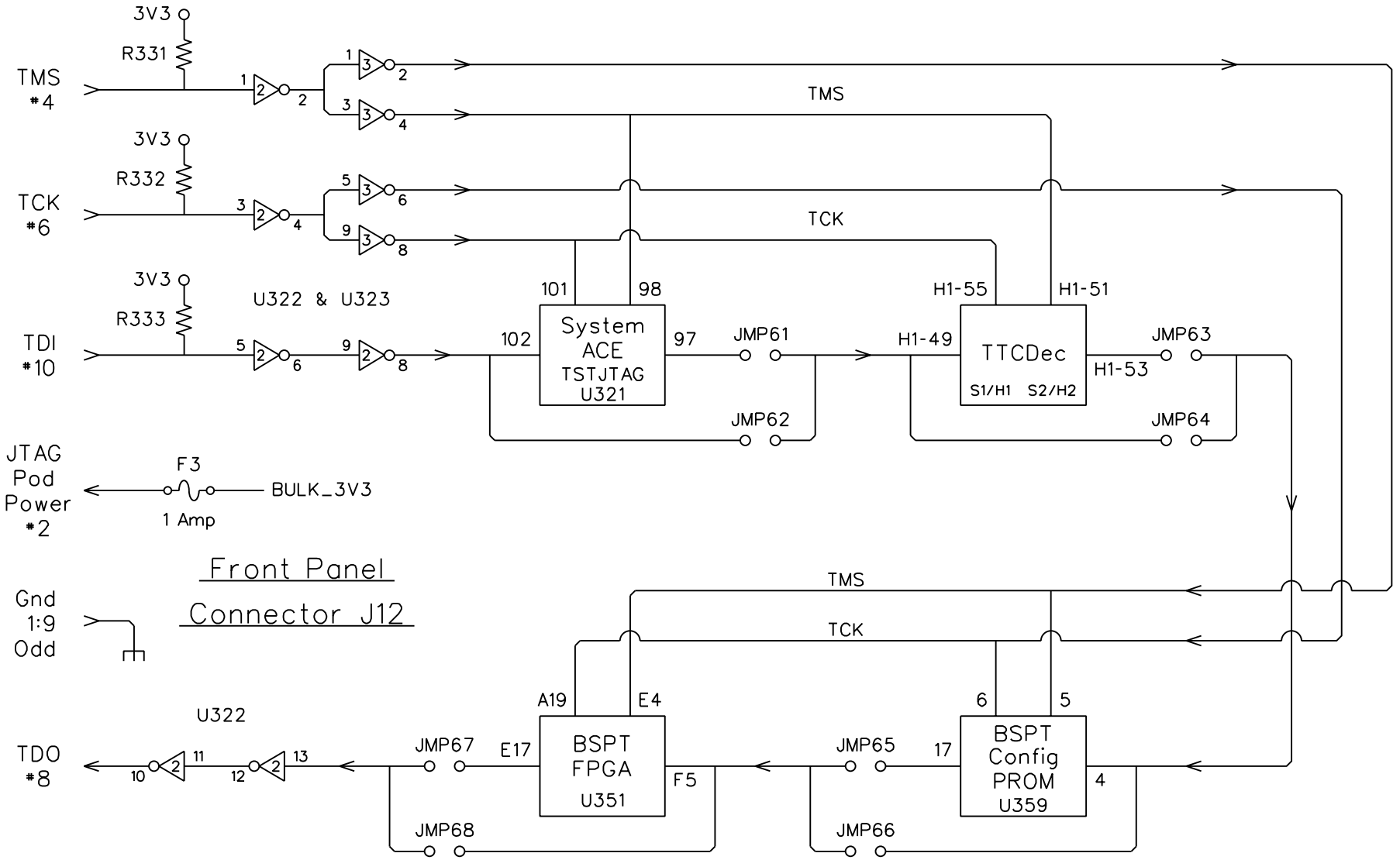
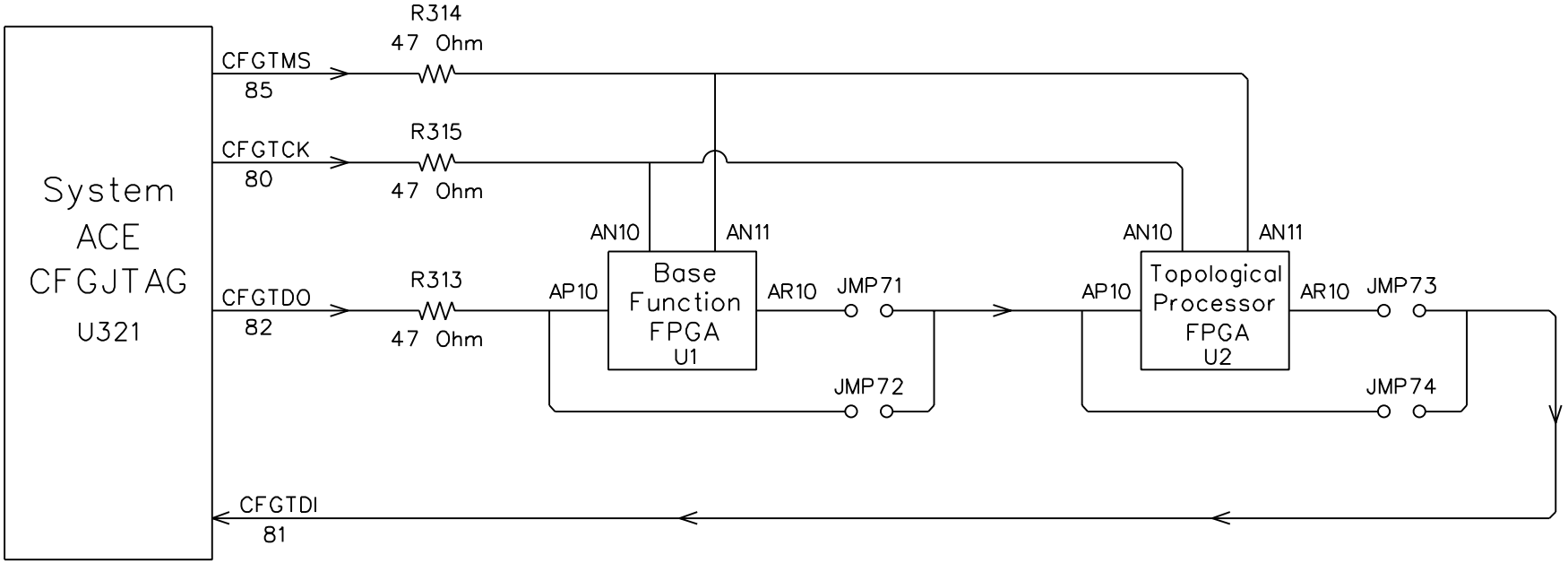
CMX TEST JTAG Chain



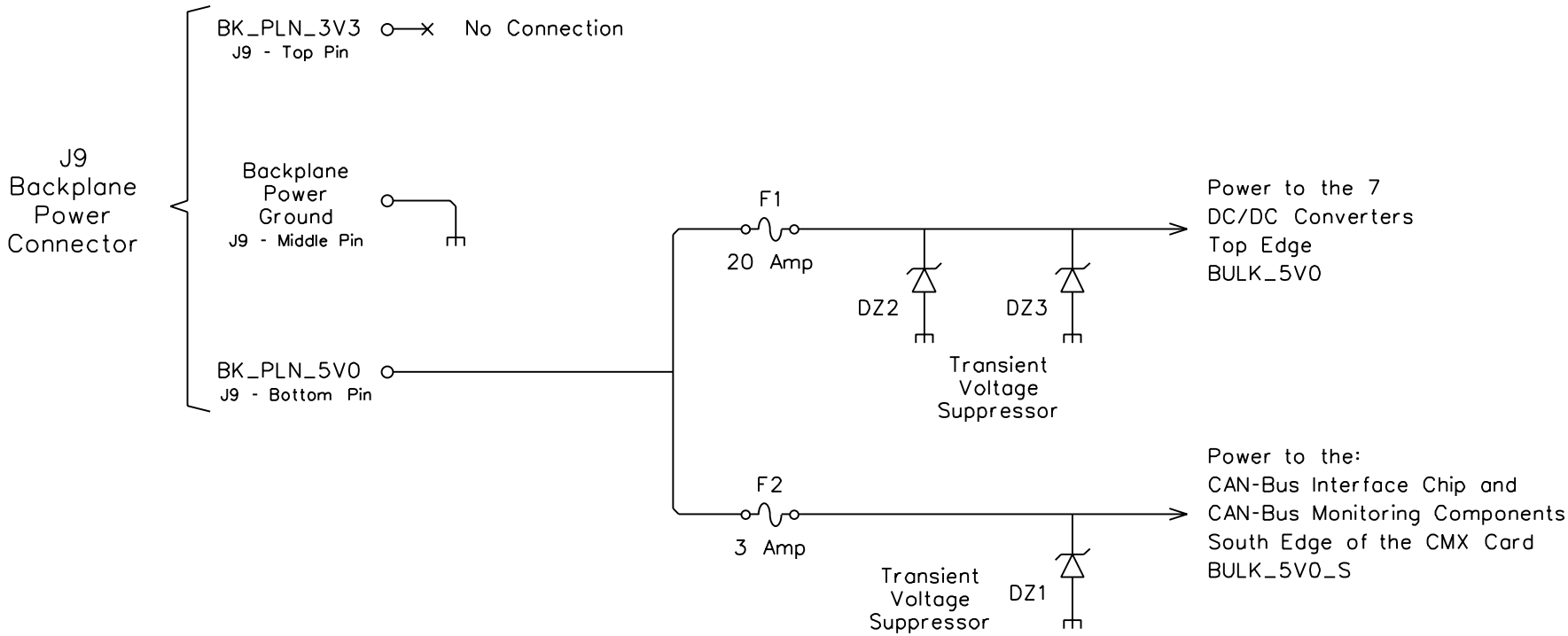
Rev. 3-Jan-2014

CMX CONFIGURATION JTAG Chain



Rev. 14-May-2013

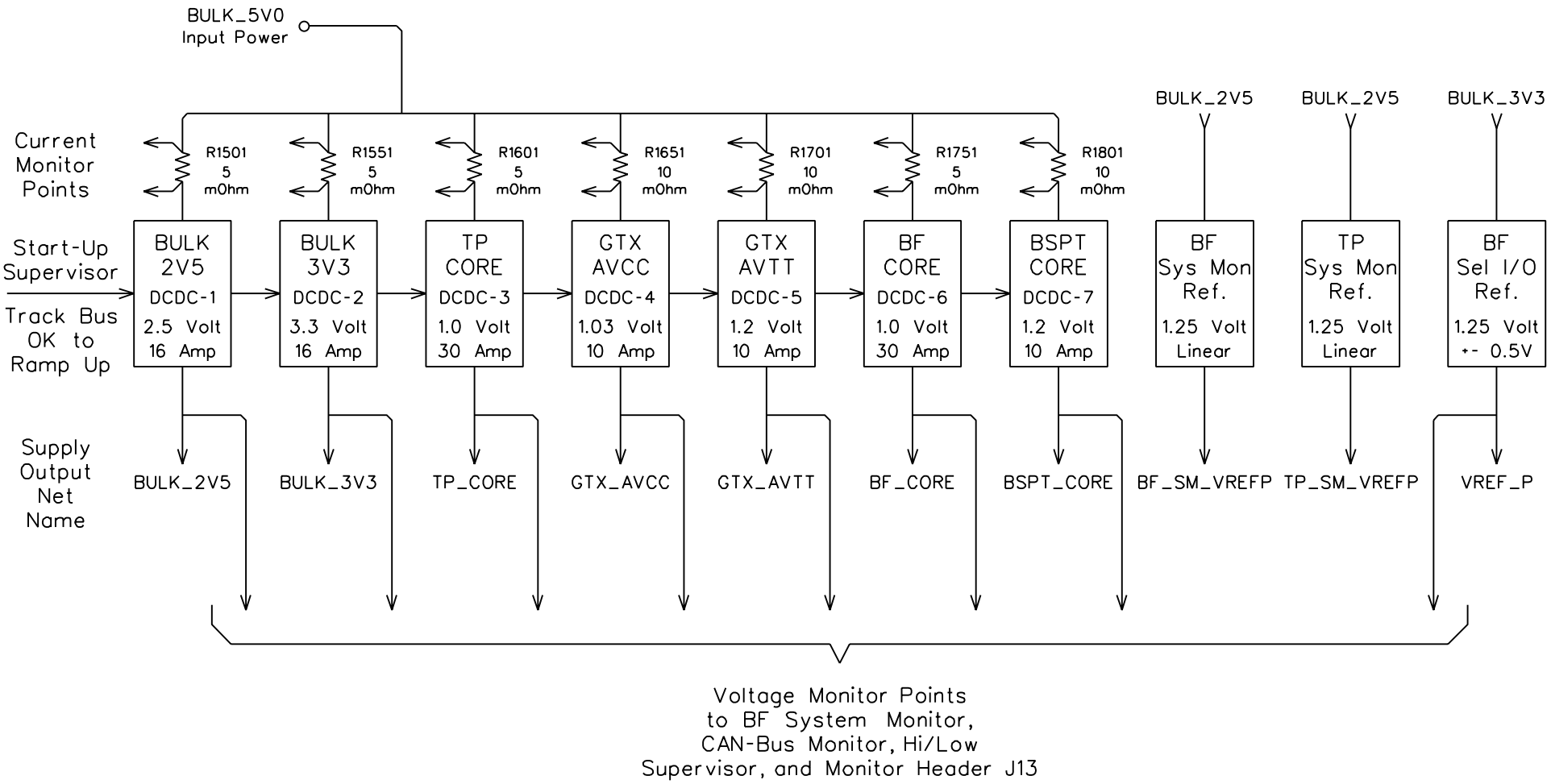
5 Volt Power Entry and Distribution



Note: On board SMD fuse F3 is mounted near the bottom front panel connector J12. It is in the JTAG Pod power circuit.

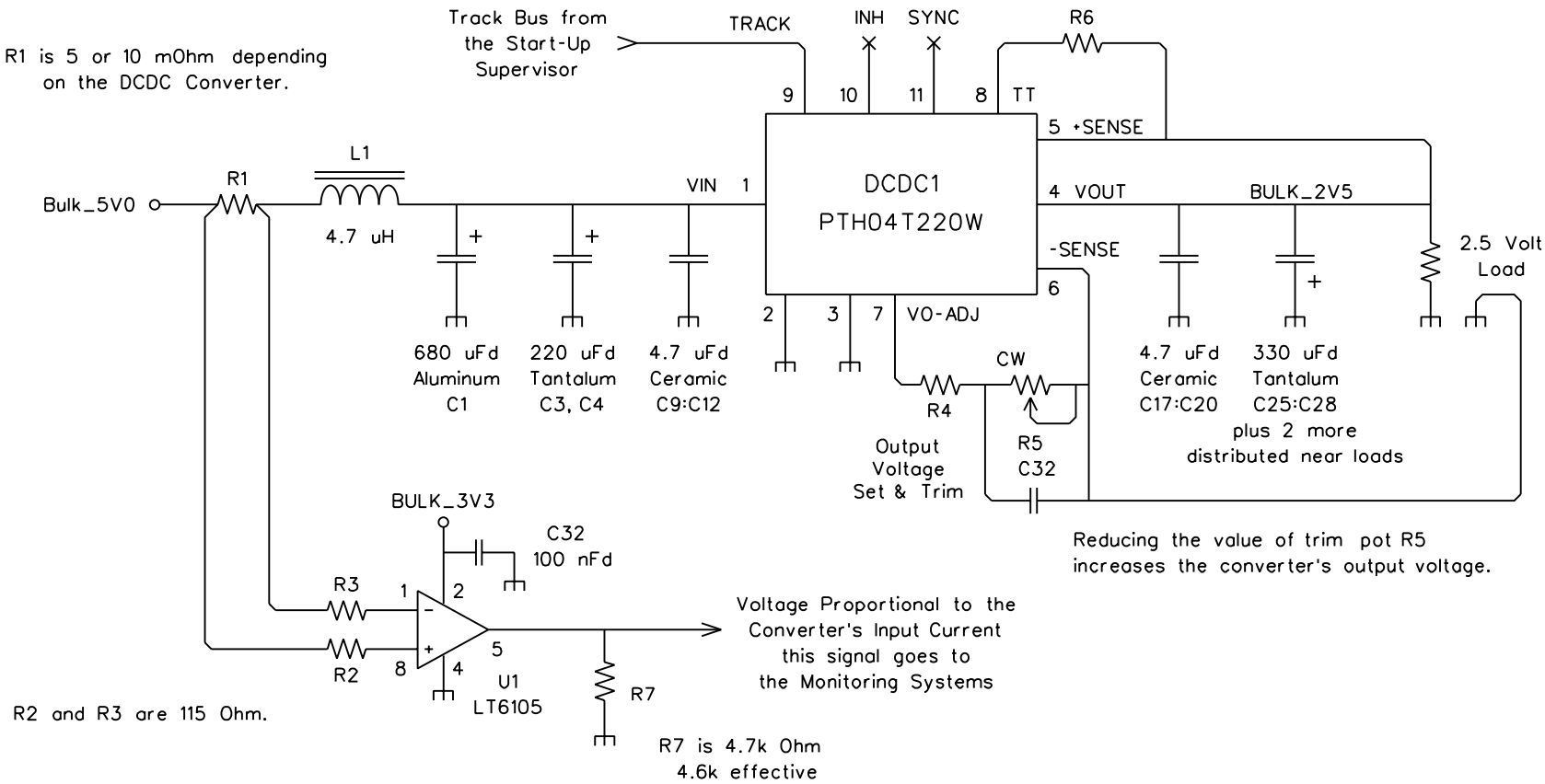
Rev. 3-Aug-2013

CMX On Card Power Supplies



Rev. 13-Dec-2013

DC-DC Converter Design



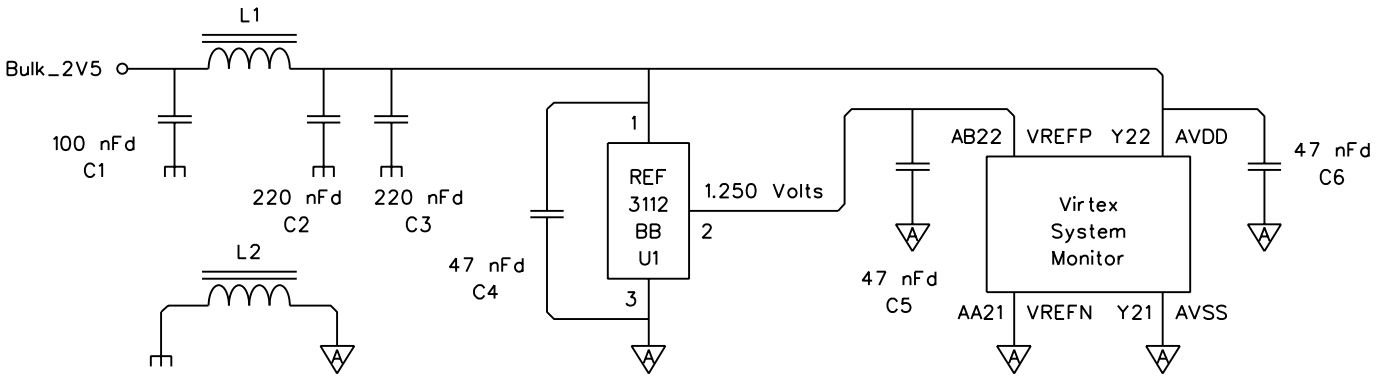
The BULK_2V5 DC/DC Converter is shown.
The other 6 converters are similar in design.
Actual reference designators are larger by 1500.
Reference designators increment by 50
from one converter to the next.

The TP_CORE converter includes disable jumpers.
The GTX_AVCC and GTX_AVTT converters include
separate LC output filters for both their BF and TP loads.

Rev. 13-Dec-2013

CMX Reference Supplies

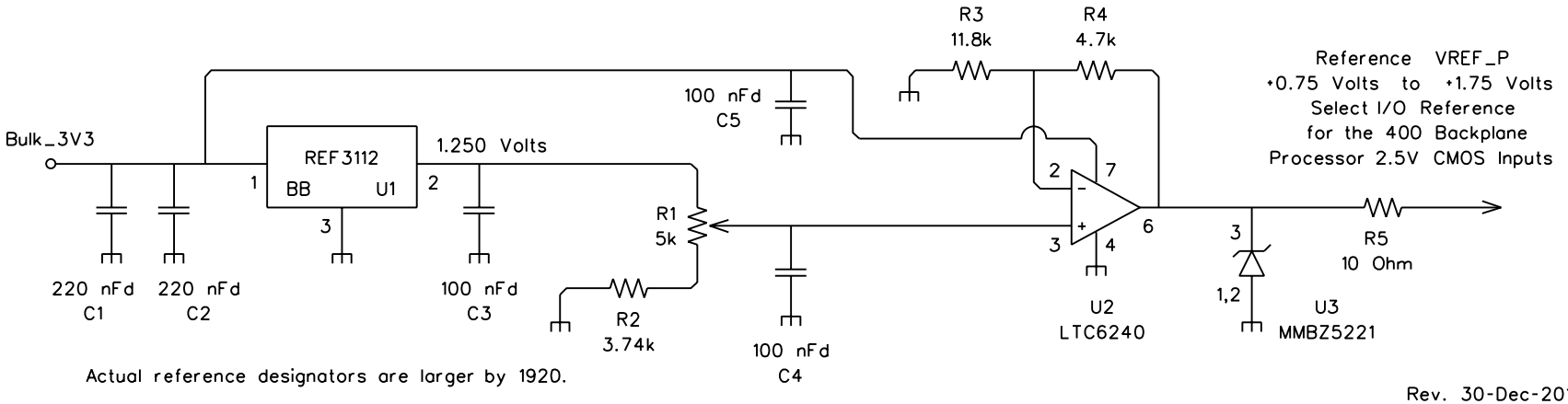
BF and TP Virtex System Monitor References



The BF System Monitor Reference is shown.
Actual reference designators are larger by 1900.

The TP reference design is the same.
TP reference designators increment by 10.

BF Select I/O Variable Reference for Backplane Signals

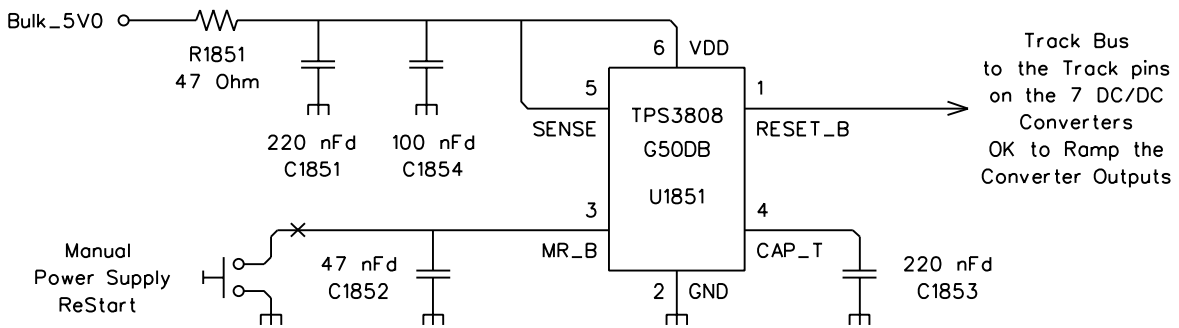


Actual reference designators are larger by 1920.

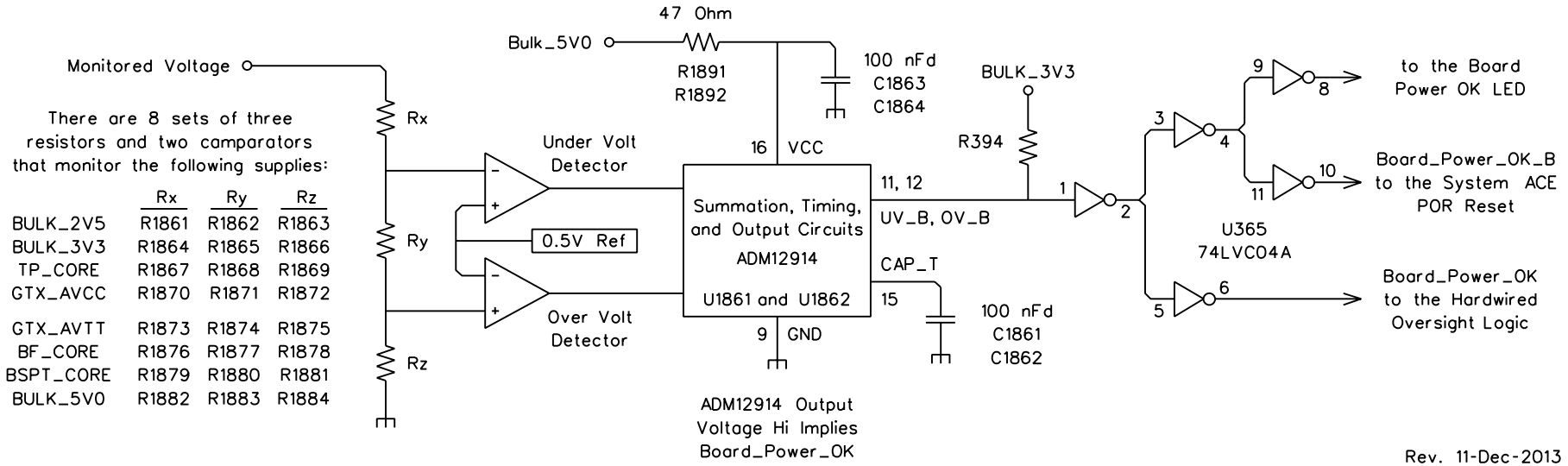
Rev. 30-Dec-2013

CMX Power Supply Supervisors

Converter Startup Supervisor



Hi/Low Board-Power-OK Supervisor

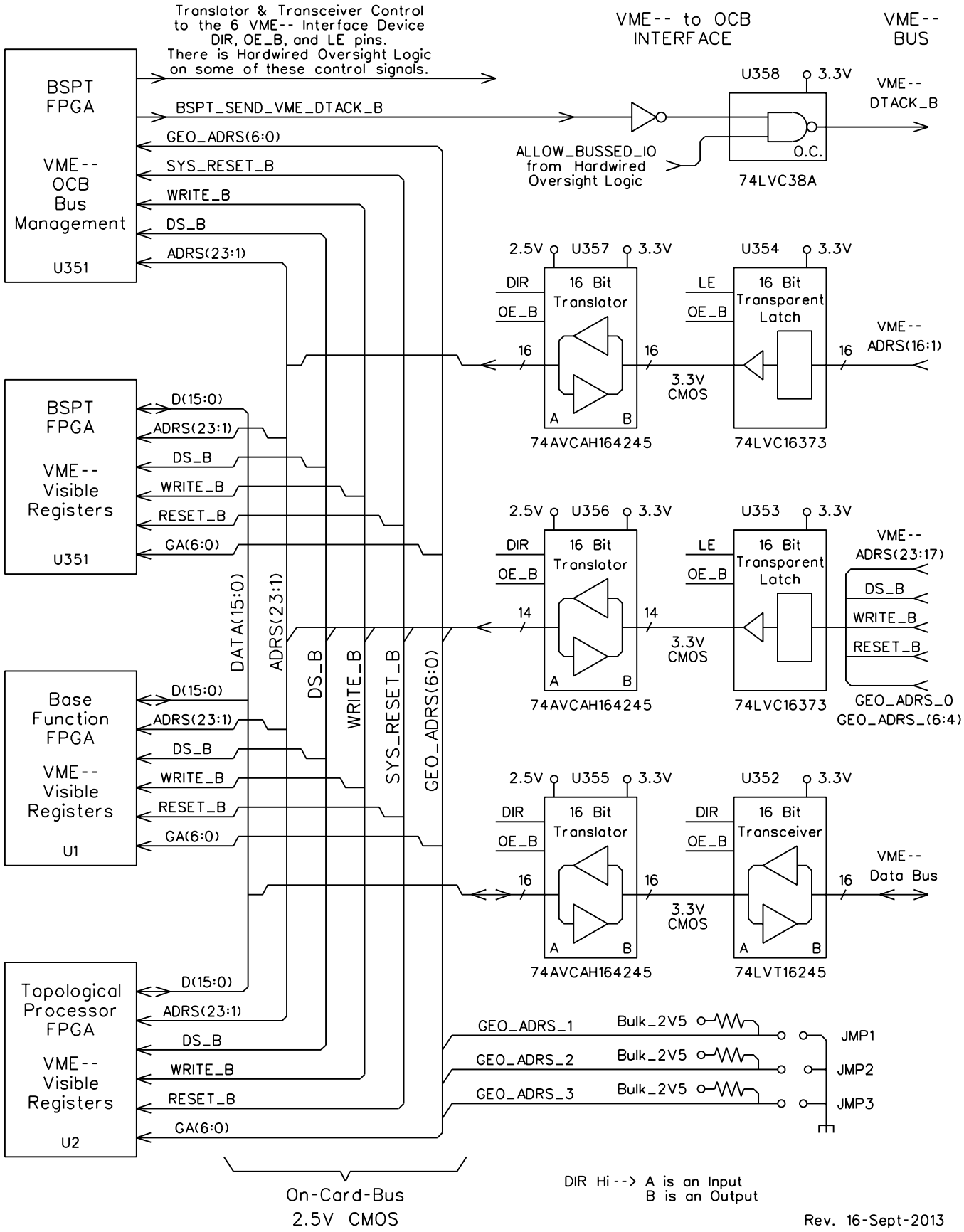


There are 8 sets of three resistors and two comparators that monitor the following supplies:

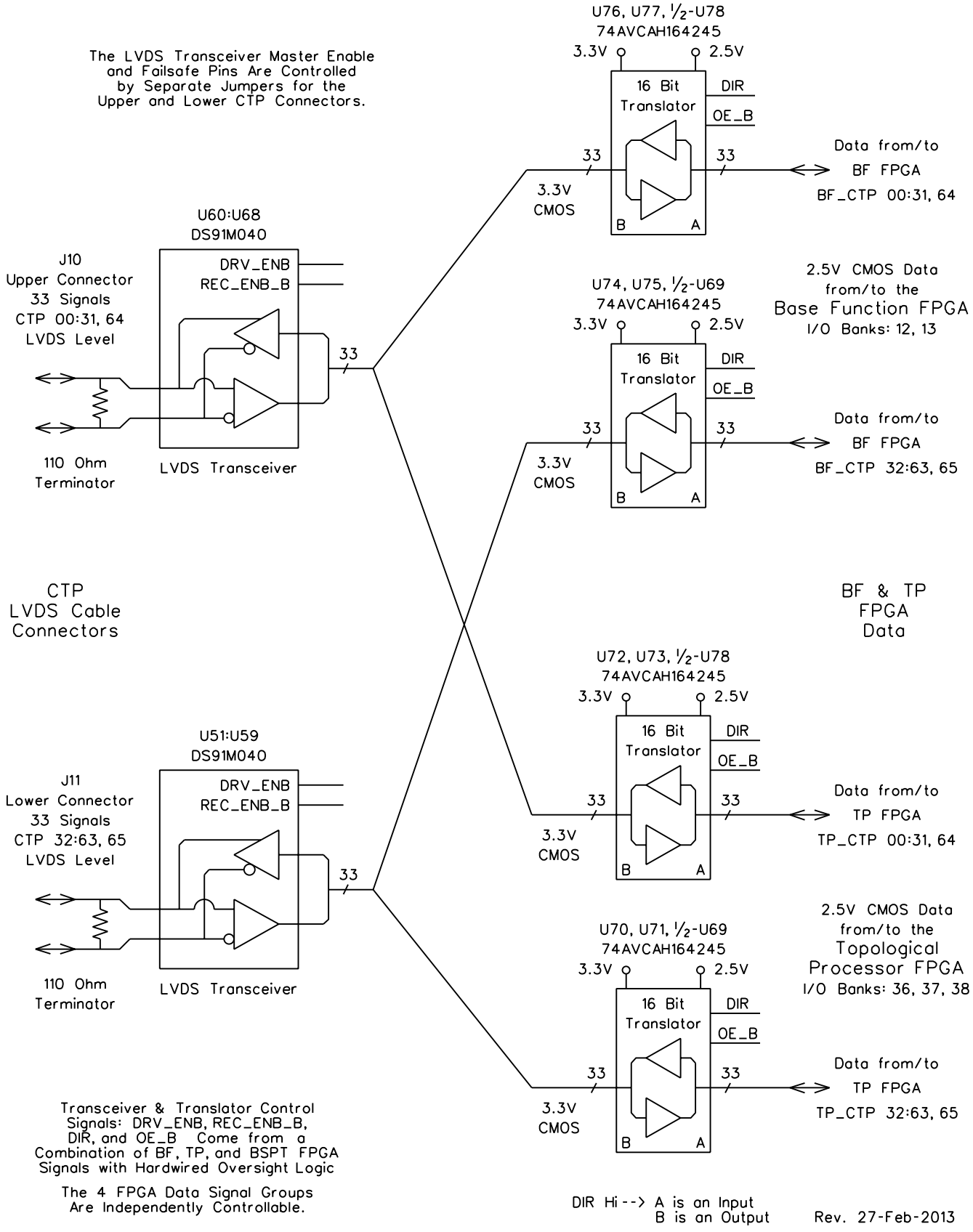
	Rx	Ry	Rz
BULK_2V5	R1861	R1862	R1863
BULK_3V3	R1864	R1865	R1866
TP_CORE	R1867	R1868	R1869
GTX_AVCC	R1870	R1871	R1872
GTX_AVTT	R1873	R1874	R1875
BF_CORE	R1876	R1877	R1878
BSPT_CORE	R1879	R1880	R1881
BULK_5V0	R1882	R1883	R1884

Rev. 11-Dec-2013

On-Card-Bus and VME-- Interface



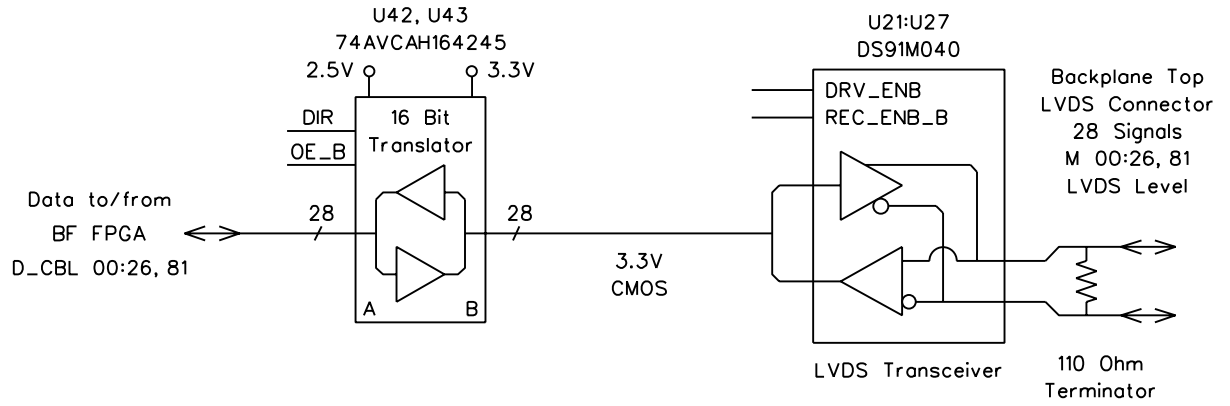
CTP Front Panel LVDS Transceivers

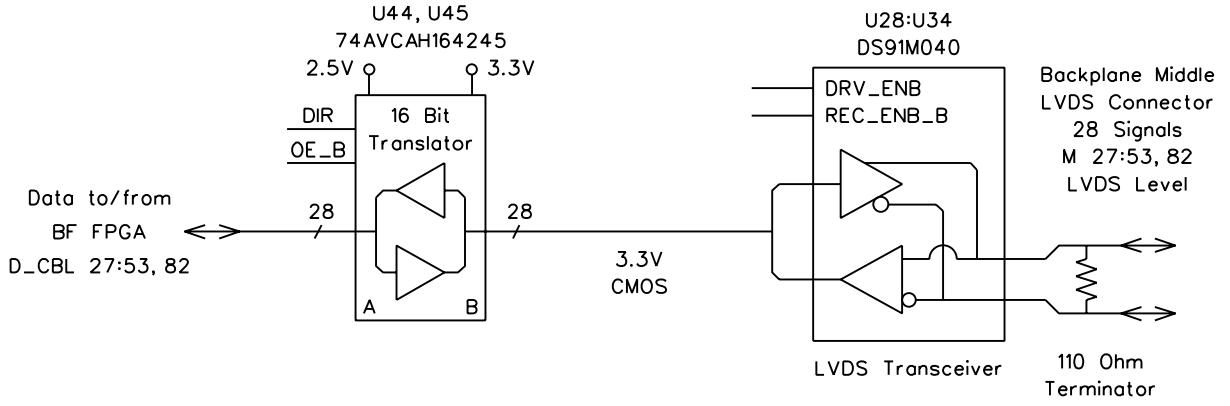


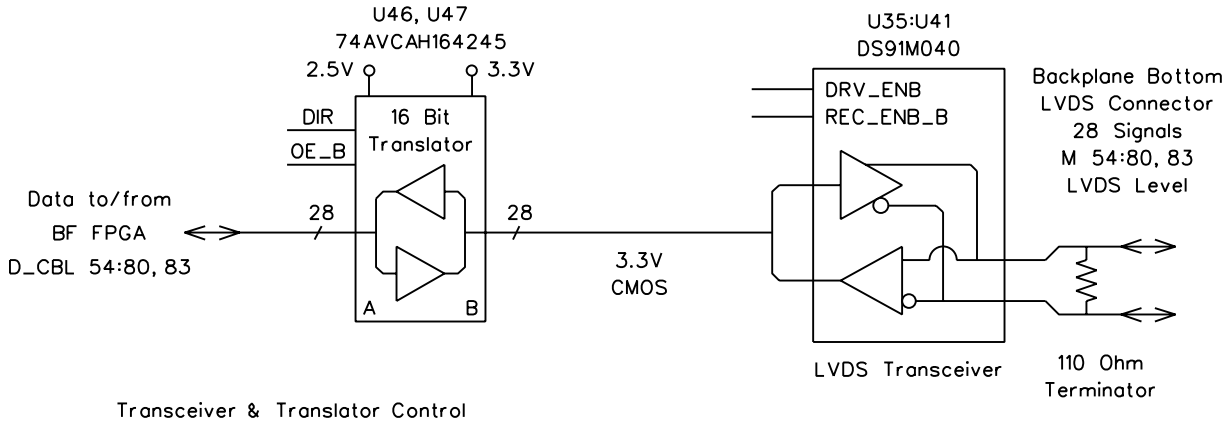
Backplane LVDS Cable Transceivers

2.5V CMOS Data
from/to the
Base Function FPGA
I/O Banks: 15, 16, 17

Backplane LVDS
Cable Connections







Transceiver & Translator Control Signals: DRV_ENB, REC_ENB_B, DIR, and OE_B Come from a Combination of BF and BSPT FPGA Signals with Hardwired Oversight Logic

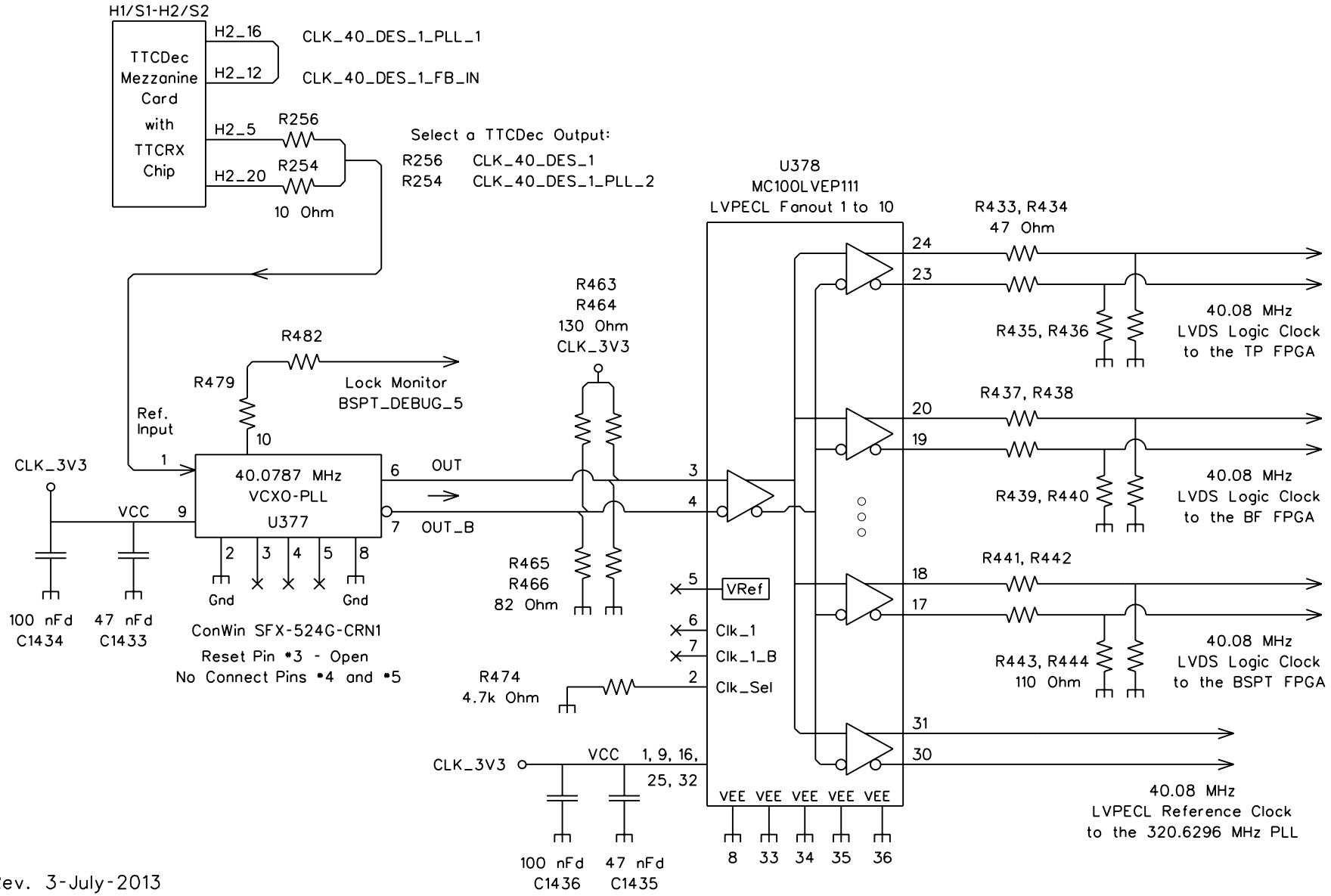
The Direction of Data Flow Is Independently Controllable for the 3 Backplane LVDS Cables.

DIR Hi --> A is an Input
B is an Output

The LVDS Transceiver Master Enable and Failsafe Pins Are Controlled by Separate Jumpers for the Top, Middle, and Bottom LVDS Cables.

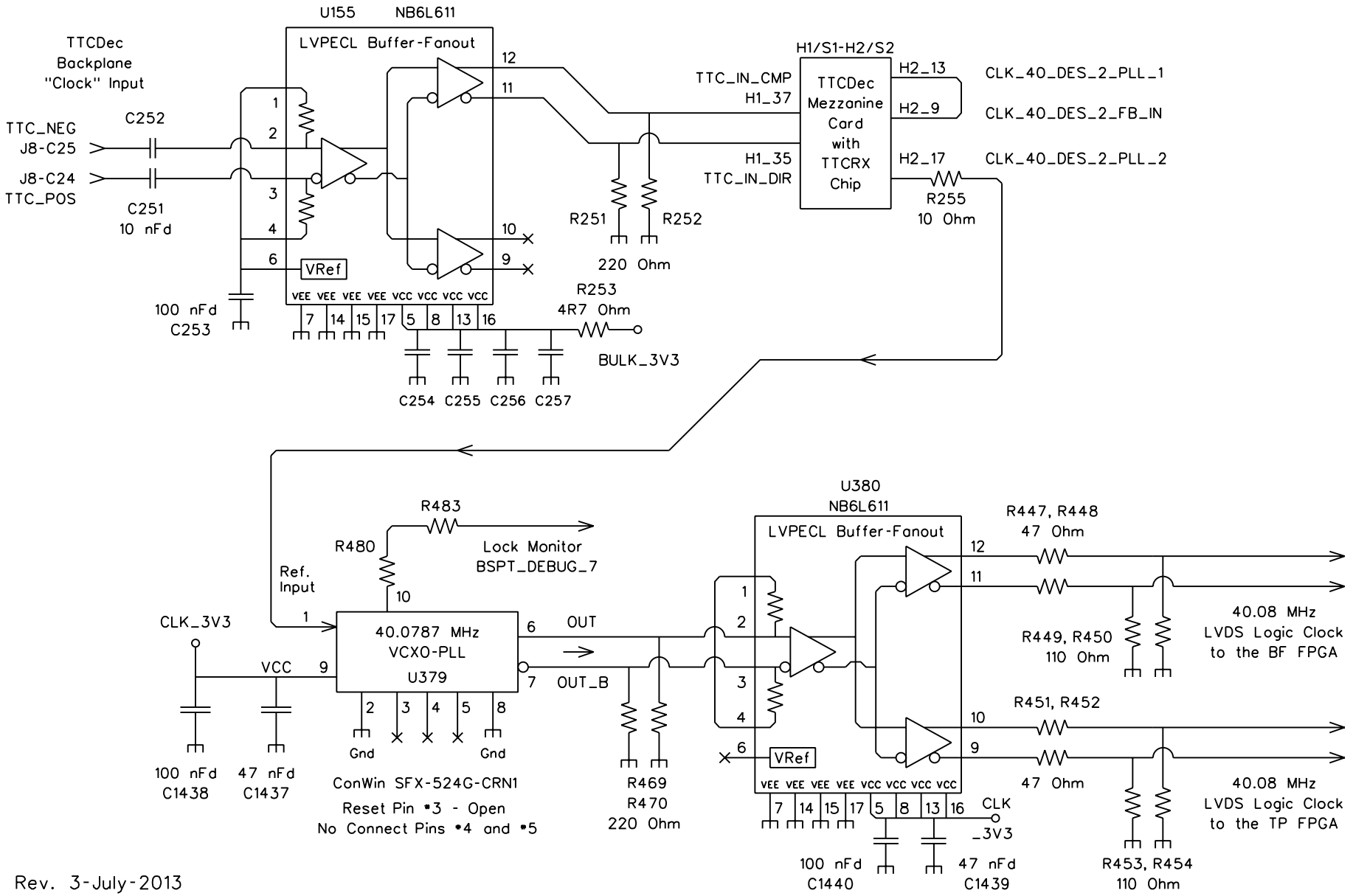
Rev. 27-Feb-2013

CMX 40.08 MHz DeSkew-1 LHC Clock



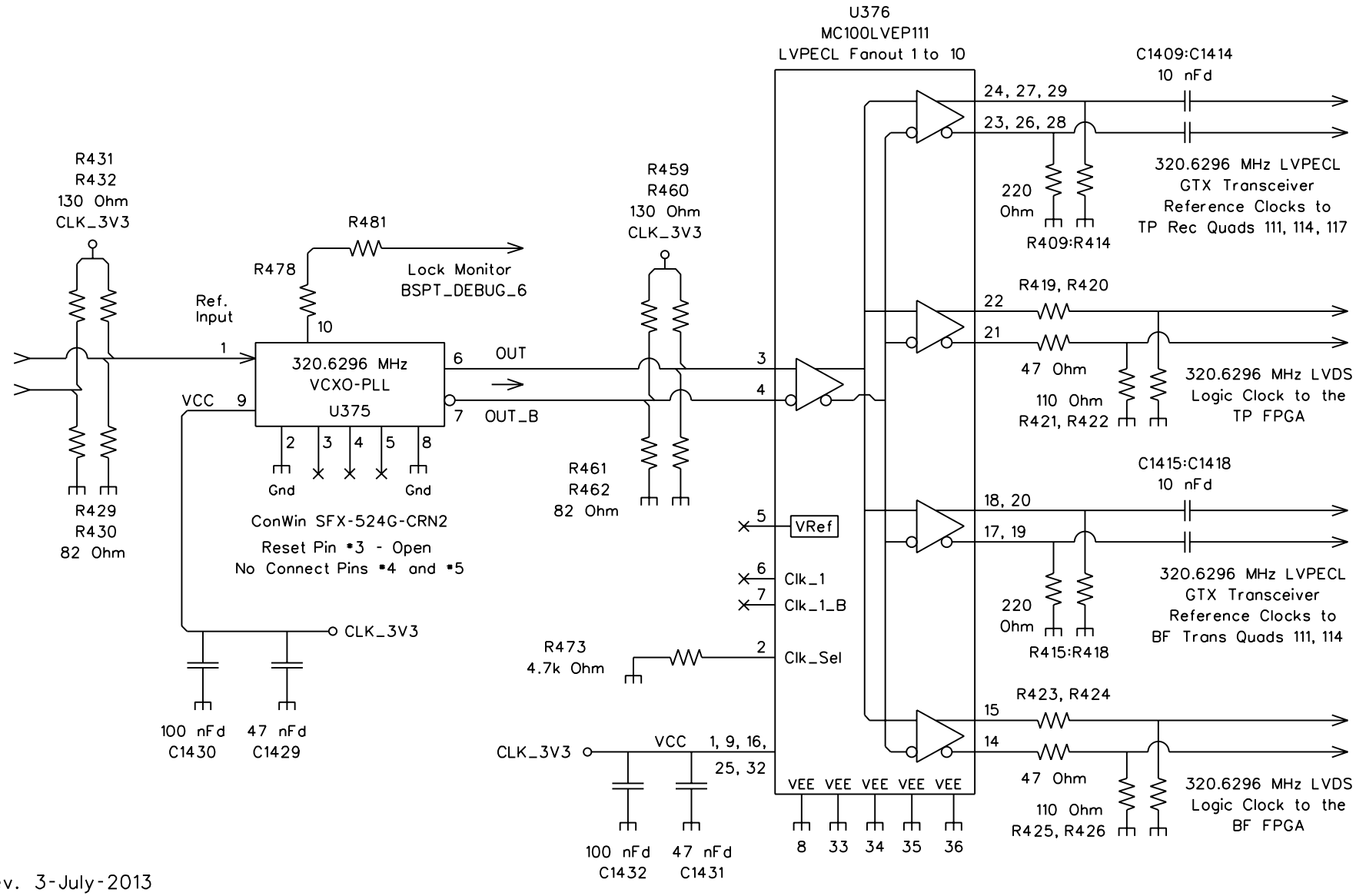
Rev. 3-July-2013

CMX 40.08 MHz DeSkew-2 LHC Clock



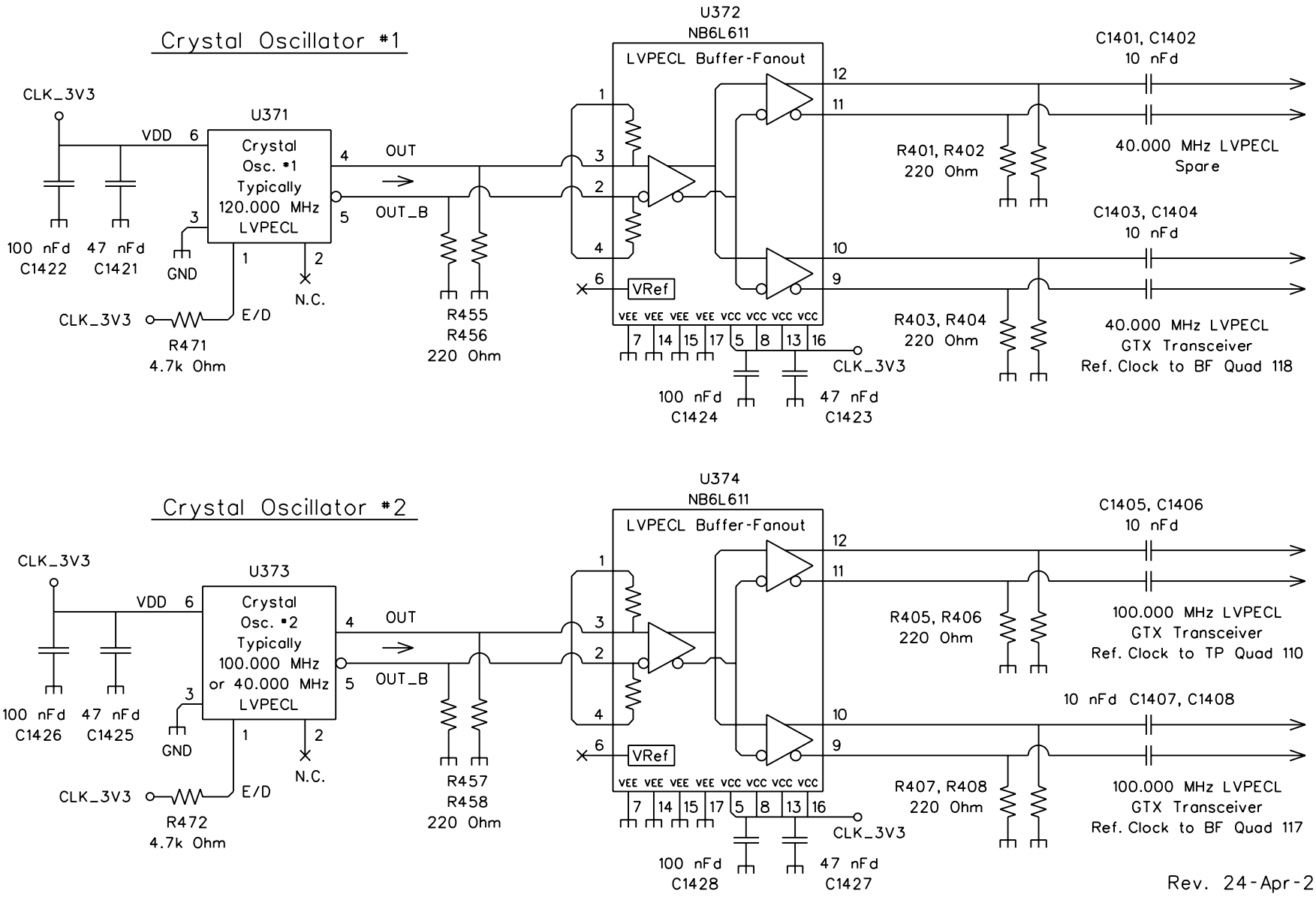
Rev. 3-July-2013

CMX 320.6296 MHz LHC Clock



Rev. 3-July-2013

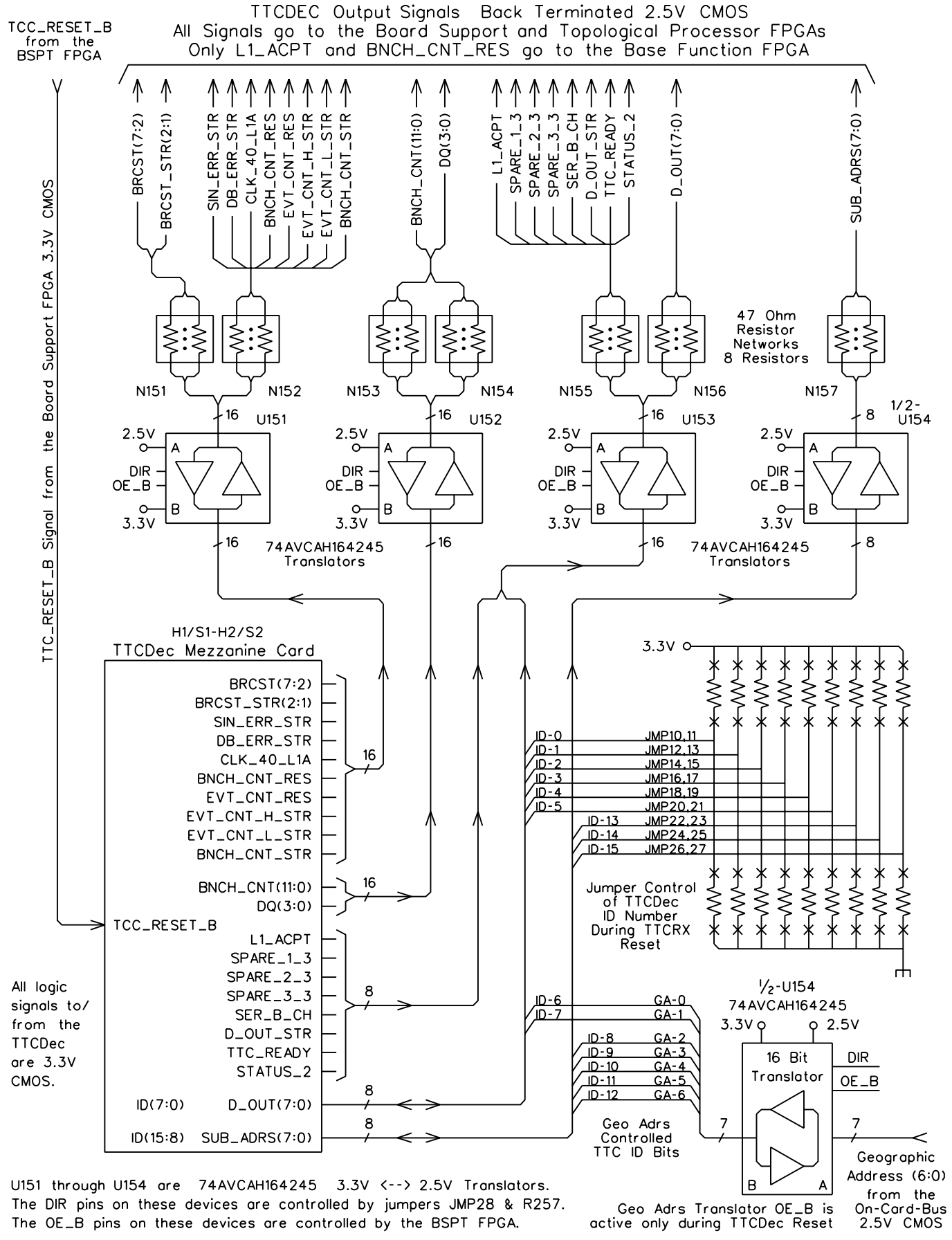
CMX Crystal Oscillator #1 and #2



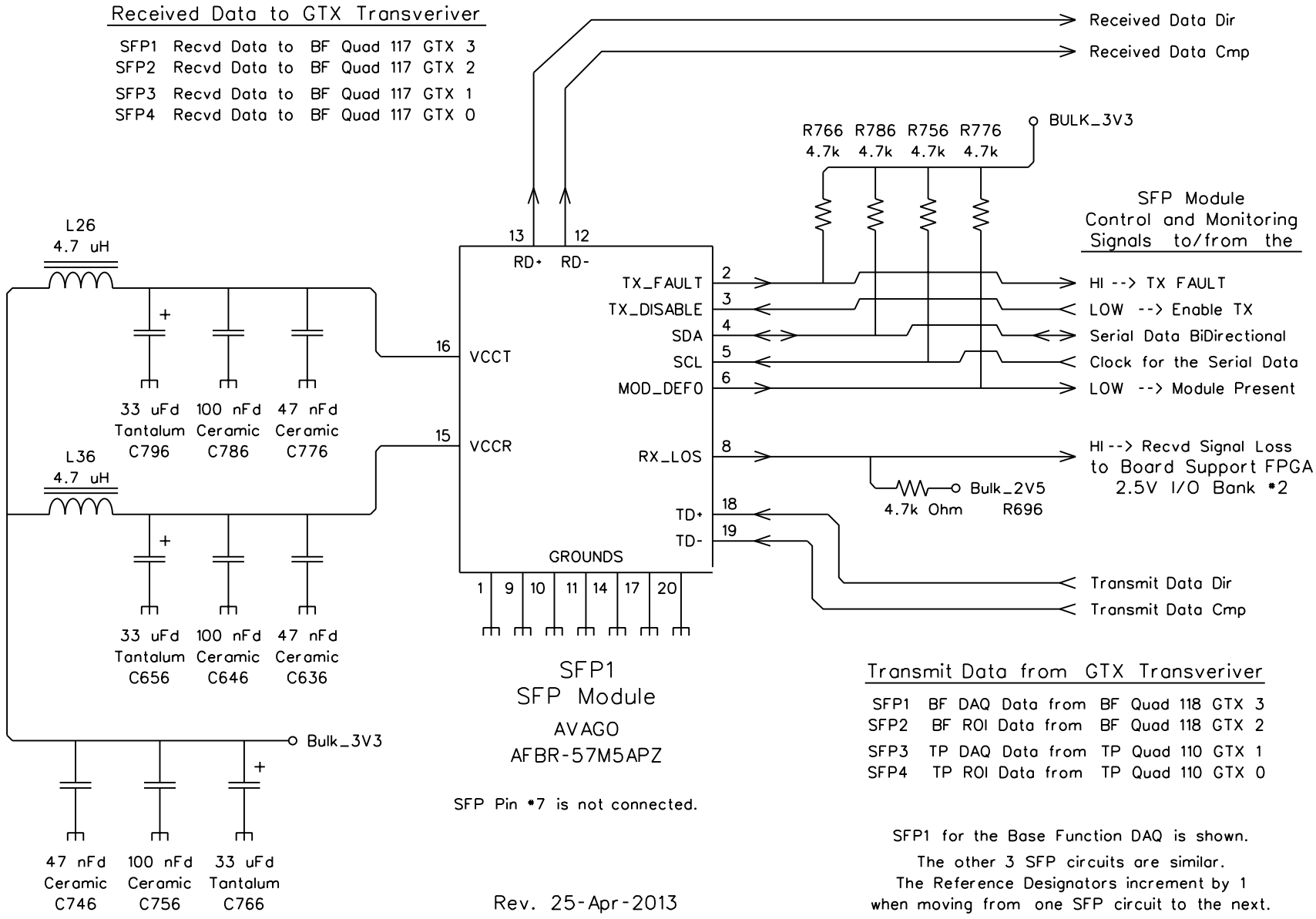
Rev. 24-Apr-2014

TTCDec Data Distribution

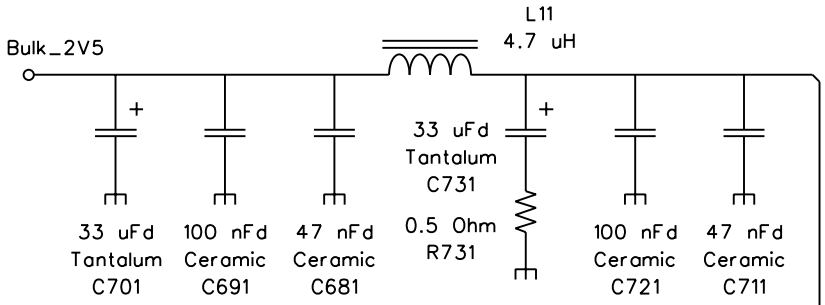
Rev. 25-Sept-2013



SFP Low-Speed Optical Transceivers

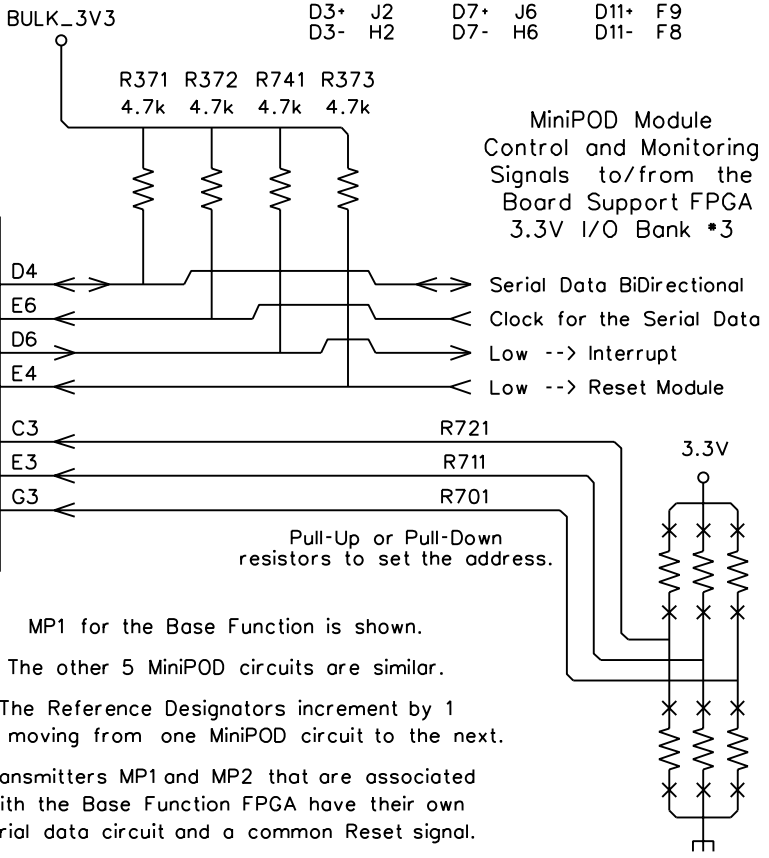


MiniPOD Hi-Speed Optical Components



MiniPOD Transmit or Receive Data Pairs

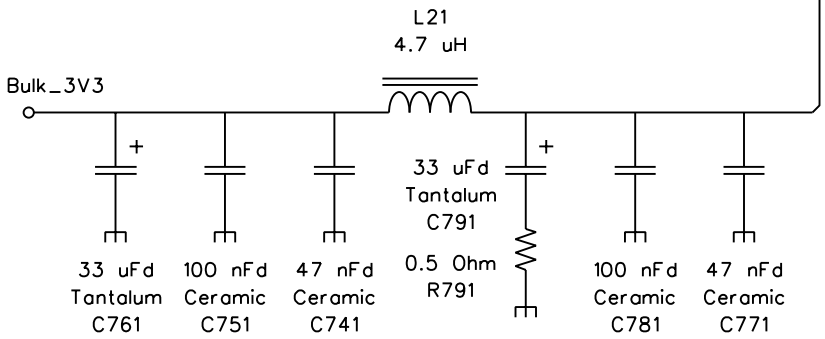
Signal	Pin	Signal	Pin	Signal	Pin
D0+	D1	D4+	A4	D8+	A8
D0-	D2	D4-	B4	D8-	B8
D1+	F1	D5+	J4	D9+	J8
D1-	F2	D5-	H4	D9-	H8
D2+	A2	D6+	A6	D10+	D9
D2-	B2	D6-	B6	D10-	D8
D3+	J2	D7+	J6	D11+	F9
D3-	H2	D7-	H6	D11-	F8



MiniPOD Module
Control and Monitoring
Signals to/from the
Board Support FPGA
3.3V I/O Bank *3

The MiniPOD No-Connection Pins are:
C7, D5, E5, E7, F5, F6, G7

The MiniPOD Ground Pins are:
A1, A3, A5, A7, A9
B1, B3, B5, B7, B9
C1, C2, C8, C9
D3, D7
E1, E2, E8, E9
F3, F7
G1, G2, G8, G9
H1, H3, H5, H7, H9
J1, J3, J5, J7, J9



MP1 for the Base Function is shown.

The other 5 MiniPOD circuits are similar.

The Reference Designators increment by 1 when moving from one MiniPOD circuit to the next.

Transmitters MP1 and MP2 that are associated with the Base Function FPGA have their own serial data circuit and a common Reset signal.

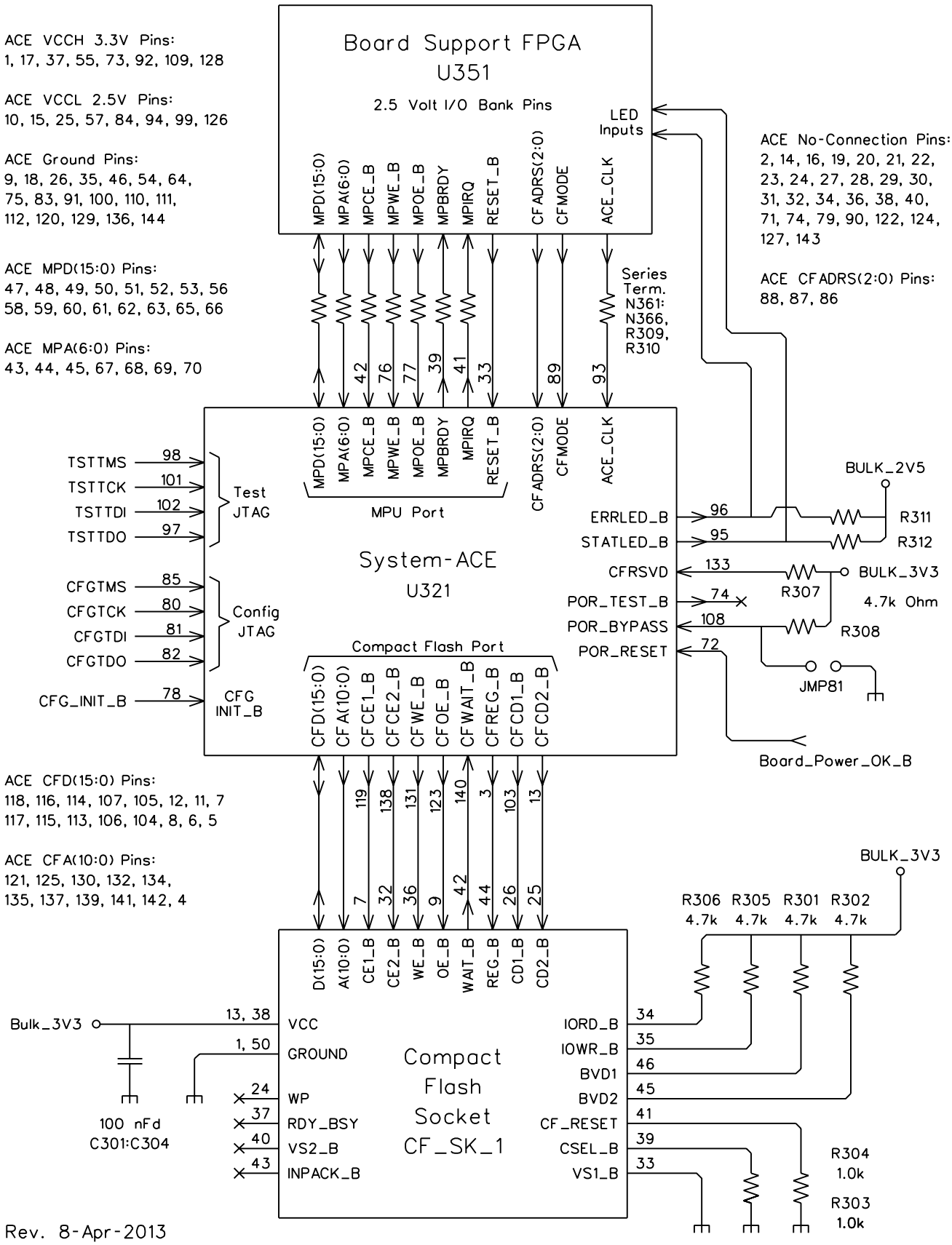
Receivers MP3, MP4, and MP5 that are associated with to Topological Processor FPGA have their own serial data circuit and a common Reset Signal.

All 5 MiniPODs have independent Interrupt signals.

MP1, MP3 Adrs = 0
MP2, MP4 Adrs = 1
MP5 Adrs = 2

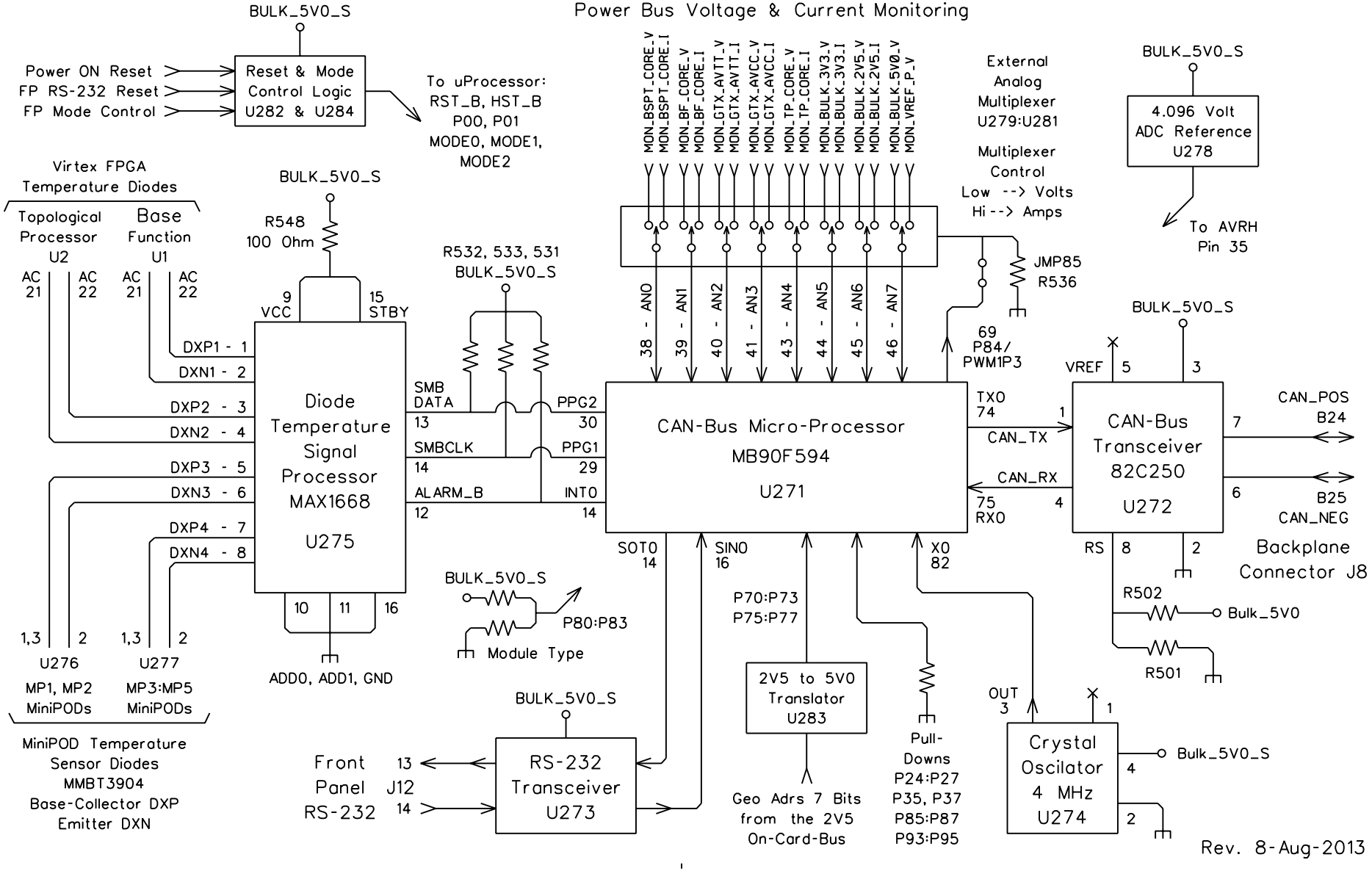
Rev. 6-Feb-2013

System-ACE Connections

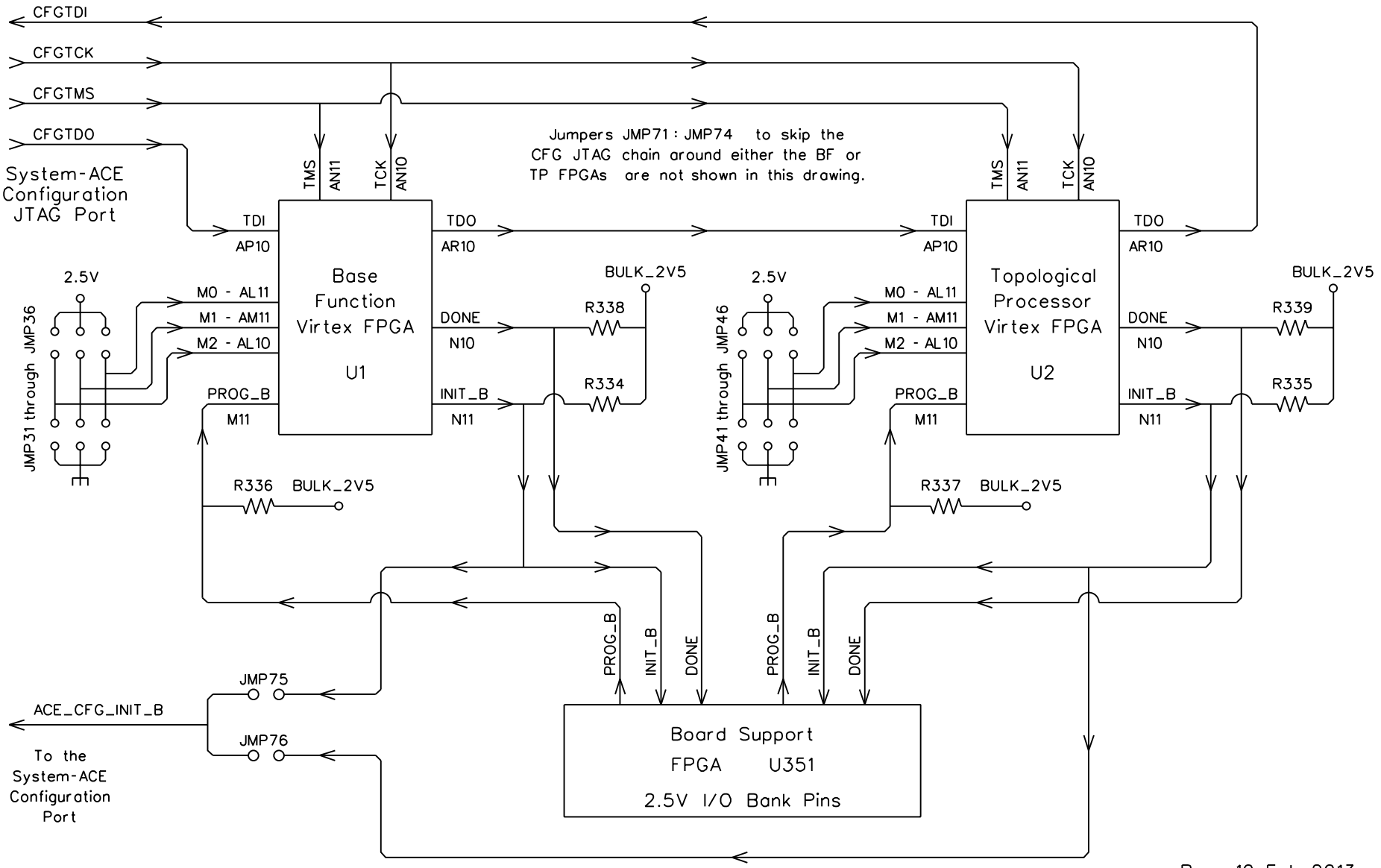


Rev. 8-Apr-2013

CAN-Bus Monitoring



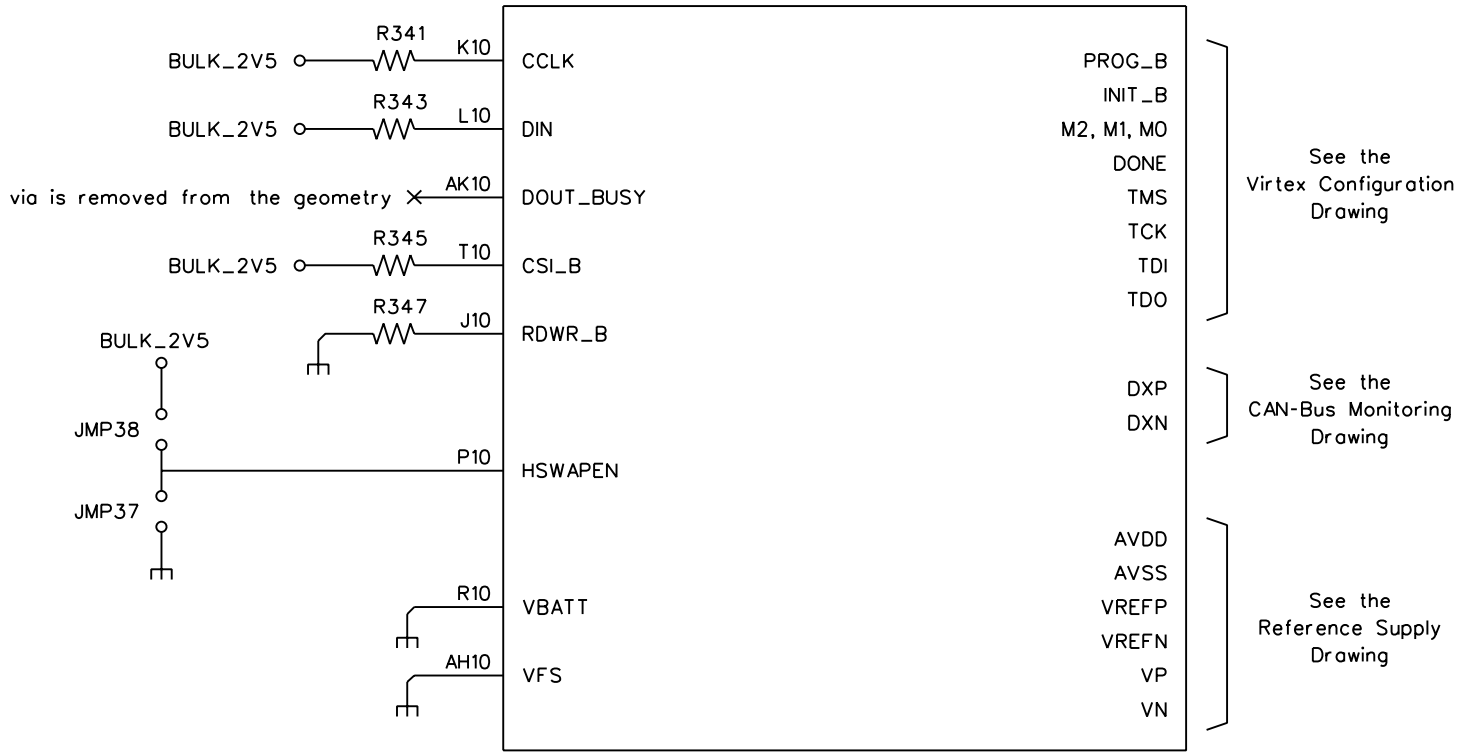
CMX Virtex FPGA Configuration



Rev. 10-Feb-2013

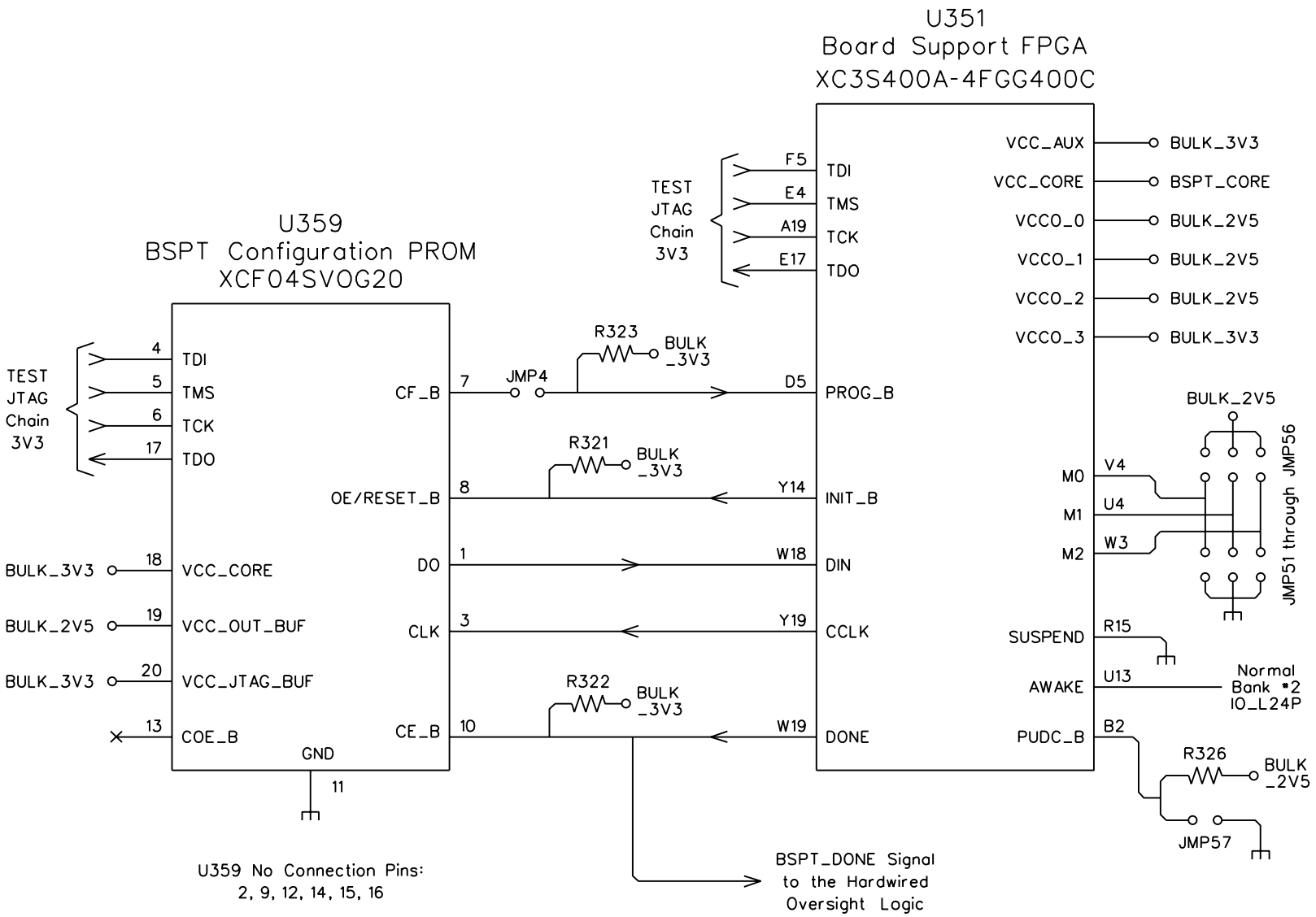
CMX Virtex FPGA Bank #0

Virtex-6 FPGA
Bank #0 Pins
U1 and U2
26 Pins on each



Rev. 11-Feb-2013

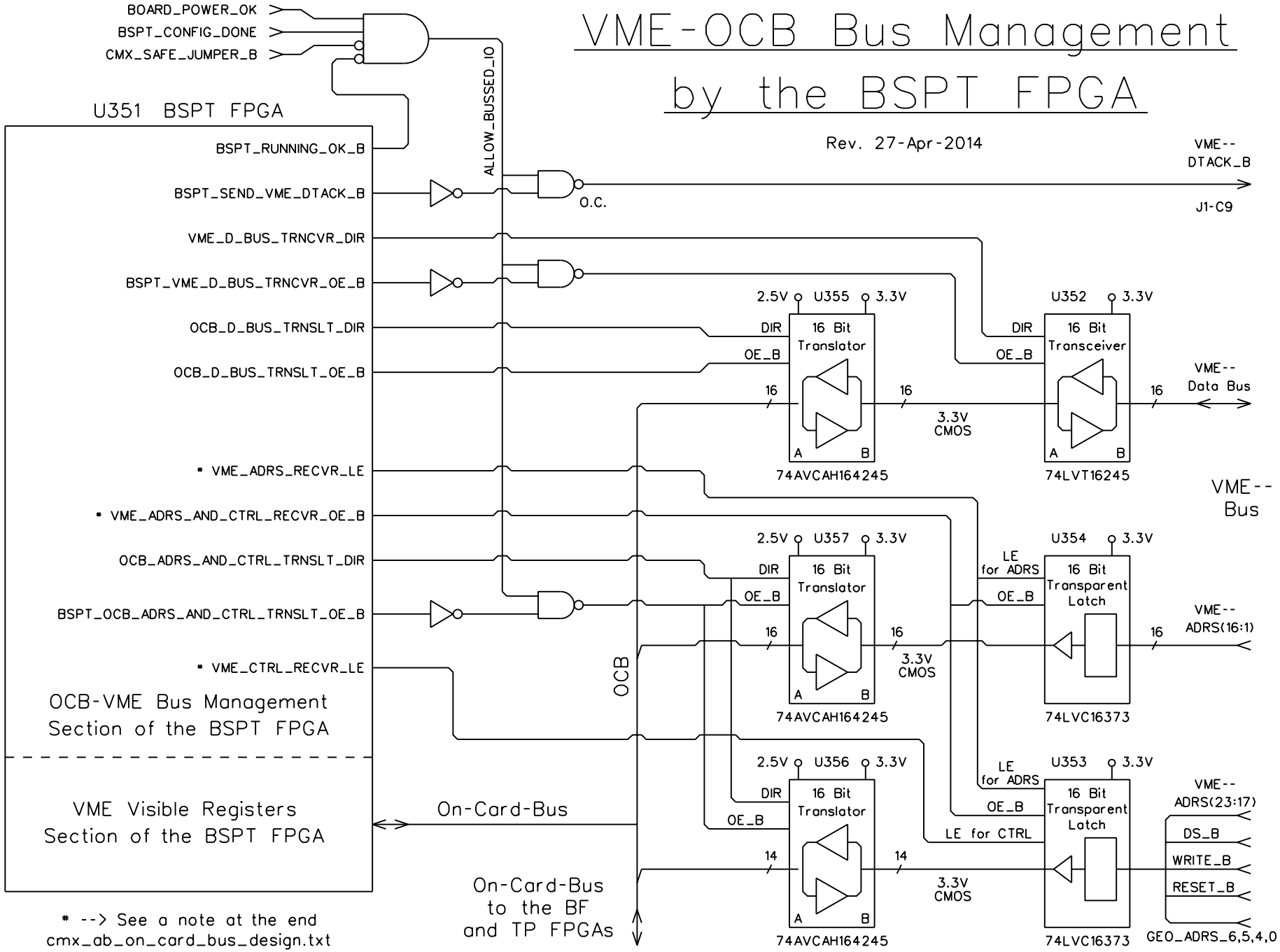
CMX Board Support FPGA Configuration



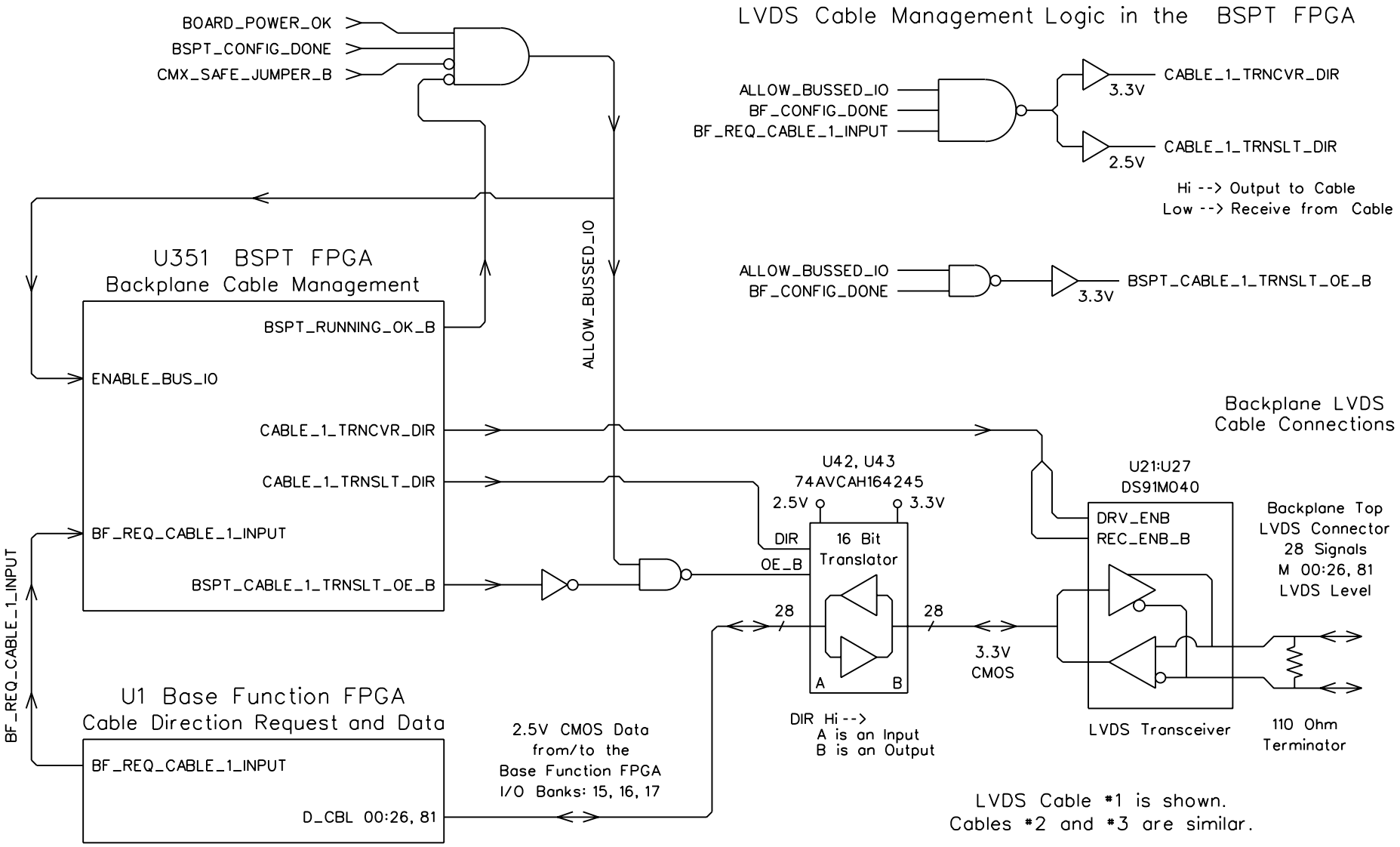
Rev. 28-Feb-2013

VME-OCB Bus Management by the BSPT FPGA

Rev. 27-Apr-2014

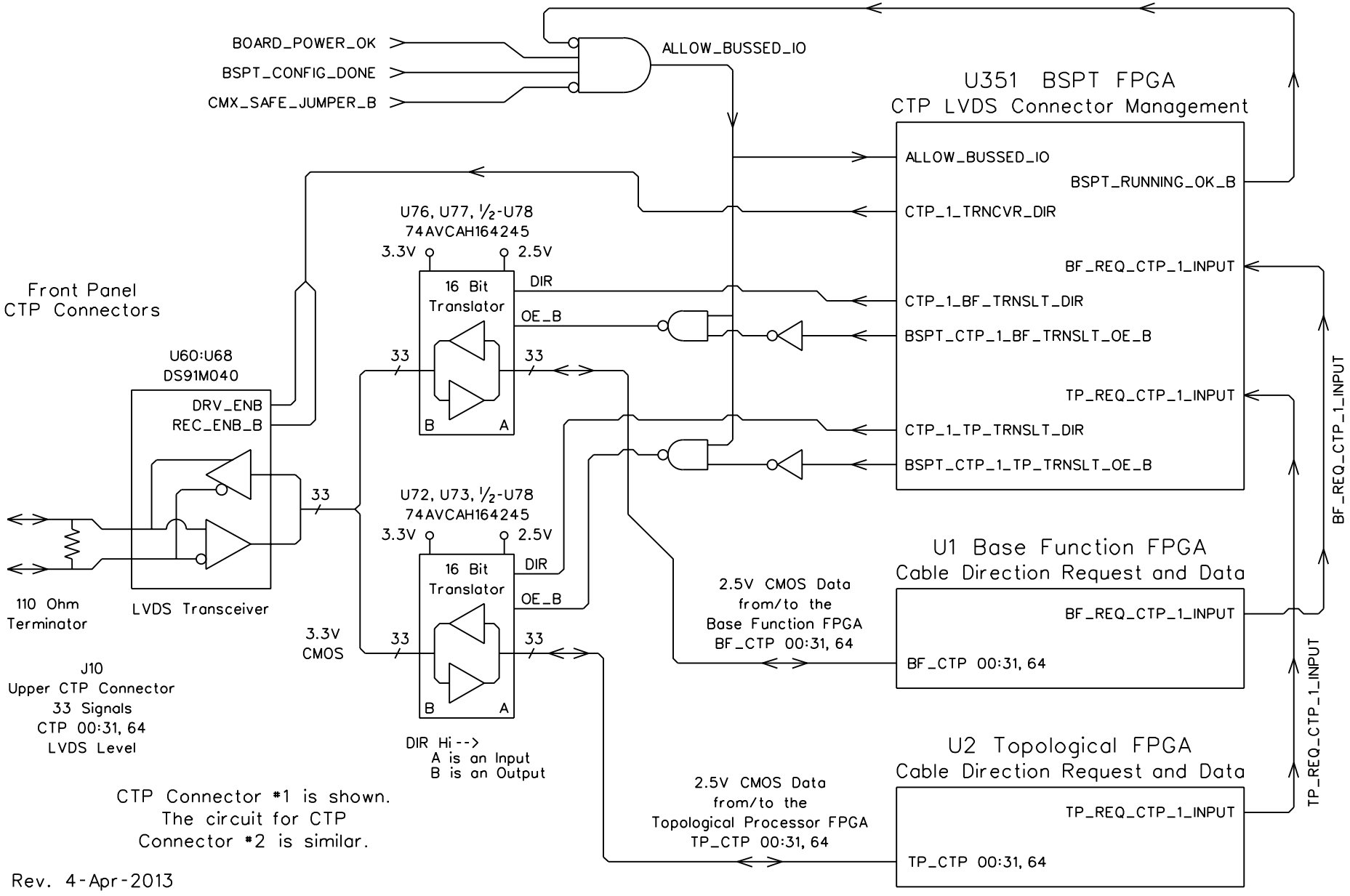


Backplane LVDS Cable Management



Rev. 4-Apr-2013

CTP LVDS Connector Management



CTP Connector #1 is shown.
The circuit for CTP
Connector #2 is similar.

Rev. 4-Apr-2013

CTP Connector Management Logic in the BSPT FPGA

CTP Connector Management Rules

When the "TP Installed Jumper" says that the TP FPGA is NOT installed on this CMX card then: force the INTERNAL_TP_CONFIG_DONE signal Low force the INTERNAL_TP_REQ_CTP_1_INPUT signal Hi.

The LVDS Transceiver direction is is Output unless both the BF and TP request the direction to be Input.

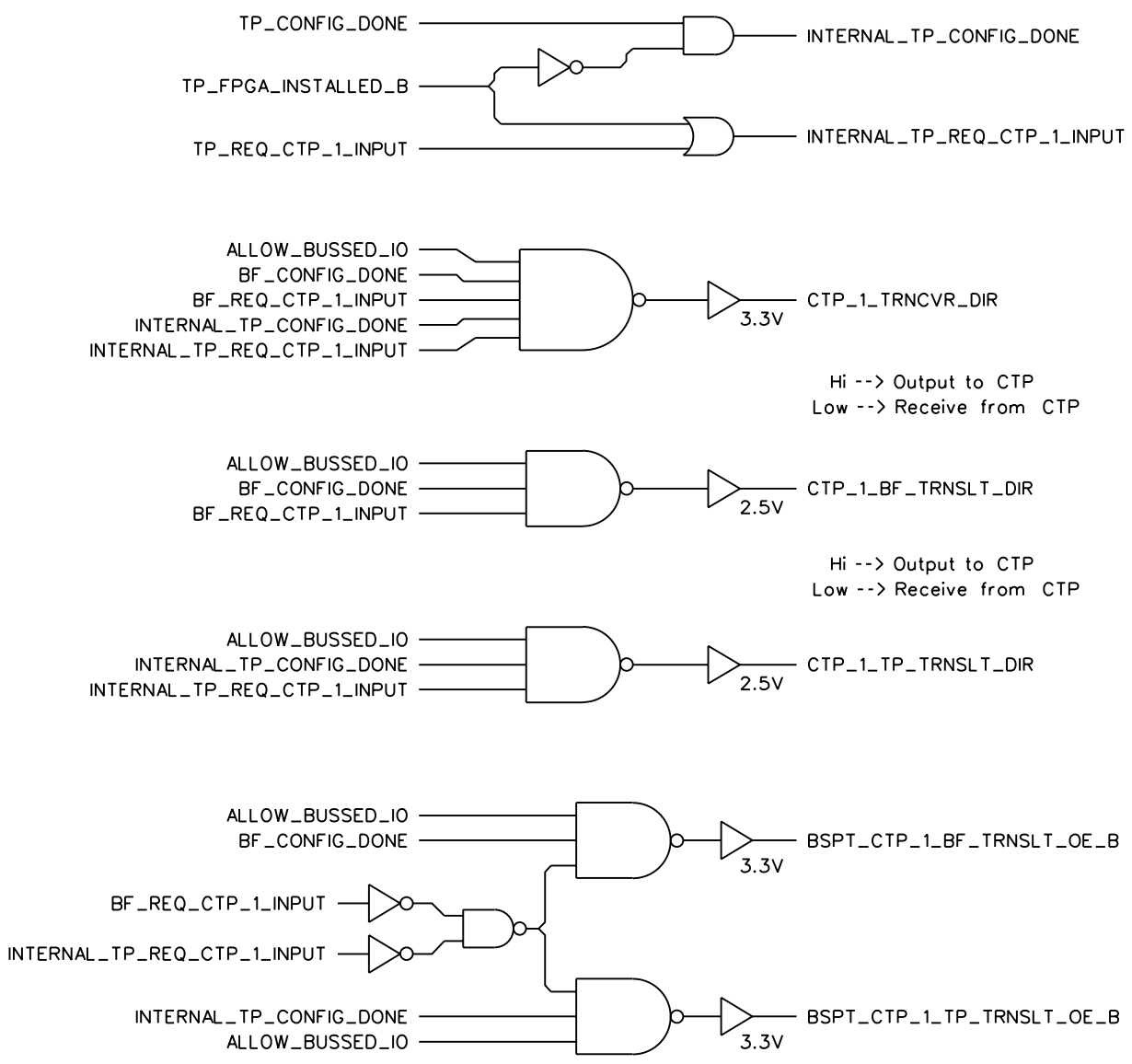
Never enable the Translator Output Drivers unless the associated FPGA (BF or TP) is Configured.

When both the BF and TP FPGAs are Configured you may Enable both the BF and the TP Translator Output Drivers except when both the BF and TP have requested the Direction to be Output. In that case disable both the BF and the TP Translator Output Drivers.

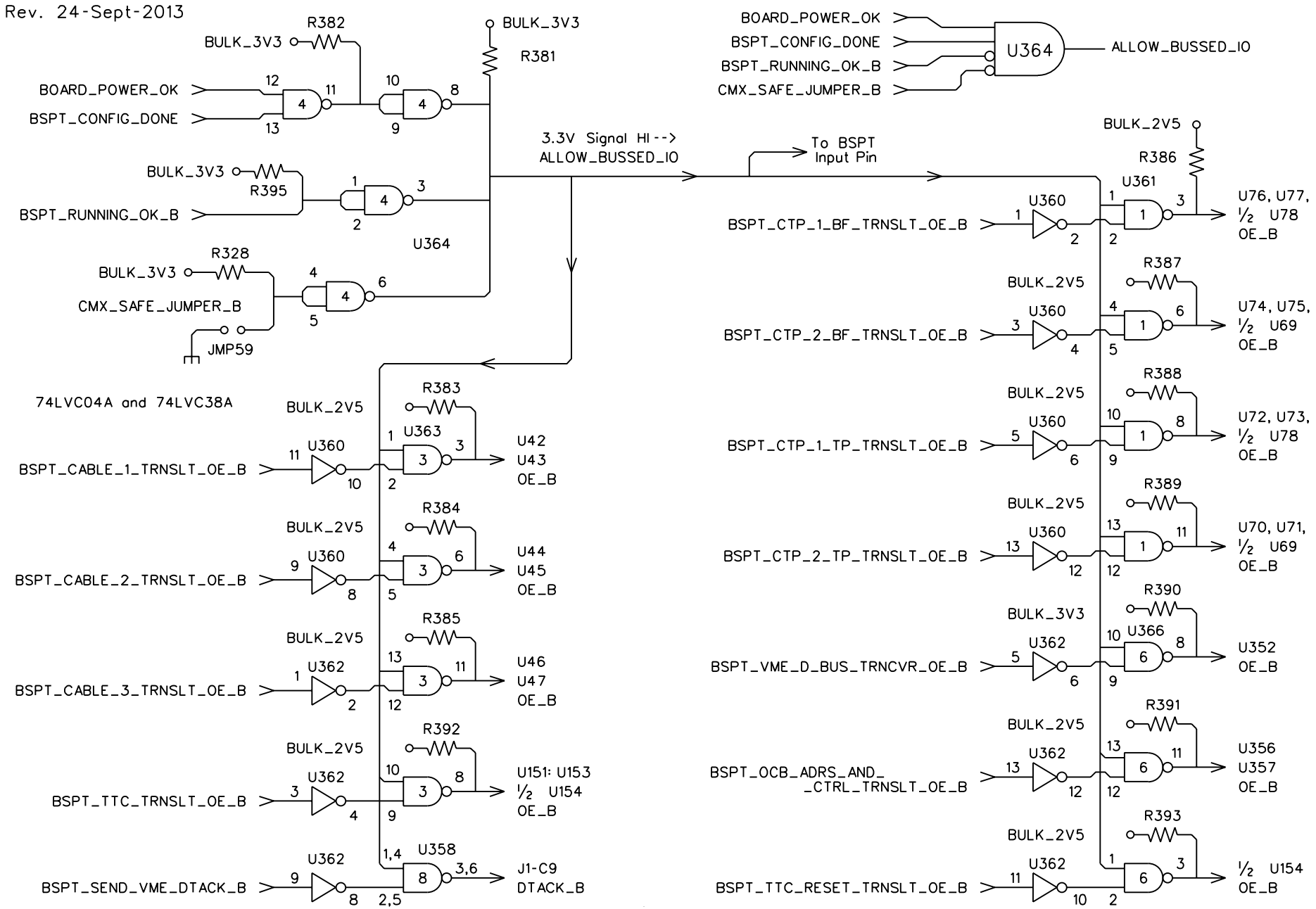
It is an Error Condition when both the BF and TP are requesting the Direction to be Output.

The logic for CTP Connector #1 is shown. The logic for CTP Connector #2 is similar.

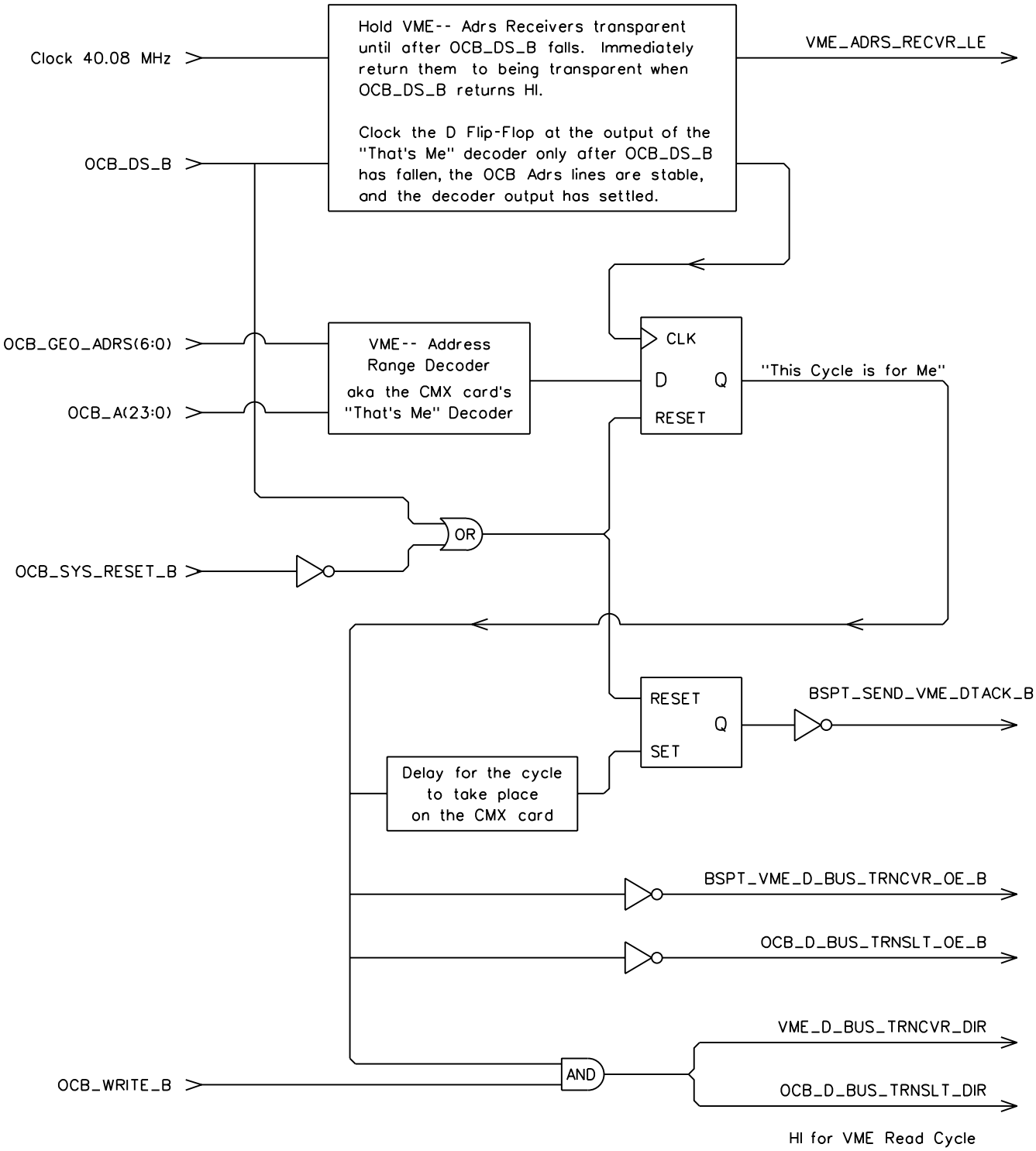
Rev. 4-Apr-2013



Hardwired Oversight Logic - the Full System



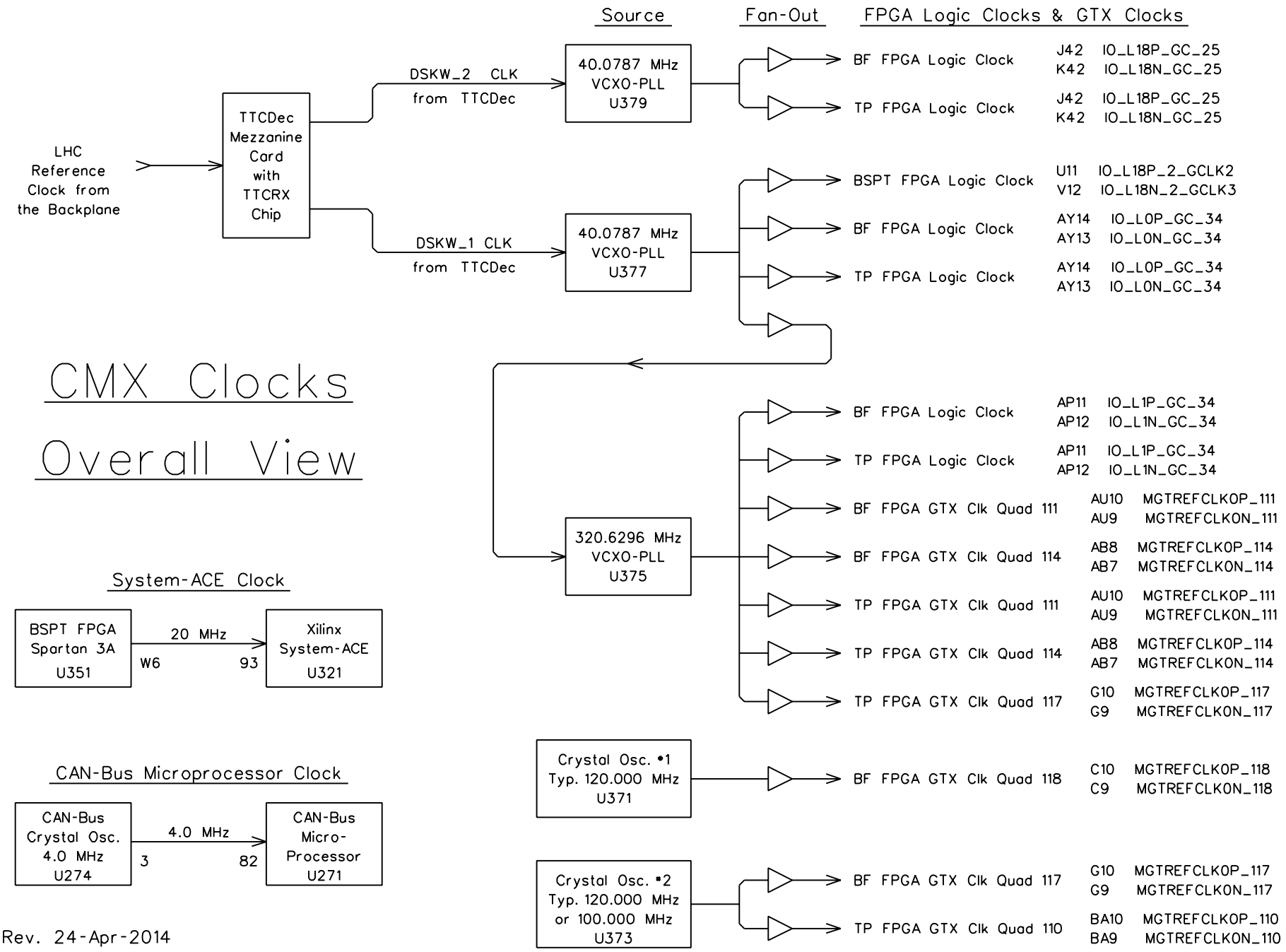
VME-OCB Management Logic in the BSPT



Logic in the BSPT's VME/OCB management section may set the following signals to static levels. For normal VME-- bus operation these signals do not need to switch levels:

VME_ADRS_AND_CTRL_RECVR_OE_B always Low
OCB_ADRS_AND_CTRL_TRNSLT_DIR always Low
VME_CTRL_RECVR_LE always Hi
BSPT_OCB_ADRS_AND_CTRL_TRNSLT_OE_B once the Virtex FPGAs are Configured then always Low

Rev. 14-Sept-2013



CMX Clocks

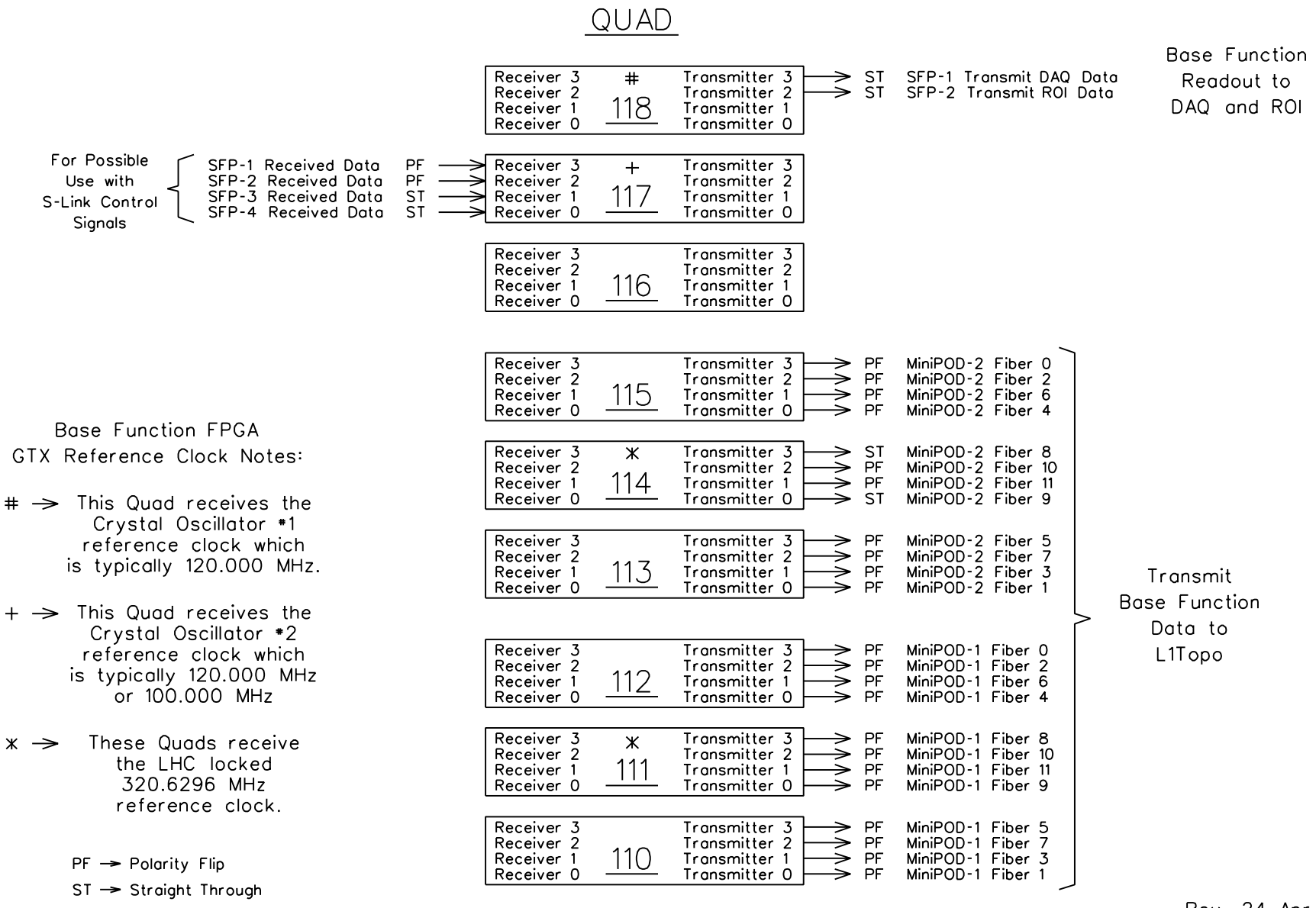
Overall View

System-ACE Clock

CAN-Bus Microprocessor Clock

Rev. 24-Apr-2014

GTX Transceivers - Base Function FPGA



Base Function FPGA
GTX Reference Clock Notes:

\# → This Quad receives the Crystal Oscillator #1 reference clock which is typically 120.000 MHz.

\+ → This Quad receives the Crystal Oscillator #2 reference clock which is typically 120.000 MHz or 100.000 MHz

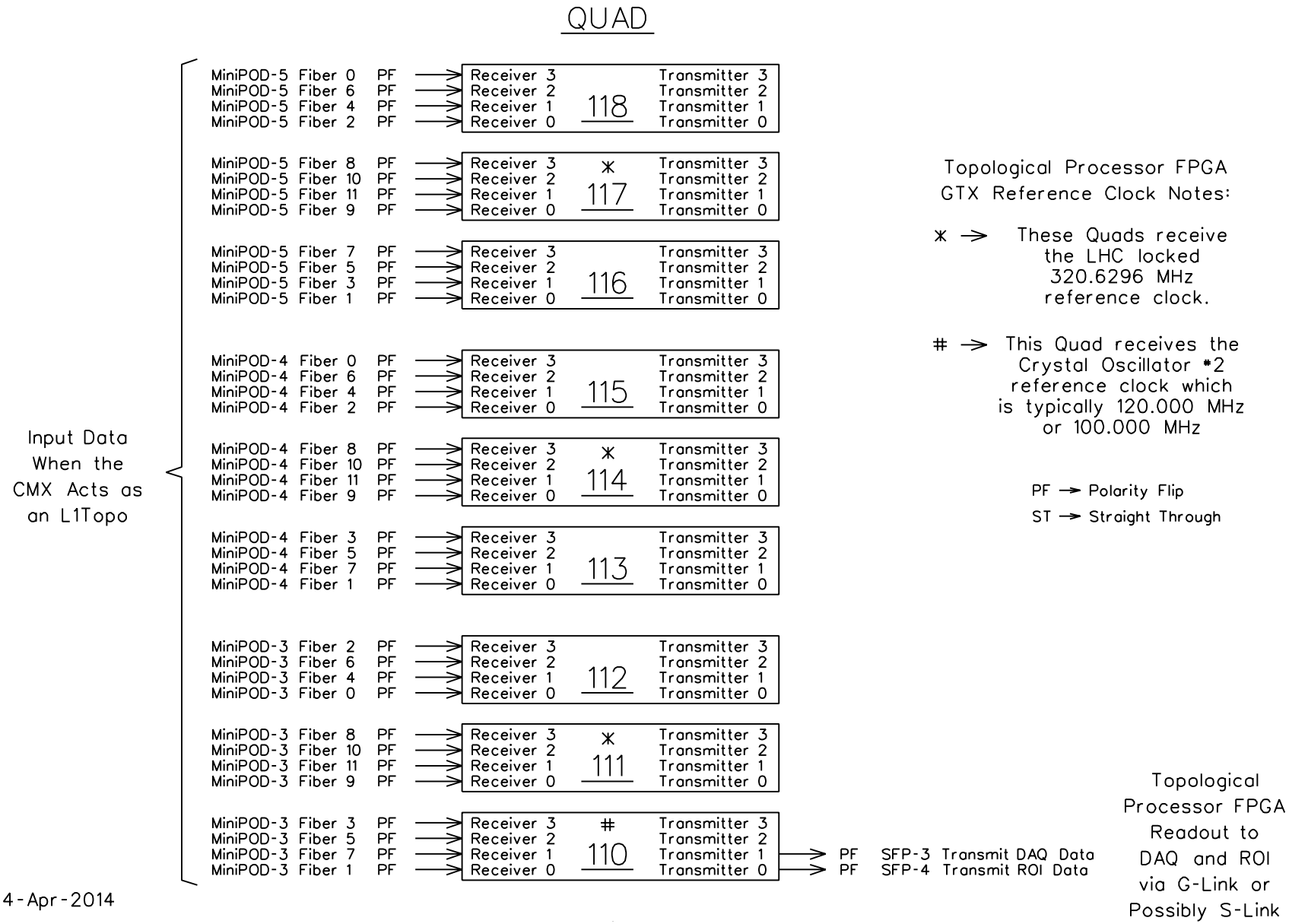
* → These Quads receive the LHC locked 320.6296 MHz reference clock.

PF → Polarity Flip

ST → Straight Through

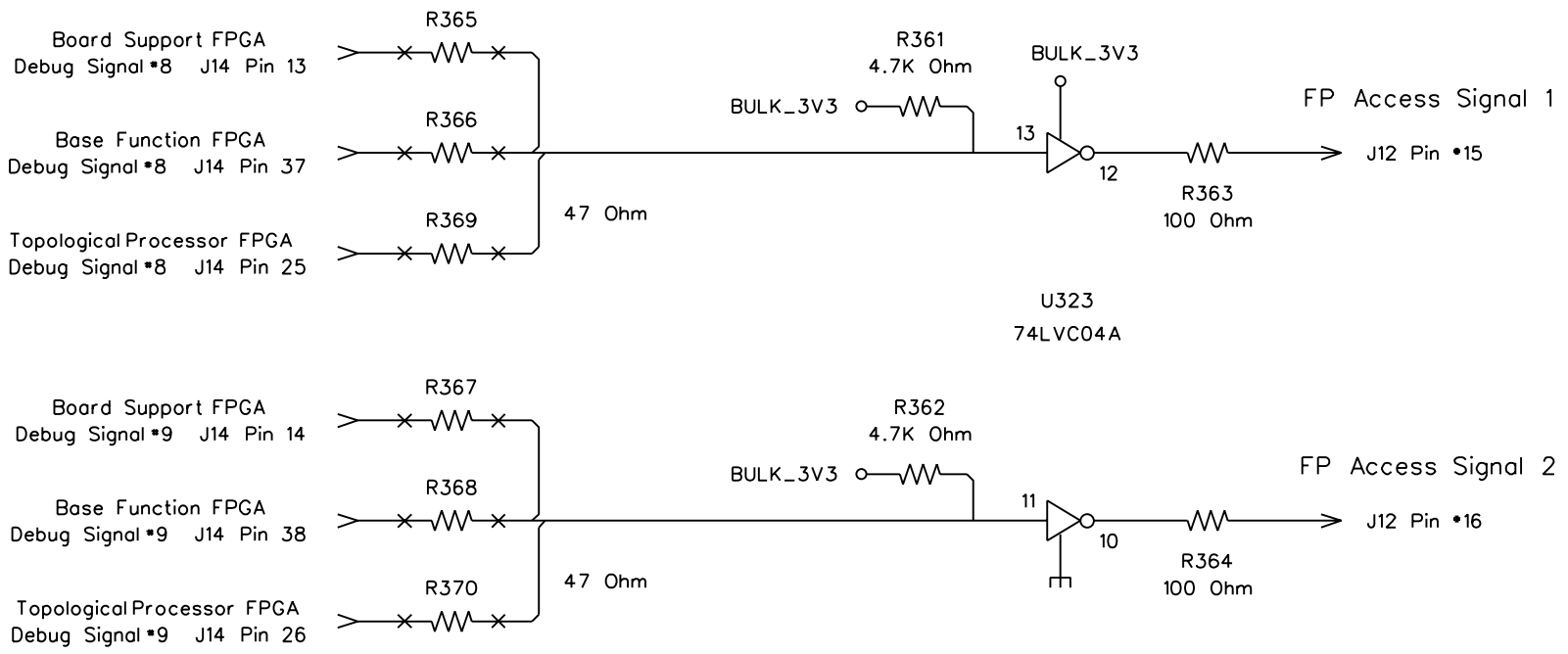
Rev. 24-Apr-2014

GTX Transceivers - Topological FPGA



Rev. 24-Apr-2014

Two Access Signals on the Front Panel



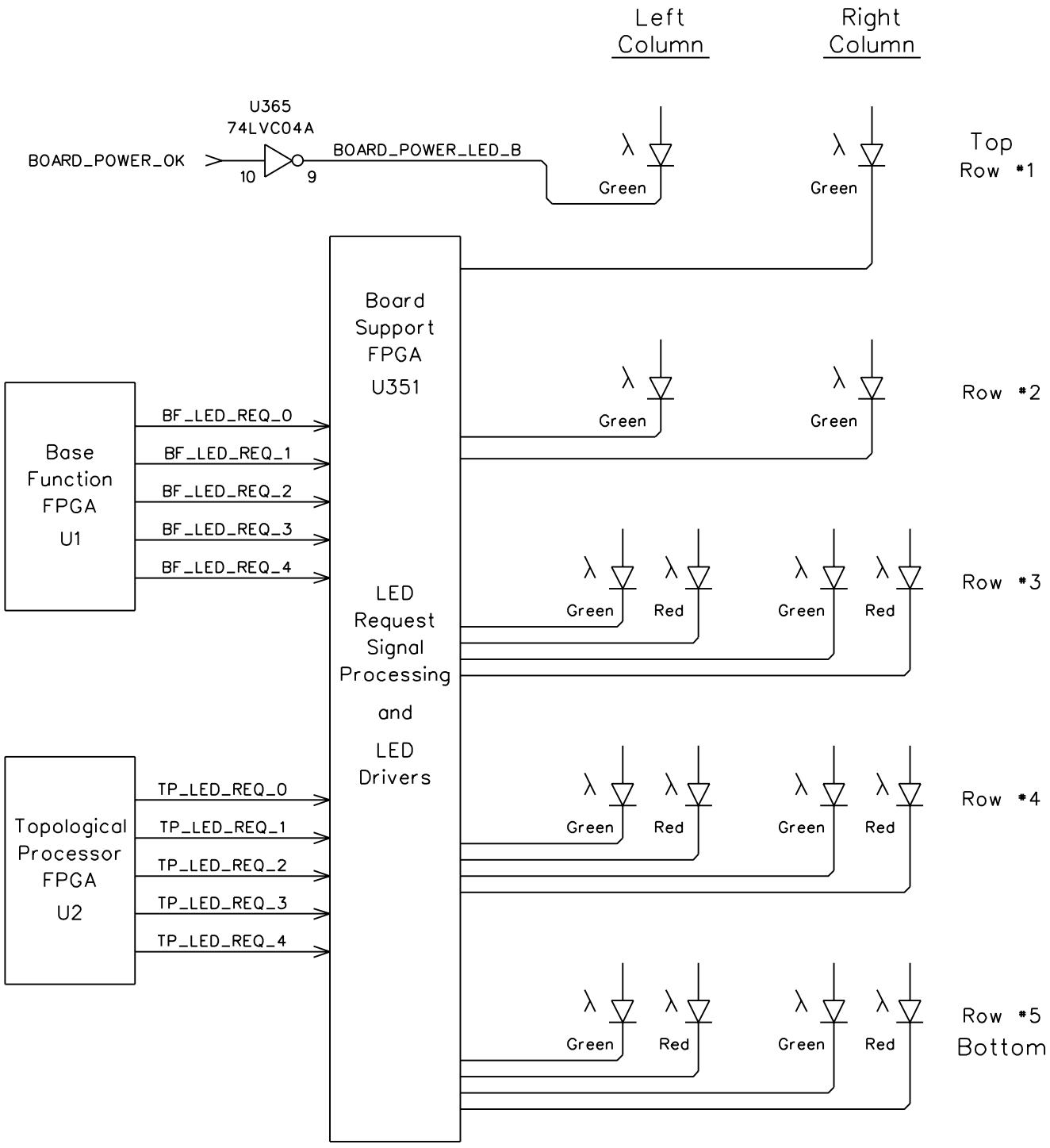
Front panel connector J12 pins 15 and 16 provide access to two buffered signals from either the: Board Support FPGA, the Base Function FPGA, or the Topological Processor FPGA.

These two front panel access signals can be used e.g.: clock monitoring, S-Link Busy, scope or logic analyzer trigger.

All J12 odd numbered pins 1 through 9 are grounds.
The 74LVC04A buffer can provide 20 mA max output.
The 74LVC04A has a logic Hi input minimum of 2.0 volts.
The Xilinx 2.5V CMOS output logic Hi is a minimum of 2.1 volts.
The Xilinx I/O pin clamp diode can handle 10 mA max.

Rev. 19-Sept-2013

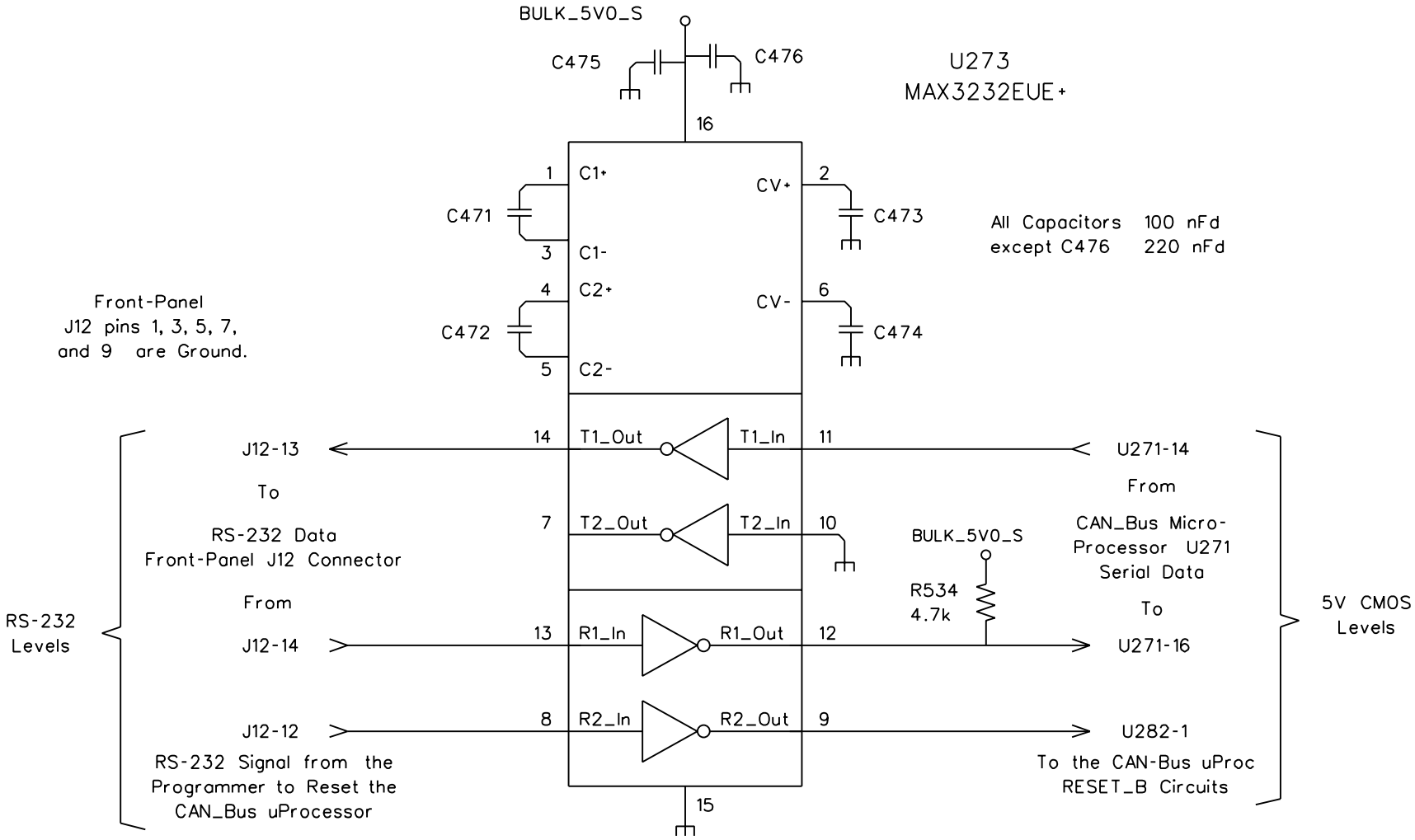
Front Panel Dual-LEDs



All LED Anodes are connected to BULK_3V3 through 680 Ohm Resistors.

Rev. 1-July-2013

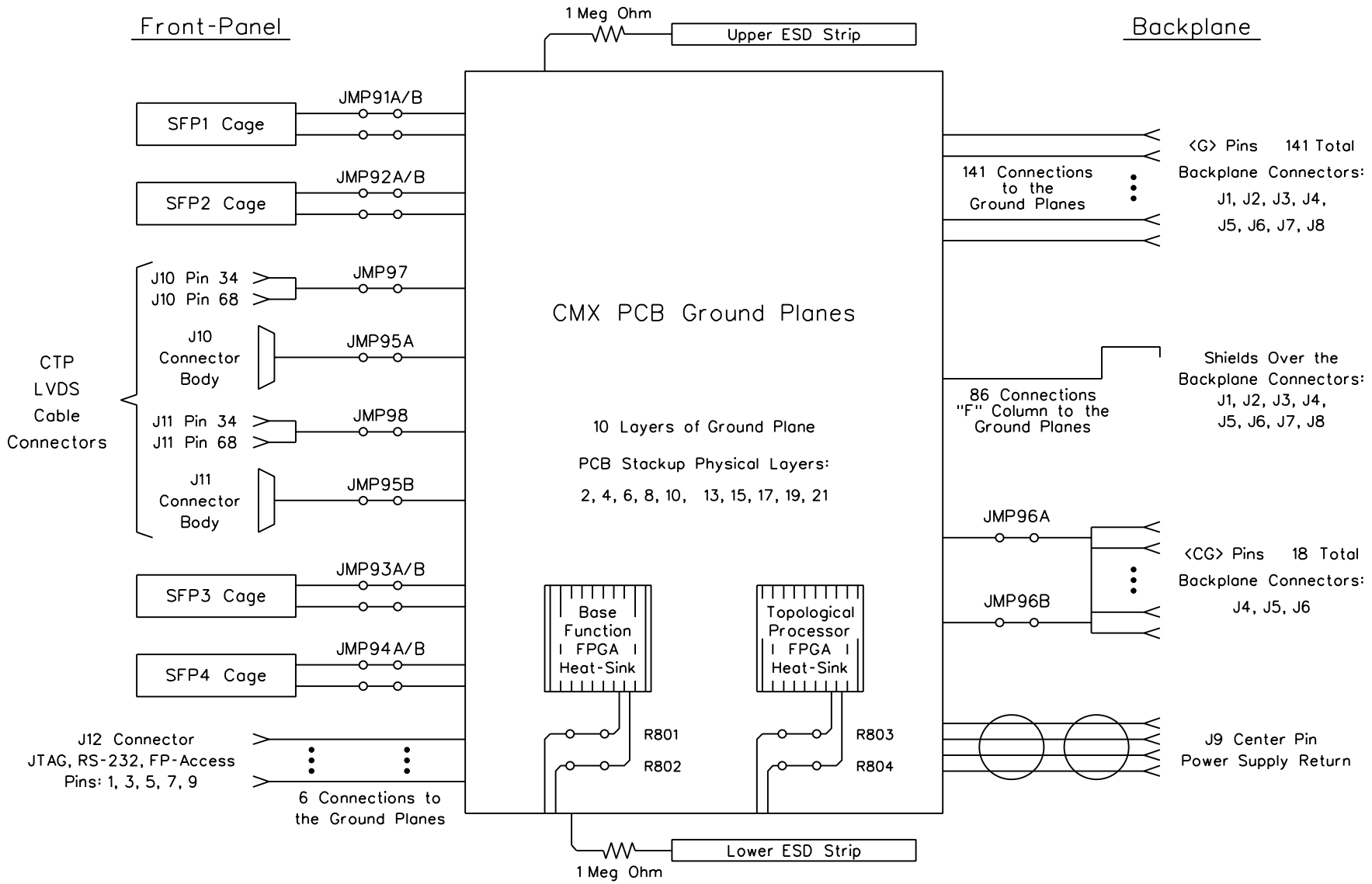
RS-232 Interface to the CAN-Bus Micro-Controller



Both the transmitters and receivers are level inverting.
The receiver inputs have internal 5k Ohm pull-down resistors.

Rev. 24-July-2013

Ground Connections on the CMX Card



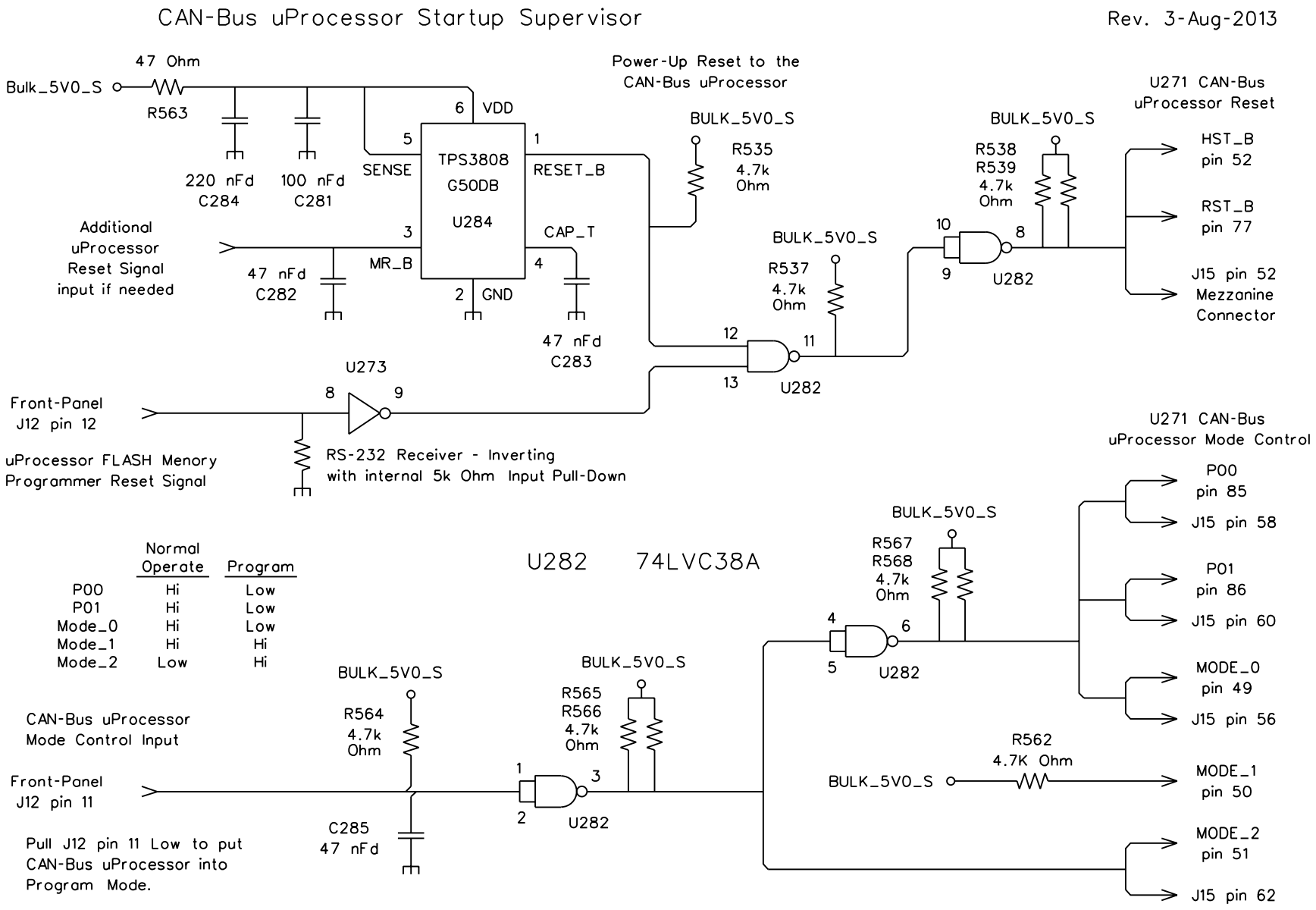
The front-panel, stiffener bars, and guide pin receptacle are electrically connected to the bodies of connectors J10 and J11.

During assembly the SFP Cages may be electrically connected to or insulated from the front-panel.

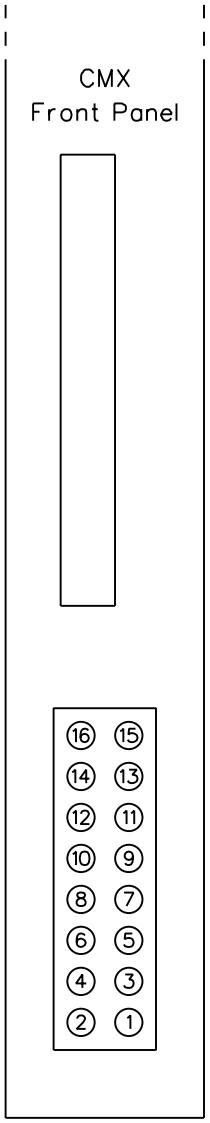
All jumpers shown in this drawing may be: open circuits, Zero-Ohm jumpers, or appropriate value 0805 resistors as required to control ground loops.

Rev. 14-Aug-2013

CAN-Bus uProcessor Reset and Mode Signals



Front Panel J12 Connector and Cables



Compact Flash Menory Socket

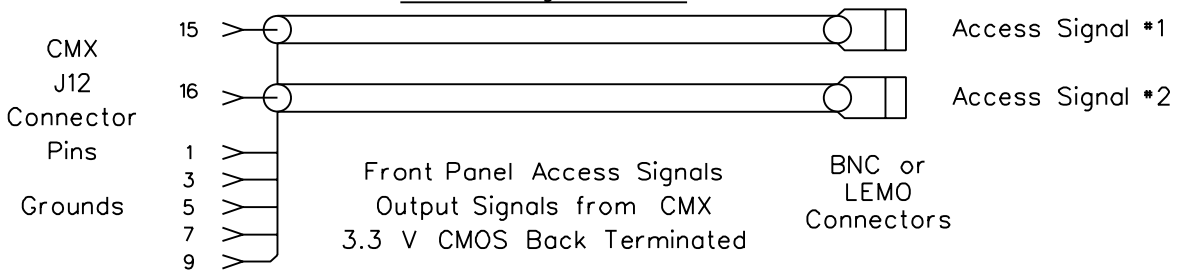
Lower Section of the CMX Front Panel

J12 Connector

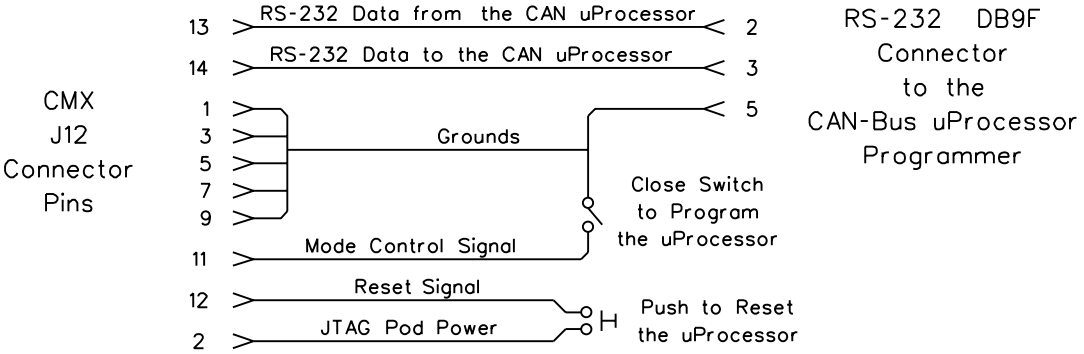
Access Signals, CAN-Bus uProc Programming, and JTAG

Rev. 21-May-2014

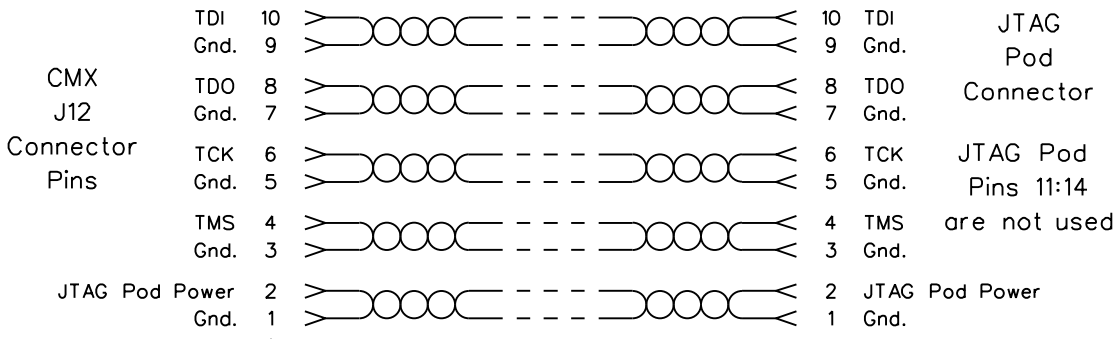
Access Signal Cable



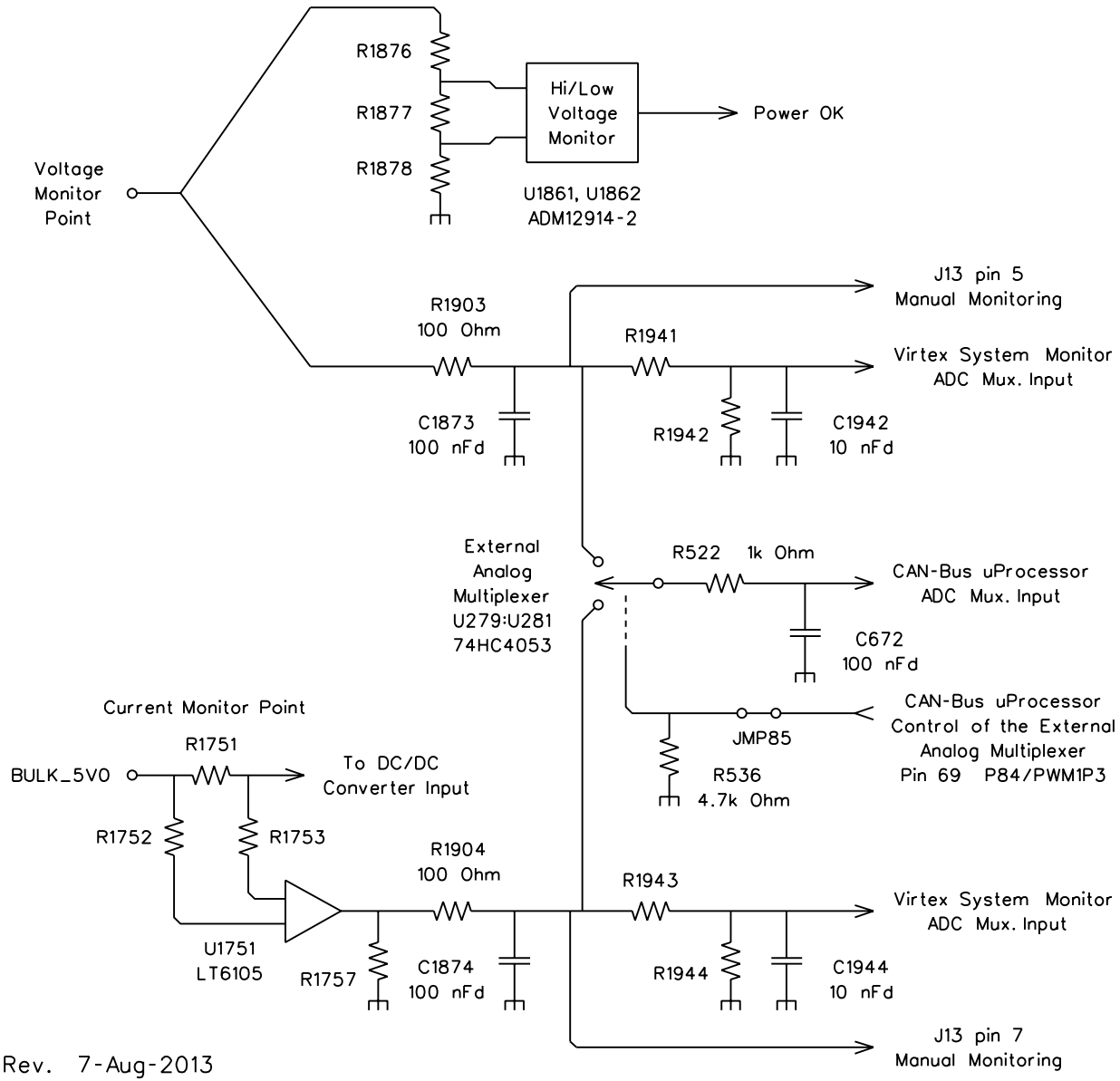
CAN-Bus uProcessor Programming Cable



JTAG Pod Twisted-Pair Cable



Voltage and Current Monitoring Analog Circuits



Rev. 7-Aug-2013

Notes:

The reference designators and pin numbers shown are for the Base Function FPGA Core power supply.

The Voltage and Current Monitoring of the other 6 power supplies is similar.

ADC inputs to the CAN-Bus uProcessor are 4.096 Volts full-scale.

The ADC Inputs to the Virtex System Monitor are 1.0 Volts full-scale. R1941 through R1944 must scale the monitored signal to fit within this 1.0V ADC input range.

R1751, R1752, R1753, and R1757 together set the calibration of the current monitoring signal.

R1752 must equal R1753. Monitor signal voltage equals Amps into the DC/DC Converter times R1751 times R1757 divided by R1752. LT6105 maximum output current is 1 mA.

R1876, R1877, and R1878 together set the Hi and Low thresholds of the BF_CORE component of the overall CMX Power OK signal.

The ADM12914-2 Hi/Low Supervisor comparators have an internal 0.500 Volt reference.

With jumper JMP85 installed the external Analog Multipoexer is controlled by the signal from the CAN-Bus uProcessor.

With jumper JMP85 removed the External Analog Multiplexer defaults to the Voltage Monitor signals