Upgrading the ATLAS Level-1 Calorimeter Trigger using Topological Information

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TWEPP 2010, Aachen, Germany, 20-24 September 2010

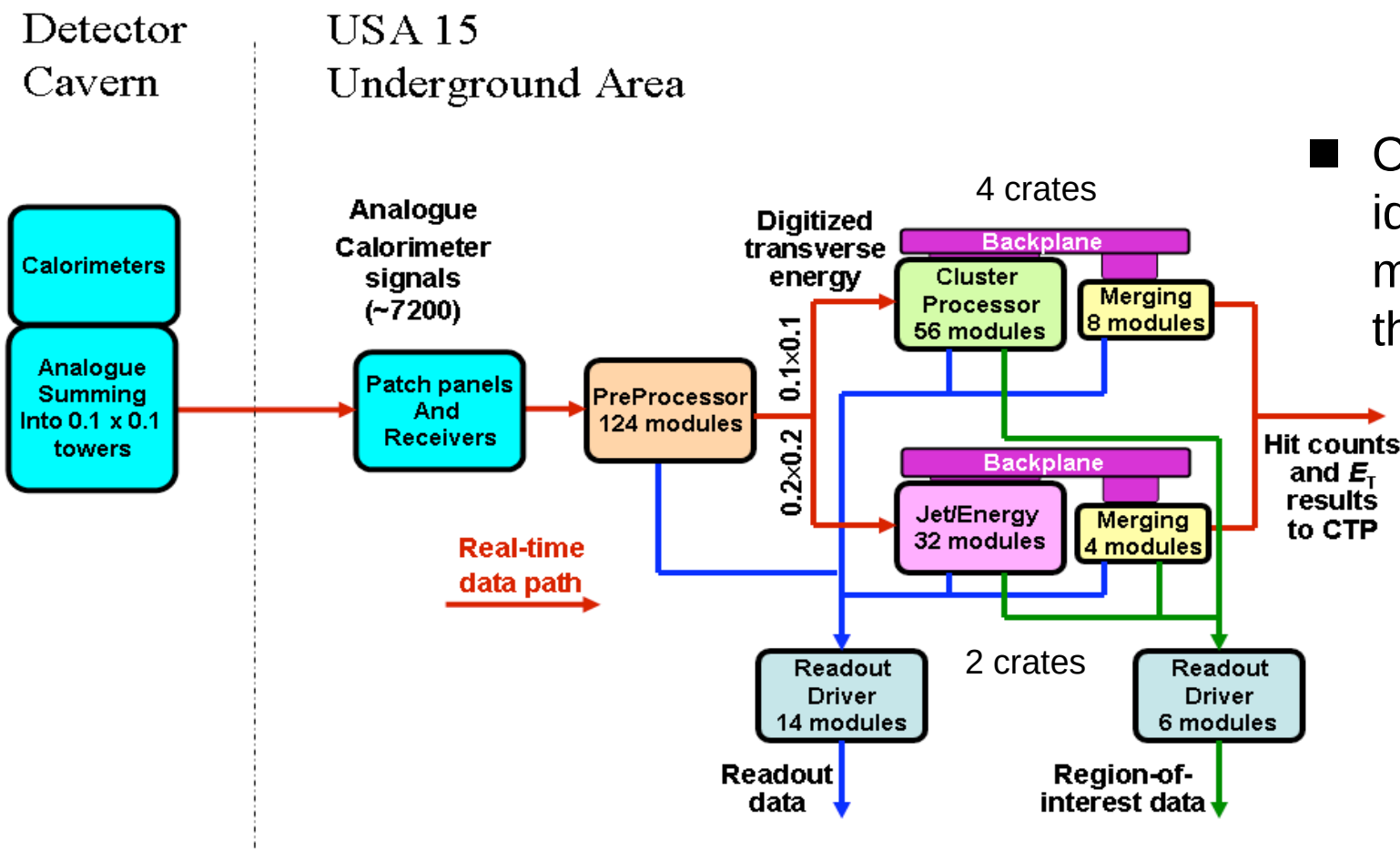
On behalf of the ATLAS TDAQ Collaboration

ATLAS TDAQ Collaboration, The ATLAS Trigger/DAQ Authorlist, version 4.0,
ATL-DAQ-PUB-2010-002, CERN, Geneva, 14 May 2010
http://cdsweb.cern.ch/record/1265604

Outline

- Current L1 Calorimeter trigger system, limitations
- New hardware for topology functionality (CMM++)
  - Functionalities
  - Algorithms
  - Development scenario
- Recent R&D
  - Backplane data transfer rates
  - Latency survey
  - Optical link studies
  - Technology demonstrator
  - Firmware studies
- Summary/conclusions

Current L1 Calorimeter trigger system



- Counts of identified objects meeting specified thresholds.

- Region of Interest (ROI) information read-out only on L1Accept.

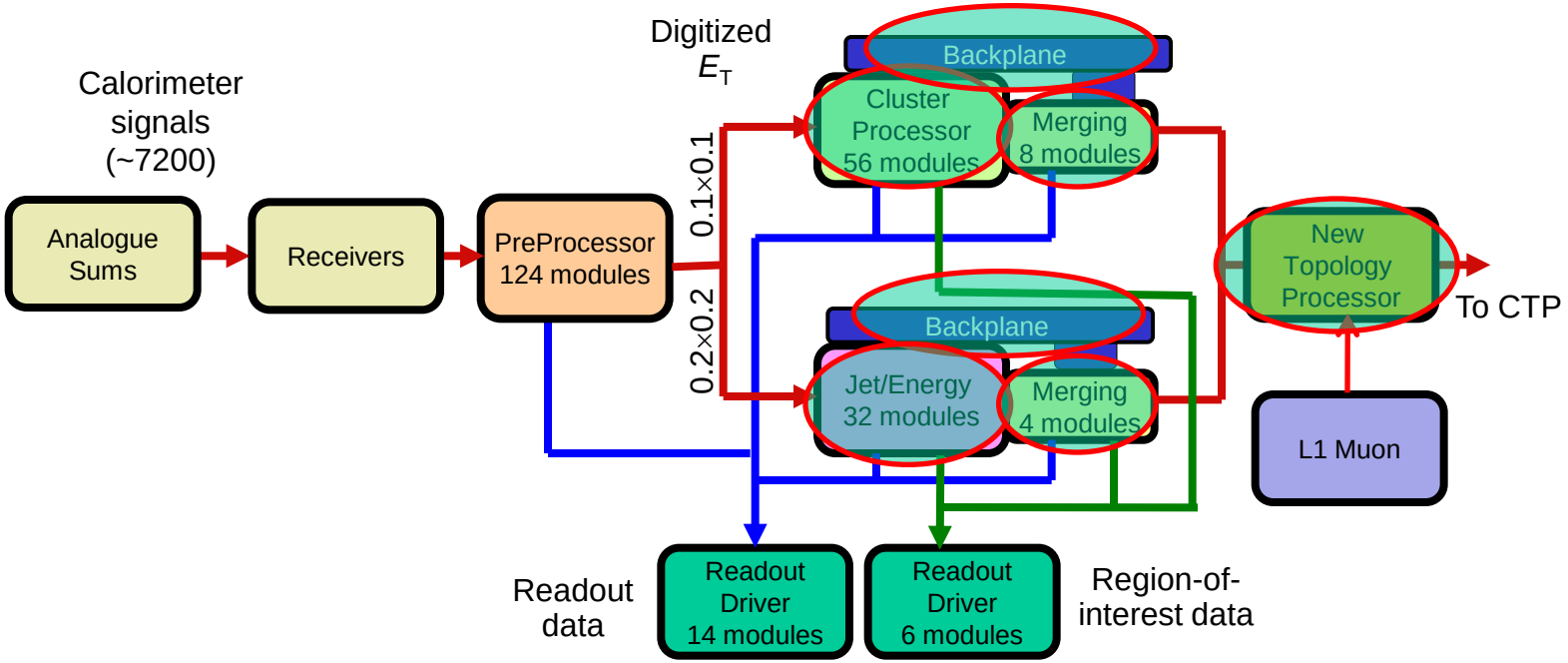
Limitations of current system

- Based only on counts of objects
- Jets and em/tau clusters identified in different subsystems
  - But clusters can also look like jets
  - No way to distinguish when this happens
- Possible solution
  - Include Jet/cluster positions in real time data path
  - Use this information to add topology-based algorithms at Level 1

Ideas on limited short-term topological upgrade

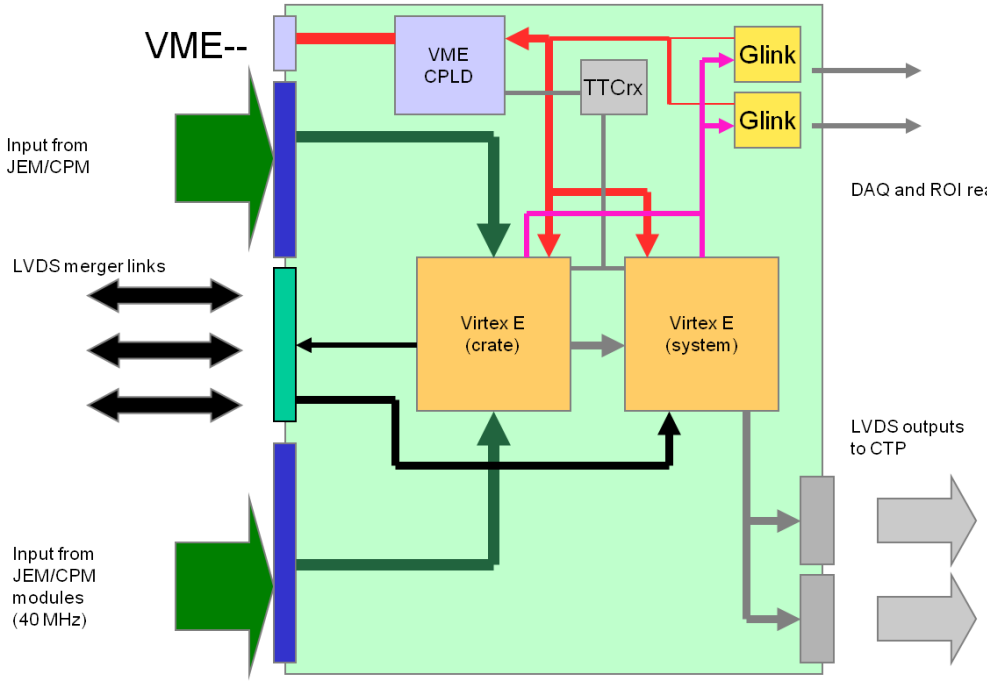
- The current L1Calo will remain mainly unchanged for next few years
  - Remain compatible with rest of running system.
  - Hardware components already 5 - 7 years old, not much freedom for modifications
- MC simulations indicate some performance degradation of multiplicity-only algorithms at 1-2E34
- A promising solution: drive backplane at higher speed to add ROI positions to the real-time data path, enabling new algorithms based on event topology

Modifications required for limited upgrade



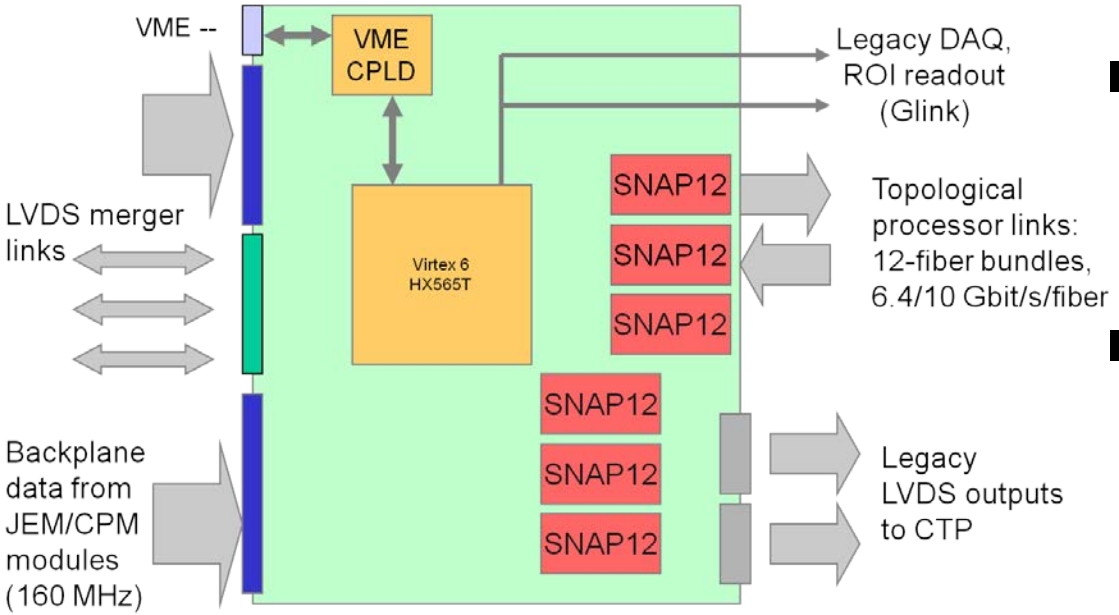
- Modify firmware in processor modules
- Increase data transfer rate over crate backplane (40 Mbit/s -> 160 Mbit/s)
- Replace merging modules with upgraded hardware
- Eventual Topology Processor (TP)

Current CMM (Common Merger Module)



- "Crate" FPGA on each CMM receives backplane data, produces crate/wide sums of indentified features
- "System" FPGA collects crate results over LVDS cables, sends trigger output to CTP.
- On L1A, data and ROI readout via G-Links
- All CMMs identical
  - Several different firmware versions
  - Xilinx SystemAce

CMM++ functionality



- Complete backward compatibility
- Feature collection from upgraded CPM/JEM modules and transmitted to toplogy processor
- Supports multiple optical tx and/or rx modules
  - TX: duplicate outputs to multiple processor nodes
  - RX: Data merging for ev. internal topology processing without TP

Topology algorithms study

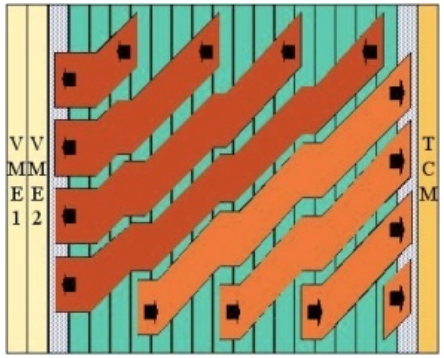
- Examples using local topology information (single calo quadrant)
  - Identify spatial overlap between e/tau clusters and jets
  - Use local jet Et sum to estimate energy of overlapping e/tau object
    - ⇨ Requires jet energies to be added to real time data path
- Examples using global topology
  - Non back-to-back jets
  - Rapidity gaps in eta and/or phi
  - Invariant transverse mass calculations
  - Jet sphericity
- Initial studies look promising
- N.B. CMM++ only option may limit global topology capabilities

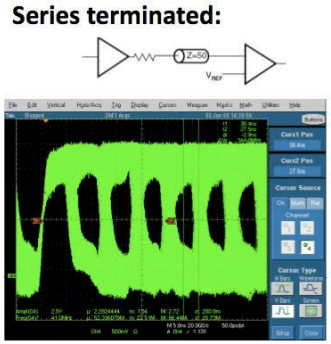
CMM++ development scenario

- Hardware design with all present interfaces plus optical links for the new topological processor, one large FPGA
- Adapt current CMM firmware to the new hardware for initial use, incrementally add new functionality
- Upgrade CPM/JEM and CMM++ modules firmware for new data format and 160 Mb/s data transfer
- Two topology processing scenarios:
  - Separate TP processor crate
  - One CMM++ in system provides limited topological functionality if final TP not yet available

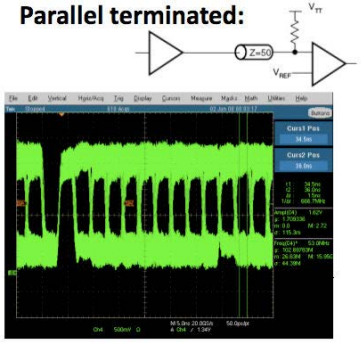
JEM-CMM backplane data transfer

- Each CPM/JEM is sourcing 50 lines into two mergers at 40 Mbit/s
- Scope shots of JEM signals over the longest backplane track





160 Mbits, CMOS 2.5V



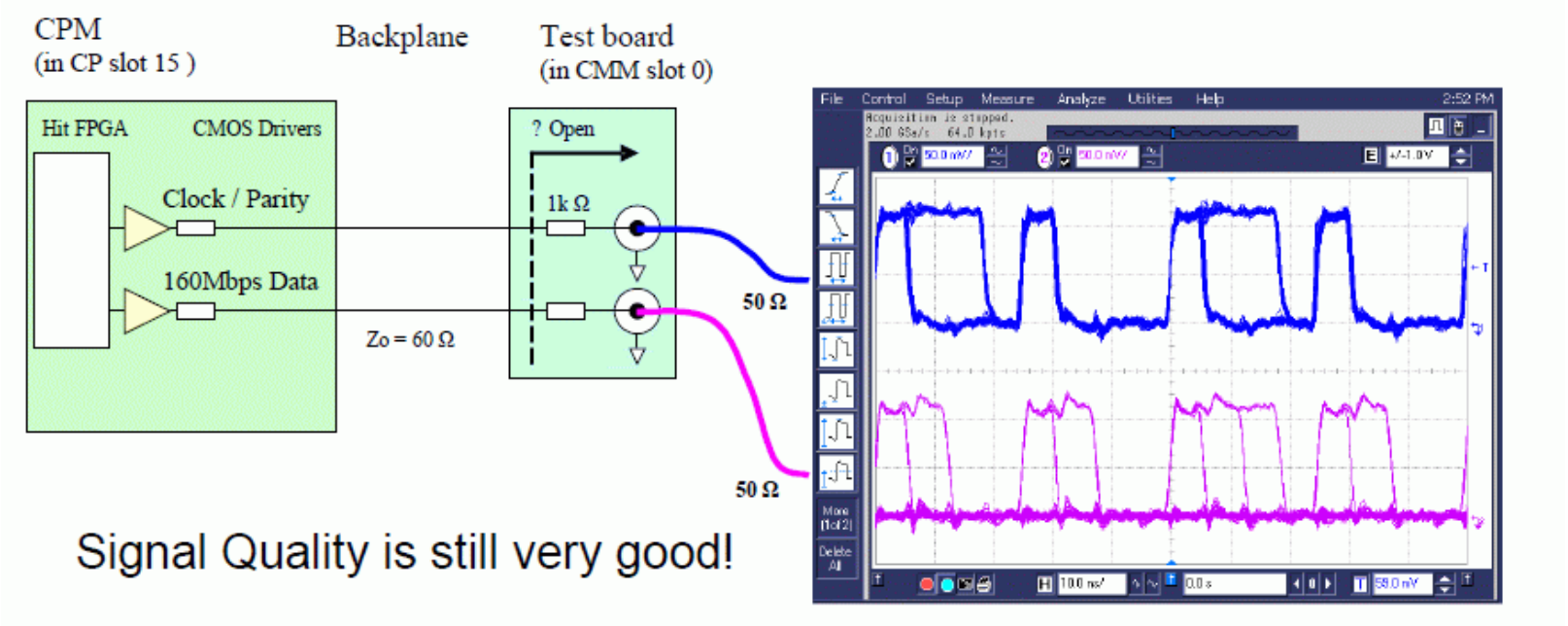
320 Mbits, CMOS 2.5V

- Backplane tester (BLT) module was built:
  - Data from all CPM/JEM modules
    - ⇨ 400 lines, individually deskewed
    - ⇨ Forwarded clock, sink terminated
  - Eye > 3.7ns @ 160Mb/s
  - Bit error rate tests on backplane data

BLT

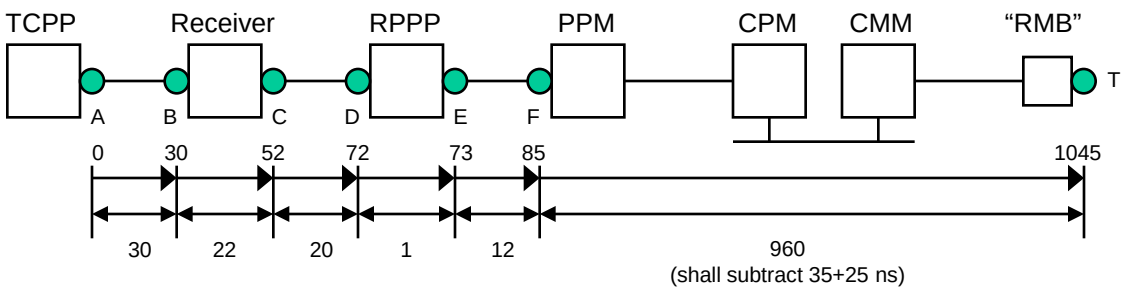
CPM-CMM backplane data transfer

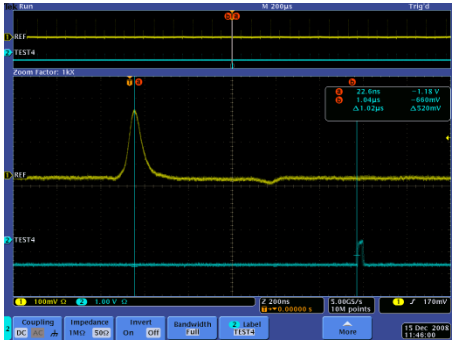
- CPM tests demonstrate160 Mbit/s with reasonable signal quality
  - Test board alows to probe backplane signals in CMM slot
  - Termination on CMM side improves signal quality,
    - ⇨ but increases dissipated power in CMM slot (a problem if done inside FPGA)
  - Also tested signals with termination on source only



L1Calo trigger latency

- Latency measurements in the complete L1Calo system:





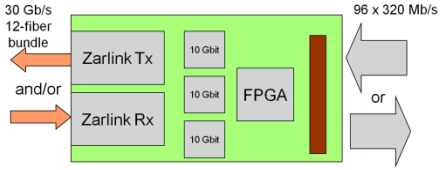
- Detailed breakdown:

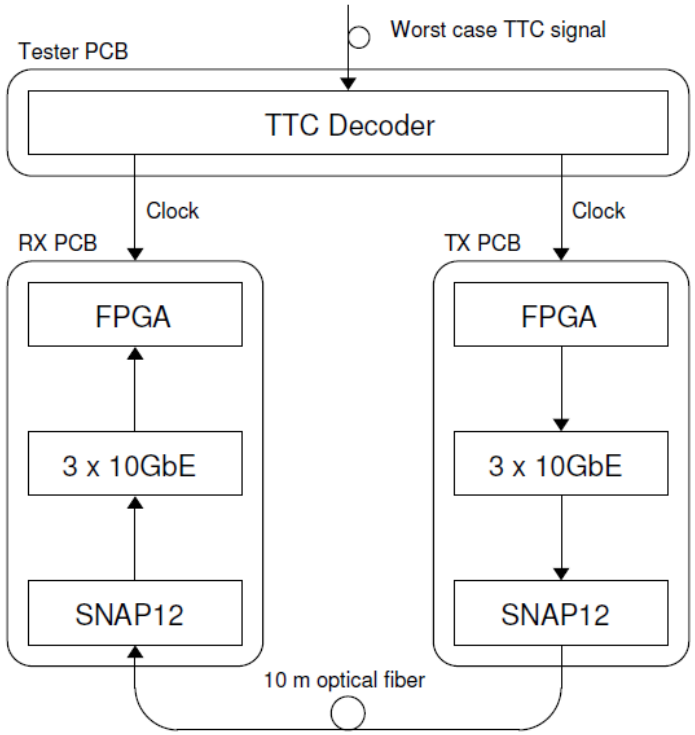
- Part of total L1 latency!

	2006			USA15			3150	
CALORIMETER TRIGGER	ns	BCs		ns	BCs		ns	BCs
PreProcessor								
Preprocessor to CP LVDS bit-stream	350.0							
Cabling to CPM (11.4 m * 5 nsec/m)	57.5	16.3						16.0
CPM								
CPM logic	269.0							
Backplane	2.5	10.9						13.0
CMM								
Crate+ system CMM logic	141.0	5.6						7.0
Total PPM-CPM-CMM	820.0	**32.8**		900.0	**36.0**			**36.0**
PreProcessor								
Preprocessor to JEP LVDS bit-stream	375.0							
Cabling to JEM (10.2 m * 5 nsec/m)	57.5	17.3						17.0
JEM								
JEM logic	257.0							
Backplane	2.5	10.4						7.0
CMM								
Crate+ system CMM logic	141.0	5.6						8.0
Total PPM-JEM-CMM	833.0	**33.3**						**32.0**

10 Gb ethernet-based optical link

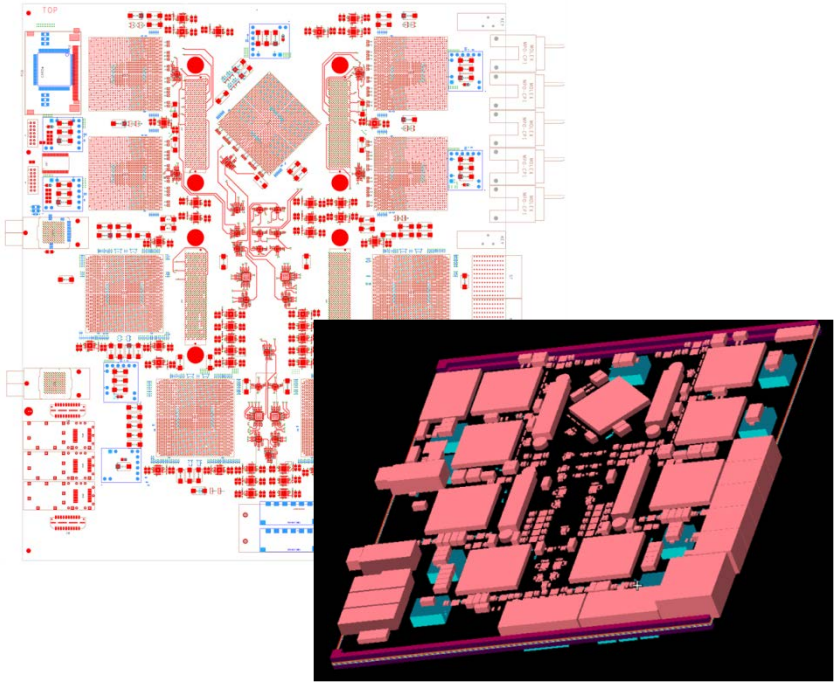
Link board prototype

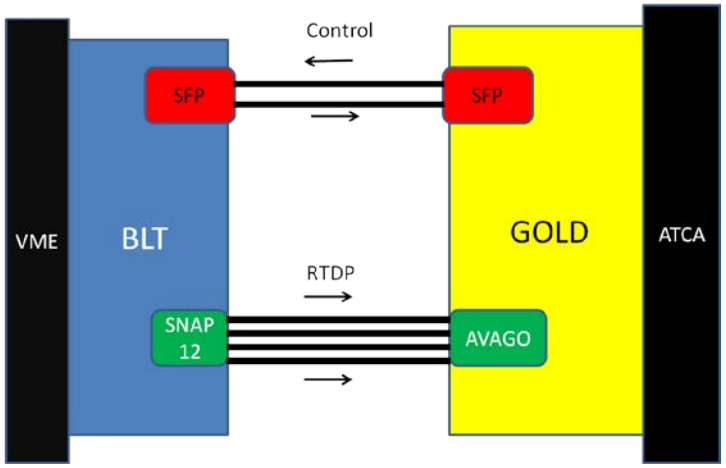




- Inexpensive 30 Gbit/s link using commercial components
  - Xilinx Spartan-3 FPGA
  - 10Gb Enet transceiver TLK3114SC (XAUI)
  - SNAP12 Tx/Rx pair
- Can run links synchronously with LHC clock
  - Send alignment characters in some LHC bunch gaps for link maintenance
- Can drive multi/Gbit links with TTCrx clock outputs
  - Reduce jitter with LMK03033CISQ clock conditioner

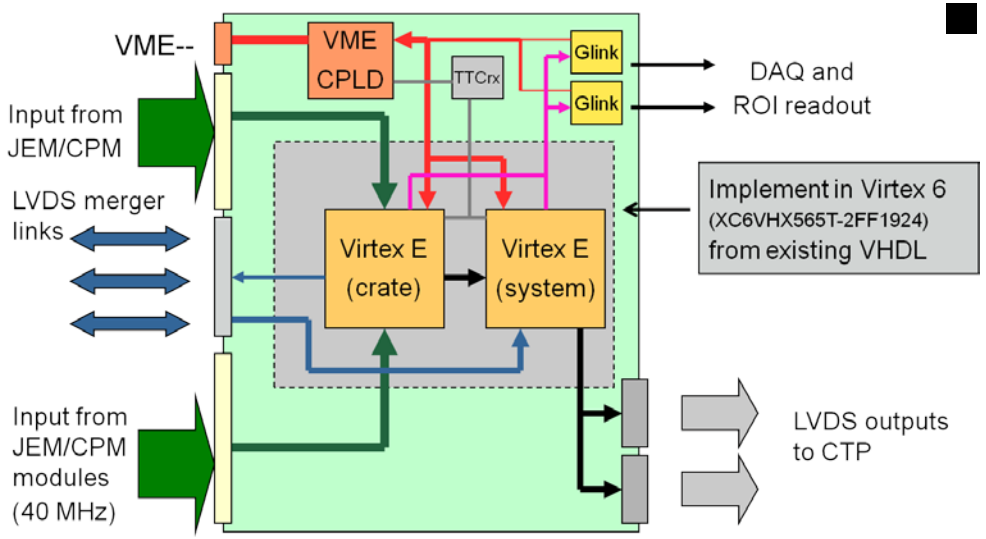
Technology demonstrator project





- GOLD (Generic Optical Link Demonstrator)
- New, state-of-art new FPGAs
  - Xilinx XC6VLXxxxT
  - Xilinx XC6VHX380T
    - ⇨ 640 I/O, 48 GTX, 24 GTH
- Optical links (6.4-10 Gbit/s)
  - SNAP12 and
  - Avago optolinks
  - Optical backplane connectors
- ATCA
  - Backplane/form factor
  - Power distribution and local conversion

Porting the existing CMM firmware



- Available I/O (*not including transceivers*): 640 pins
- Real-time data path:
  - Backplane input:
  - Cables (3 x 25):
  - CTP output (2 x 33):
- Control and timing:
  - VME-- from CPLD
  - TTC (L1A, BCR, deskew 1+2)
  - Crystal clock
  - clrpe, reset, reset_dll, plybk_en
- Readout:
  - Glink data outputs 2 x 20
  - DAV pins
- Indicator LEDs :
- TOTAL: 635 / 640
  - *Note: this is after removing spare TTL and test ports!*

400
+75
+66 = 541 pins
35
+4
+1
+4 = 44 pins
40
2 = 42 pins
8 + 8 pins
635

- Aim: port Jet CMM firmware to target Virtex 6 device:
  - Use existing VHDL with minimal changes
  - Update architecture-specific features
  - Estimate I/O requirements
  - Realistic user constraint file (UCF) for ISE timing simulation
- Results so far
  - Existing VHDL ports easily, uses ~2% of available resources
  - By emulating Glink in FPGA, can keep I/O count below 600/640 pins
    - ⇨ Not including dedicated multi-Gbit links

Summary/conclusions

- Want to improve existing L1Calo system
  - Maintain trigger quality up to 1-2E34 luminocity
  - Provide best possible algorithms for ATLAS
- Add topological trigger capability
  - Minimal changes to existing system
  - Low impact on other ATLAS components
- R&D projects/studies well under way
  - Backplane data transfer rates
  - Technology demonstrator
  - Firmware studies
- Looks promising…