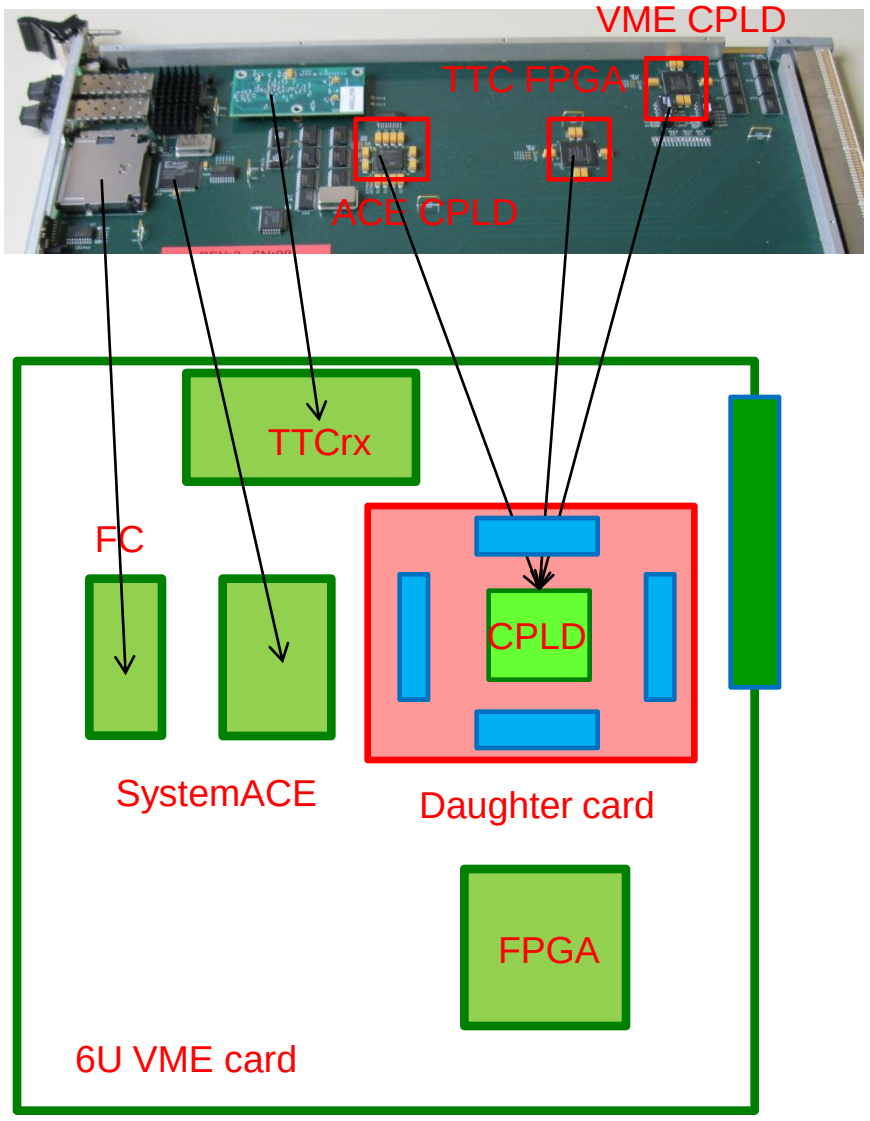
# VME test card for VME/ACE/TTC interface for CMX

Yuri Ermoline

Level-1 Calorimeter Trigger General Meeting, CERN

December 15, 2011

# Initial idea




- VME/TTC/ACE parts of CMM
  - 2 CPLDs + 1 FPGA
- Redesign HW with new components
  - Parts obsoleteness
- Merge VHDL a single design
  - FW porting on new HW
  - Fit design into (single?) newer XILINX **CPLD**
- Implement on a daughter card
  - Different implementations
  - Use later on CMX
- 6U VME test card for
  - Hardware implementation
  - FPGA re-configuration
  - Software

# Preliminary studies

- Two CPLDs merged in one design and compiled in new CPLD
  - XILINX CoolRunner-II XC2C256-6-PQ208
  - Macrocells: 160/256(63%); Pins: 137/173(80%)
- TTC FPGA complied in XILINX Spartan-3AN XC3S200AN-FTG256
  - Slices: 131/1792(7%); Pins: 69/195(70%)
  - TTC FPGA use internal memory and can't be complied in CPLD
- 2 CPLDs and TTC FPGA merged in a single FPGA design
  - Spartan-3AN XC3S200AN-FTG256
  - Slices: 286/1792(15%); Pins: 165/195(84%)
- Do we need to keep the CPLD
  - safeguard against a malfunction in the FPGA configuration process
- Single FPGA implementation
  - Configuration from EEPROM
  - Configuration from internal flash memory (Spartan-3AN)
  - Configuration from Flash Card (System ACE)

# Next steps

- Development process:
  - CADENCE schematics of the 6U VME card based on CMM schematics
  - Launch PCB layout/production/assembly
  - Design daughter card(s)
  - In parallel work on FW
- Different daughter card implementations
  - CPLD (CoolRunner-II) + FPGA (Spartan-3AN)
  - Single FPGA (Spartan-3AN)
- Test of FPGA configuration failure
  - Procedure?
- Re-configuration
  - On time-out?
  - Via DCS?