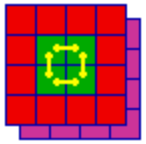
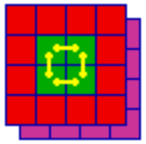


CMX: Update on status and planning

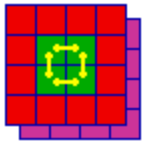
Yuri Ermoline, Wojciech Fedorko @CERN
Dan Edmunds, Philippe Laurens, Chip Brock @MSU
Michigan State University
7-Mar-2012

MICHIGAN STATE
UNIVERSITY



CMX development work on 3 fronts

1. VME/ACE/TTC interface “daughter card” @CERN
   - Yuri
2. CMX input module firmware @CERN
   - Wojtek and Yuri
3. Engineering @MSU
   - Philippe, Dan, and Chip

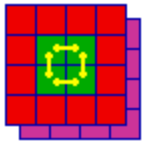


Initial CMX design studies phase

Addressed **two main questions:**

1) FPGA choice for implementing the Base-CMX functionality

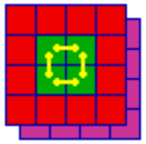
2) Strategies, costs and risks for adding Topological Processing capability to the CMX platform



Definition: **Base-CMX** functionality

1) **All of CMM functionality** (both Crate CMM and System CMM)
   - Receive and process 400 JEM/CPM input signals (@4x CMM rate)
   - All Crate CMXs send local summary to their System CMX through backplane connectors over LVDS cables (@higher rate than CMM)
   - System CMXs form and send triggering information to CTP over LVDS cables (same as CMM)
   - all CMXs send ROI and DAQ information over G-links (same as CMM)

2) **Send JEM/CPM info out to a TP** optically
   - using 12-fiber ribbons
   - with some level of duplication (at least 2x copies sent)
   - 6.4Gbps nominally sufficient for all raw data on **one** 12-fiber ribbon
   - also possible to send zero-suppressed data on less fibers

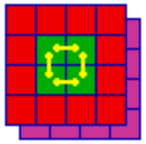


Definition: **TP-CMX** functionality

Topological Processing capability **on CMX platform**

1) Receive optical inputs from some/all 12x CMXs
2) Run multiple Topological Algorithms
3) Send Topological Triggering Information to CTP

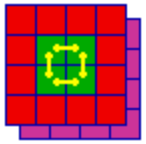
- TP-CMX functionality is needed if dedicated TP is not built, or availability delayed, or as additional safety/backup
- The CMX platform could then be asked to provide some generic TP functionality
- Or **added flexibility**: "TP-CMX" capability could also be used to support future upgrades e.g. new Base-CMX algorithms needing a larger volume of Crate->System communication



Initial CMX design studies phase

- Started with guidance from **Stockholm Review**
  - Use Xilinx Virtex 6
  - Design for **6.4Gb** optical outputs
  - Implement G-link encoding on FGPA
  - → Generally **be conservative** to deliver on time

- Conclusions from Feb 2012 **Technical Workshop at RAL**
  - Recommend **Two FPGAs**: one for Base-CMX + one for TP-CMX function
  - **Two CMX types**: e.g. an implementation might be 1 (plus spares) with 2 FPGAs, 11 (plus spares) with 1 FPGA
  - Plan for operating the Crate CMX to System CMX LVDS cables at up to 4x current speed, i.e. 160Mbps → may require new cables or RTMs
  - Base-CMX function should provide **2x** 12-fiber **output** ribbons
  - TP-CMX function should receive **3x** 12-fiber **input** ribbons



Dual FPGA: Base-CMX and TP-CMX

If TP-CMX functionality is desired on CMX platform → use two FPGAs:

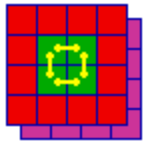
- Base-CMX and TP-CMX are totally separate functions:
  - logically don't share inputs or outputs
  - operationally in separate latency time segments
- TP-CMX needs access to CTP output → simply do not choose a System CMX to operate as a TP CMX

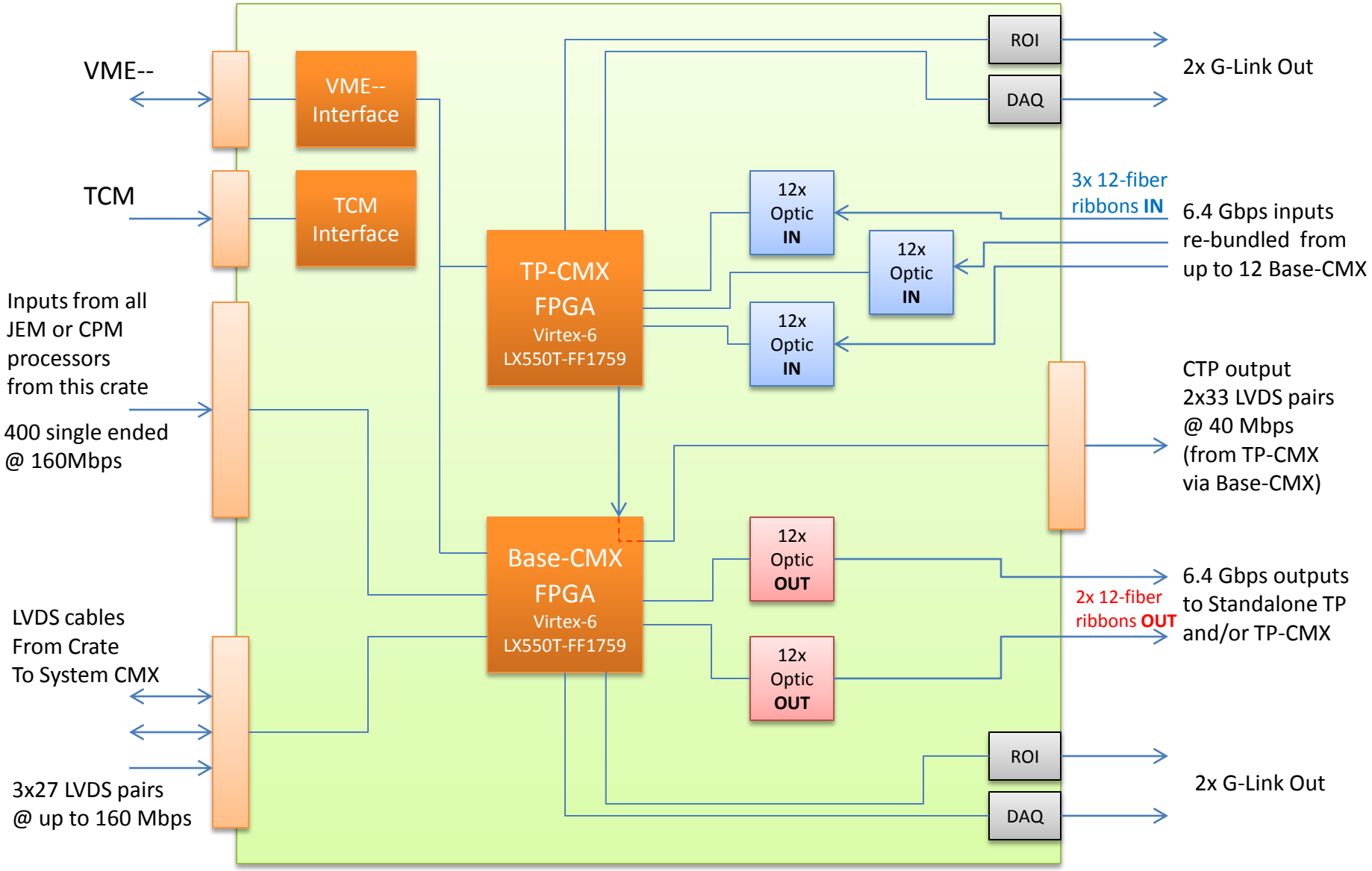
- **Separate** Base-CMX from TP-CMX **firmware** → **Easier commissioning**, easier **operation**, easier firmware **management** and easier updates

- Use smaller Virtex 6 package LX550T-FF1759 for both FPGAs
- Layout made simpler by separating routing challenges

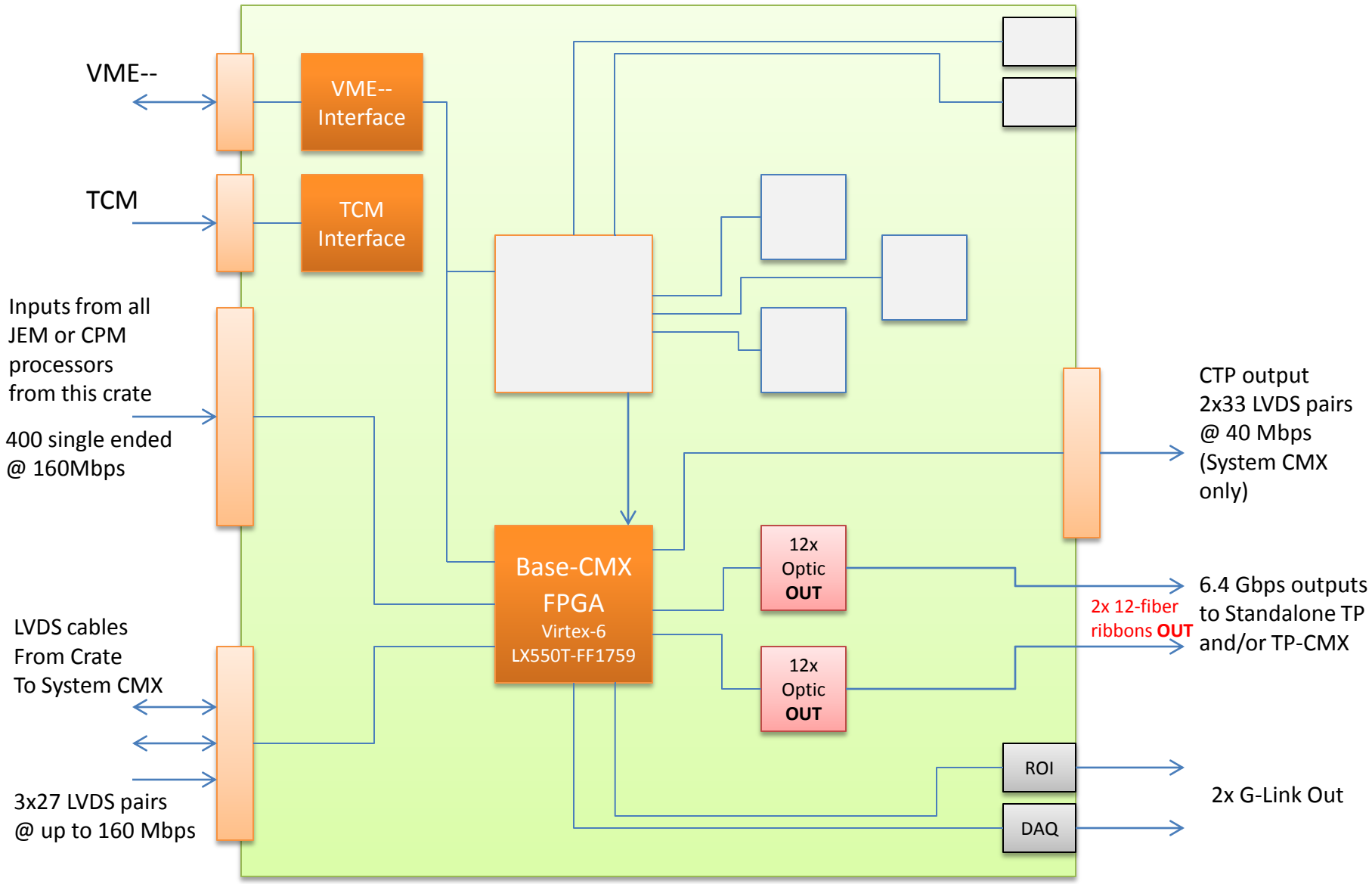
- A board TP CMX capability was originally only an option.
  - Accepting the RAL recommendations with Two CMX types will require only a modest increment in cost.

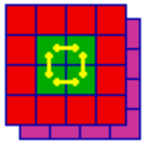
CMX Card with Base-CMX functionality and TP-CMX capability





CMX Card with Base-CMX functionality only



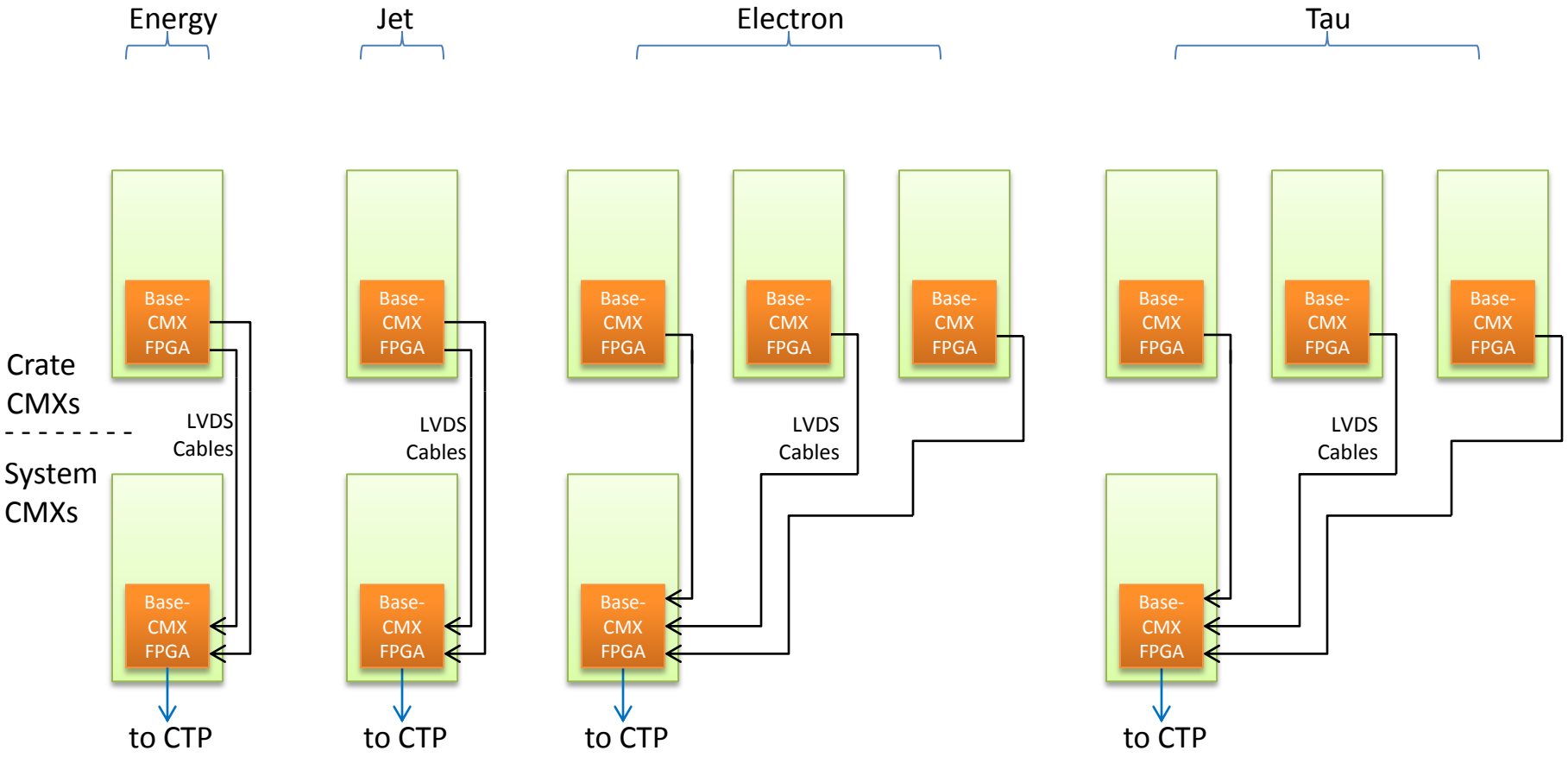


Overview of possible usage options

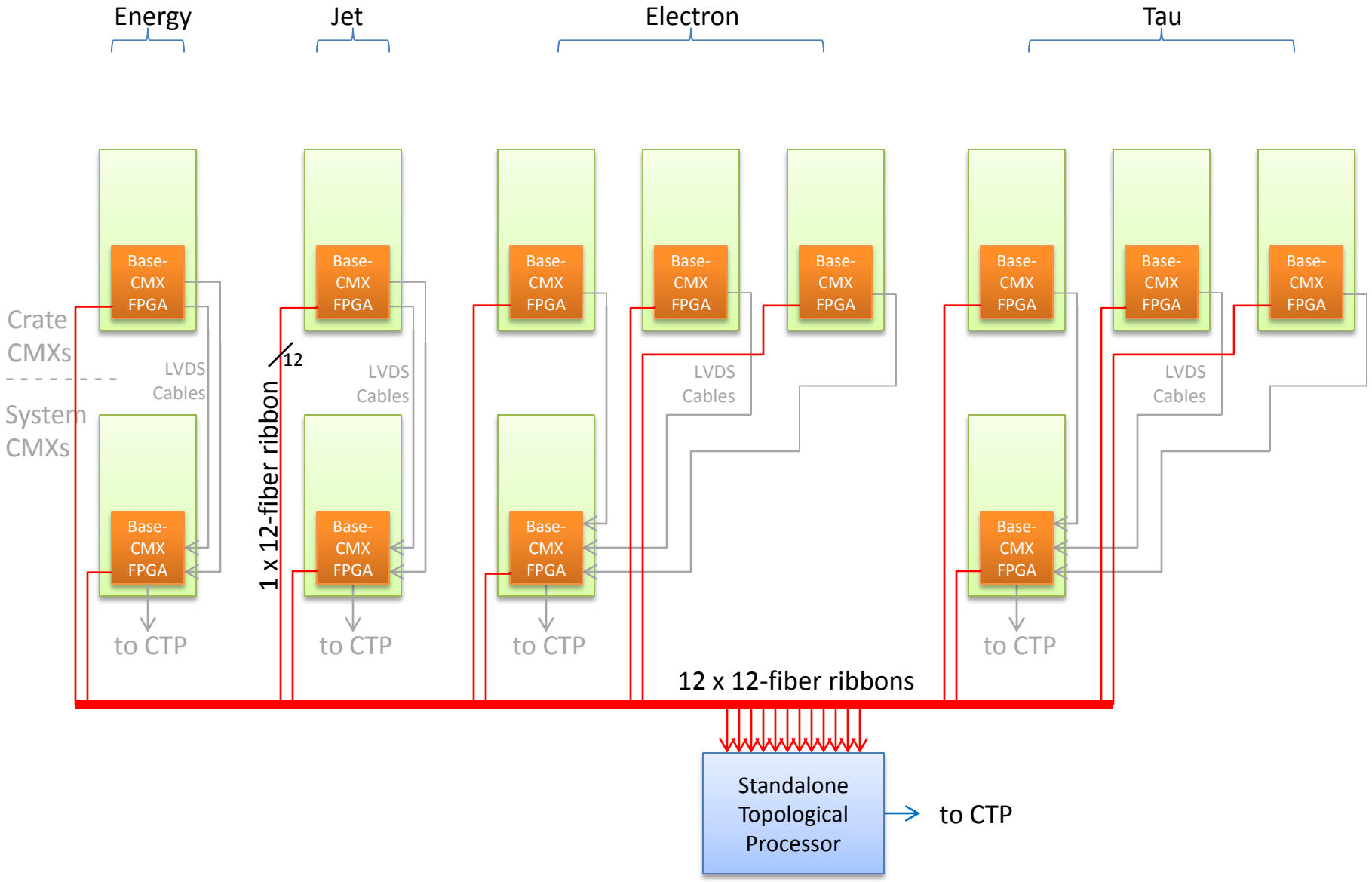
Flexibility is illustrated in following diagrams…

- CMM emulation only
- Base-CMX functionality only
  - Send data to Standalone TP (Raw or Zero-suppressed)
- TP-CMX functionality used
  - Only CMX-TP
  - Both CMX-TP and Standalone TP
  - In Crate to System CMX communication (not used as TP)

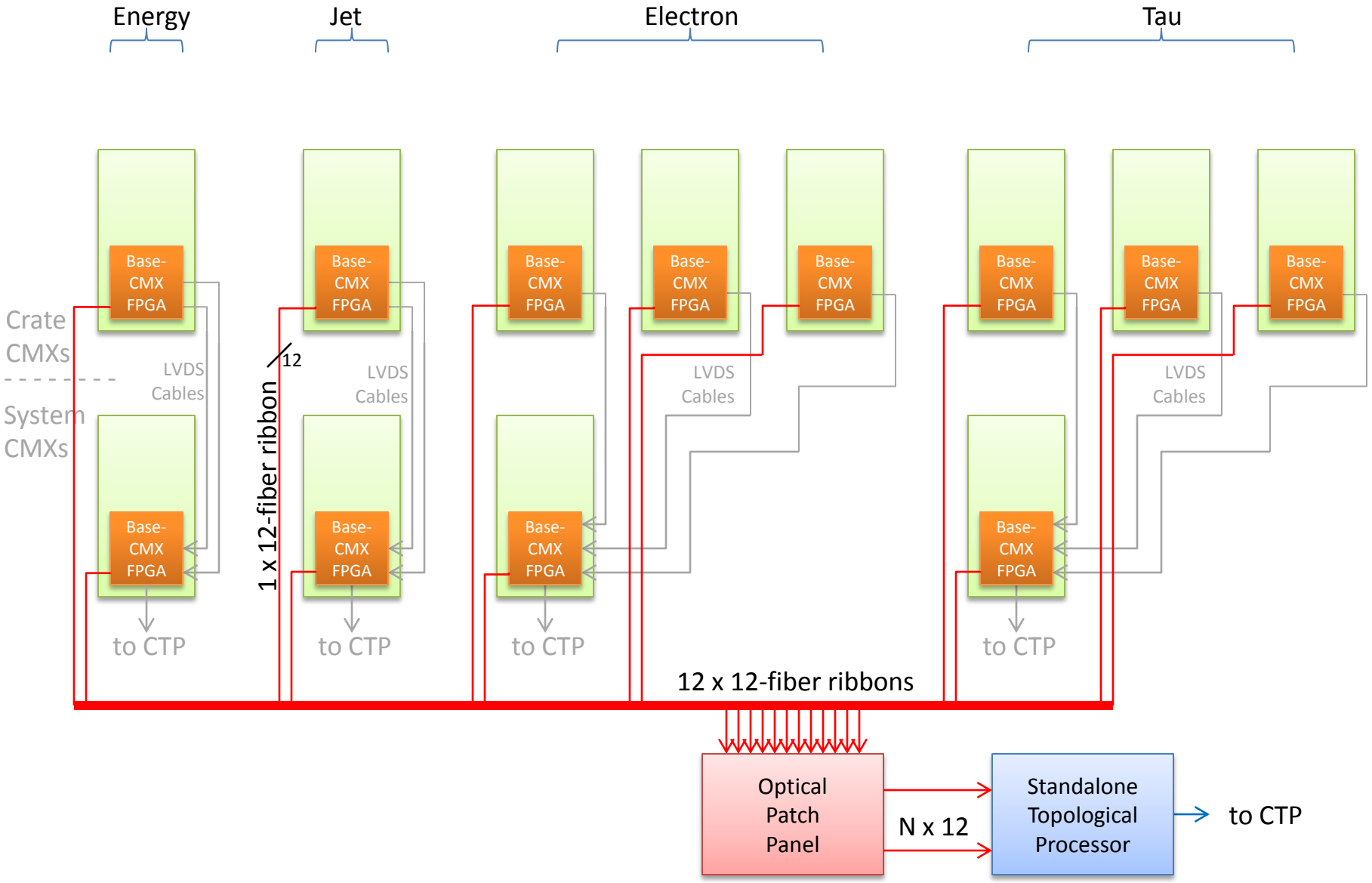
1. CMX emulation of CMM functionality (no TP involved)



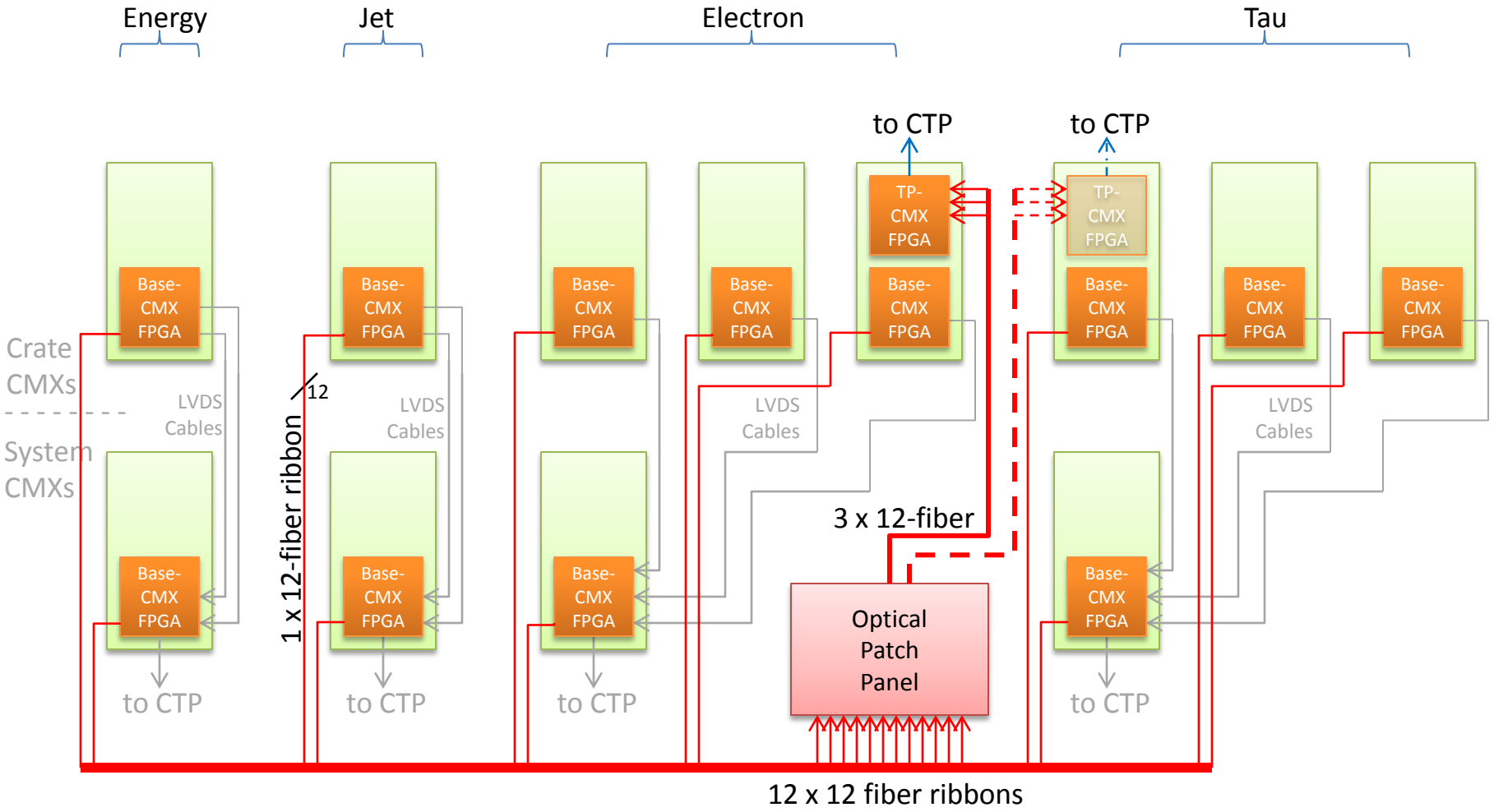
2. Standalone TP receiving Raw CMX Inputs



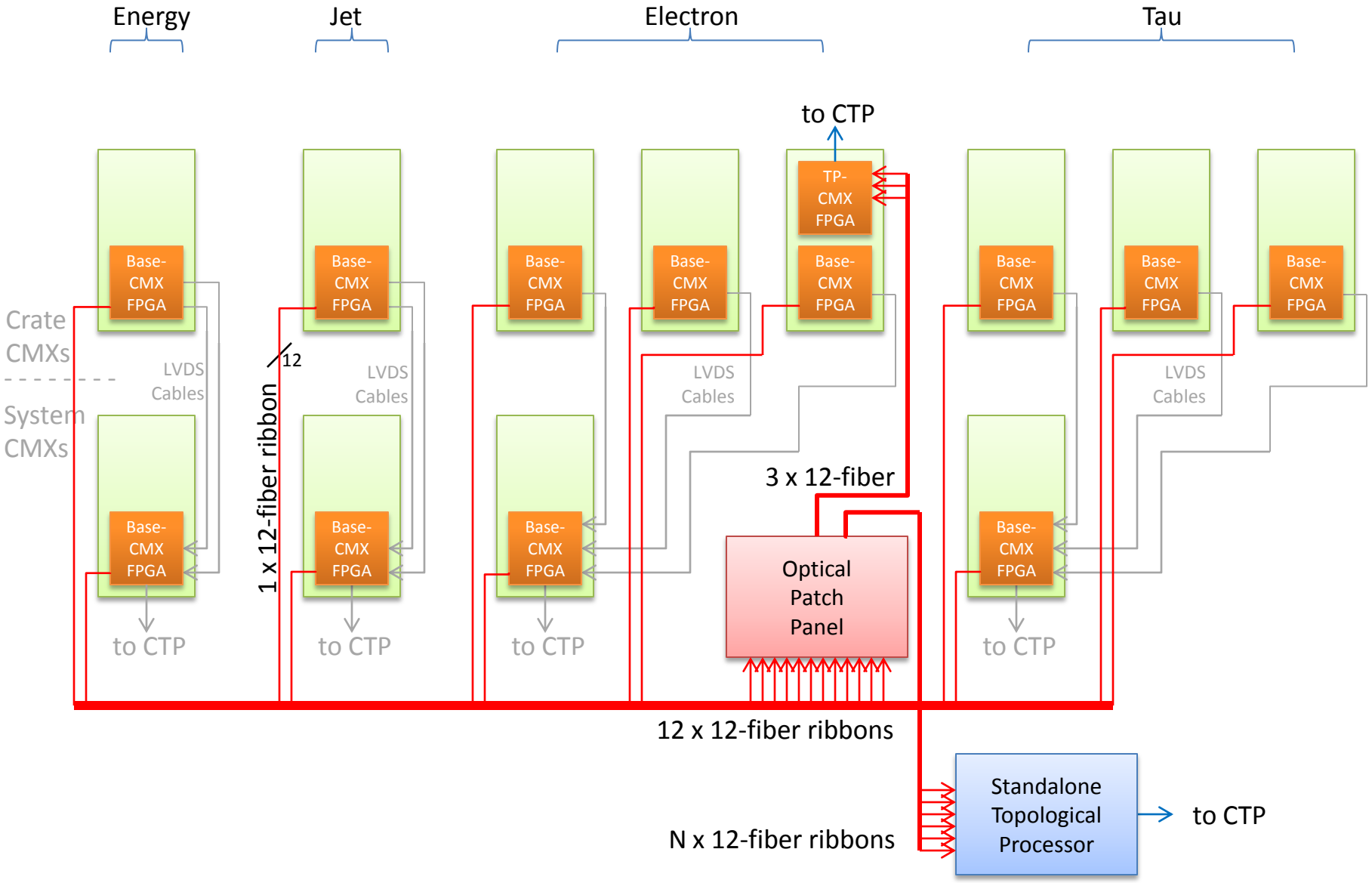
3. Standalone TP receiving Zero-Suppressed CMX Inputs



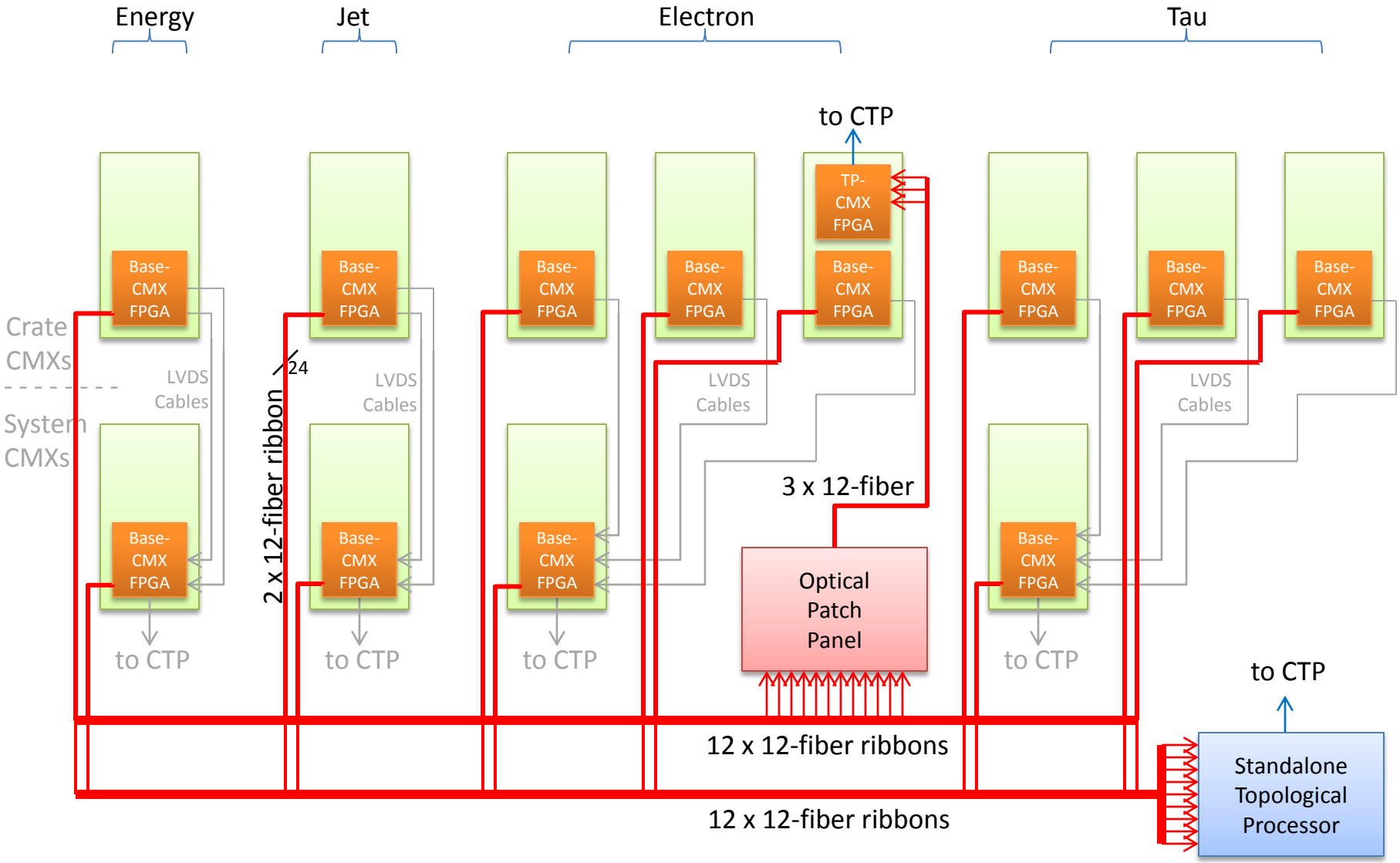
4. One (or more) CMX TP receiving Zero-Suppressed Inputs



5. CMX TP & Standalone TP receiving Zero-Suppressed Inputs



6. CMX TP receiving Zero-Suppressed & Standalone TP raw inputs



7. Example of TP-CMX FPGA in Crate to System communication