Status and planning of the CMX

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TDAQ Week, CERN

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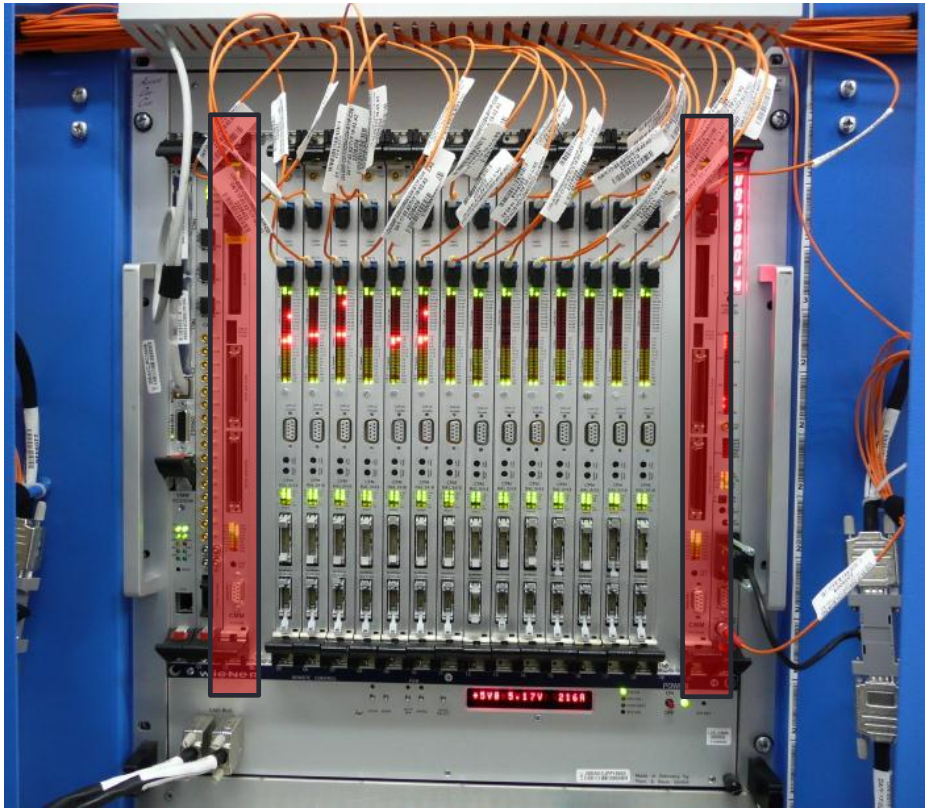
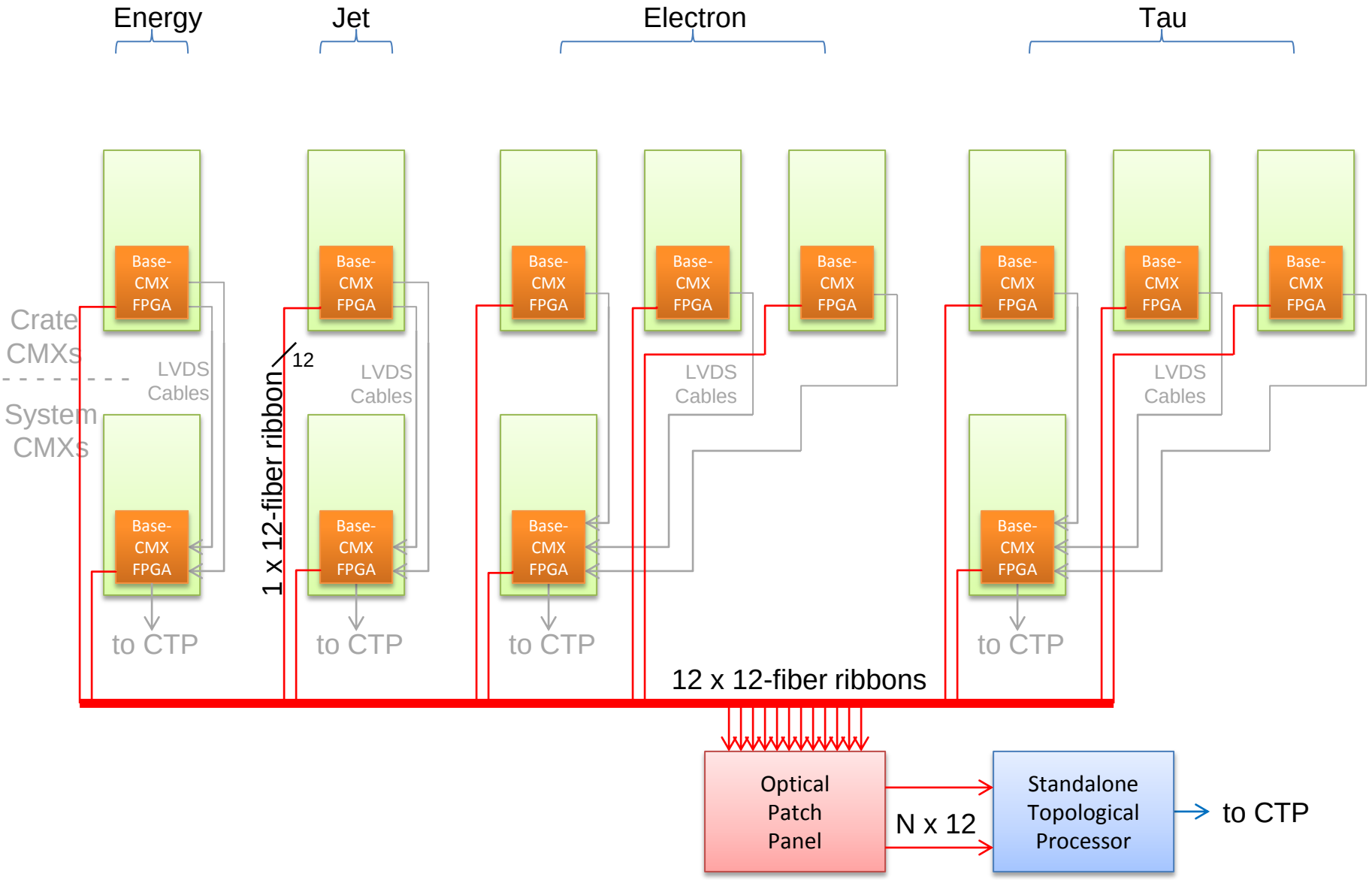
CMX: CMM upgrade

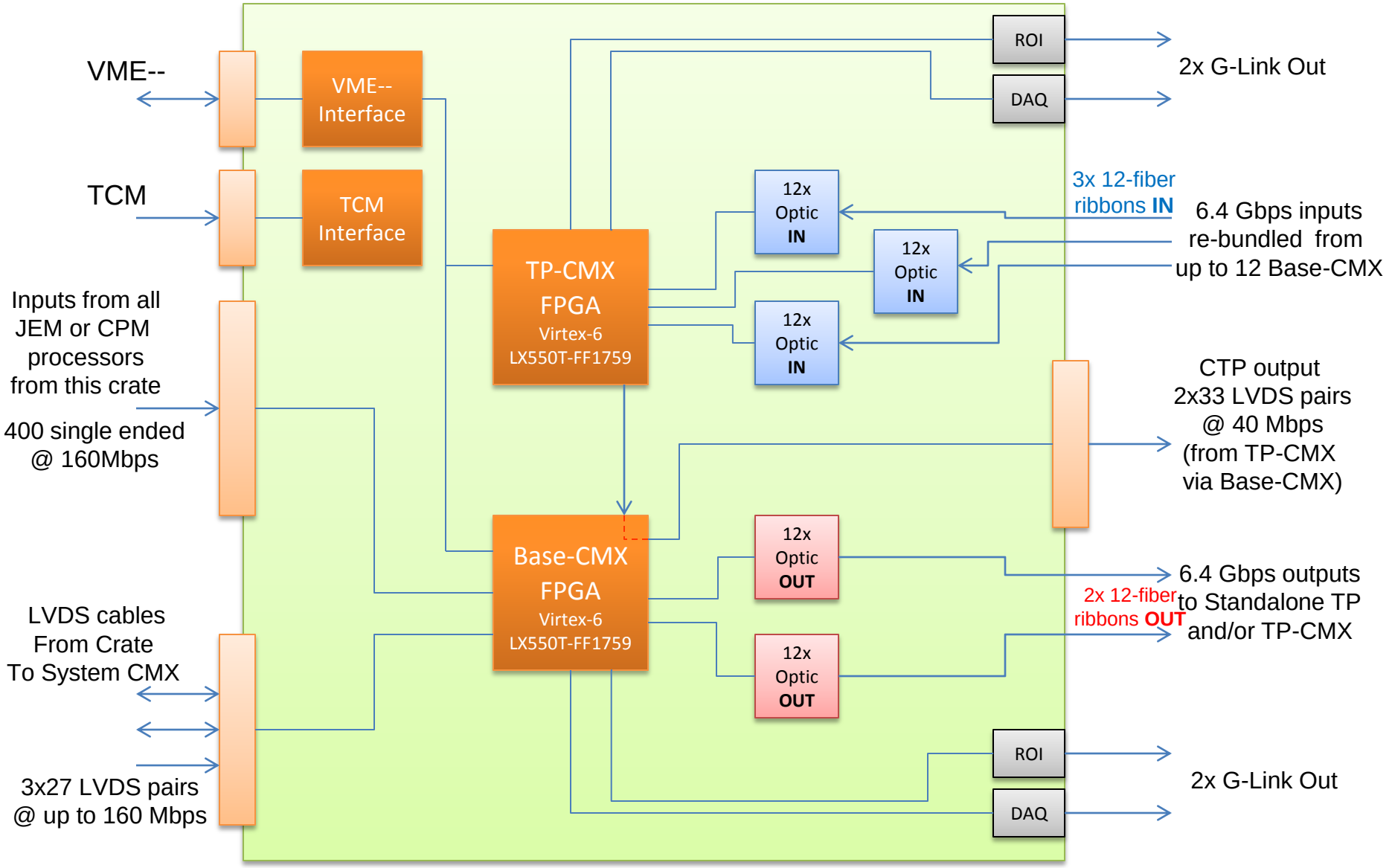


- Will replace CMM:
  - Backplane rate 40 →160Mbs
  - Crate to system rate (LVDS) 40 →160Mbs
  - Cluster information sent to Topological Processor (optical)
  - Optional partial TP functionality
    - Standalone TP is now planned
    - Some TP capability also designed onto the CMX

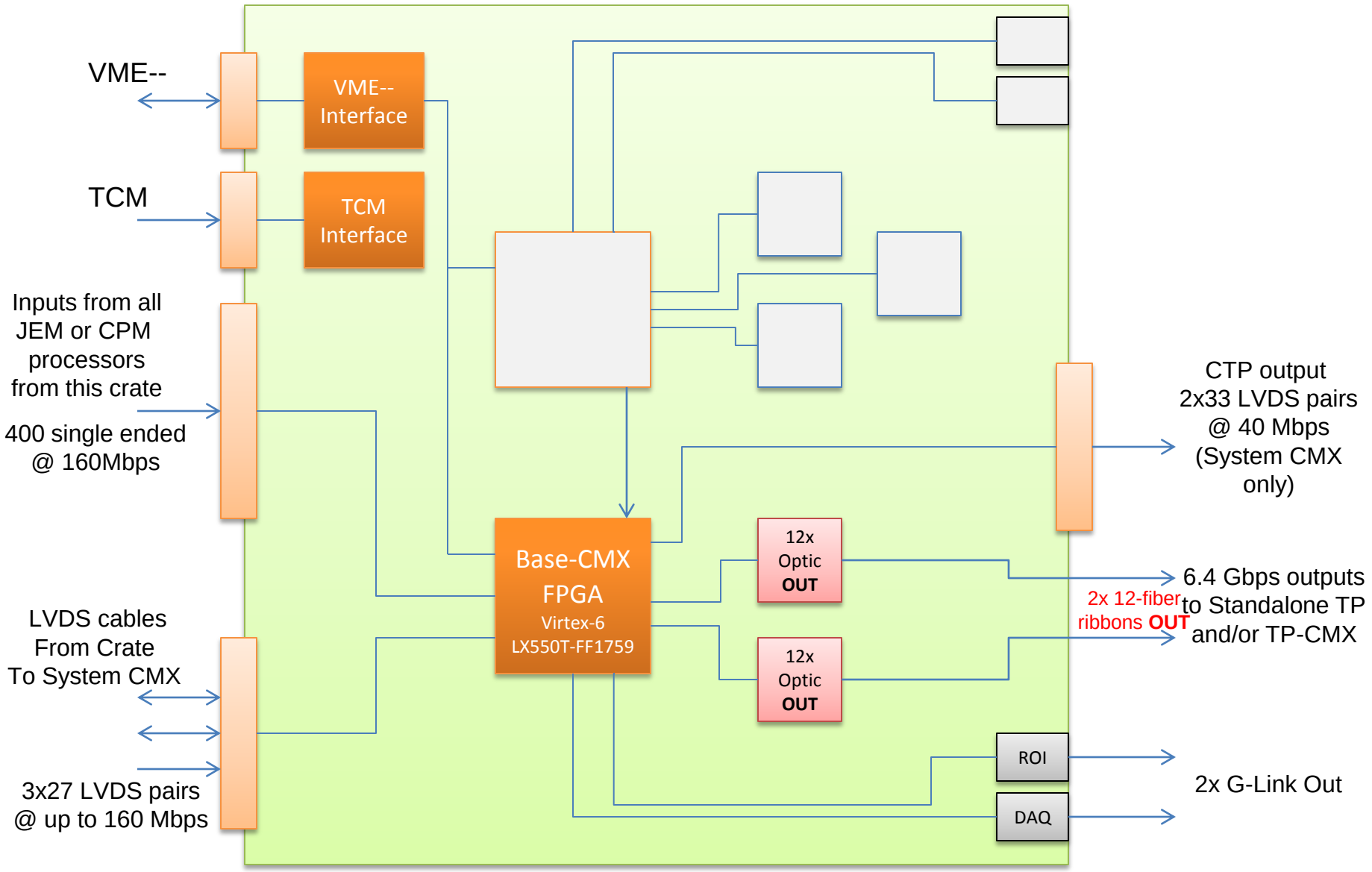
CMX: Use scenario with standalone TP



The CMX overview



CMX: modular design, most cards assembled without TP functionality



CMX development work on 3 fronts

- Engineering @MSU
  - Philippe, Dan, and Chip
- CMX input module firmware @CERN
  - Wojtek and Yuri
- VME/ACE/TTC (VAT) interface @CERN
  - Yuri

- Request from Chris and David - to address and present:

  "The detailed timeline & schedule from now until completion of commissioning at Point 1 in 2014 and a set of milestones associated to this schedule - typically ~10, including details of review procedure"

- Initial CMX development schedule is still valid
  - Minor adjustments

Initial CMX development schedule from 2011

- 2011: Project and engineering specifications
  - CMX project Preliminary Design Review (Done)
  - Preliminary design studies
  - Test rig installed, checked out at MSU (postponed until 2012)
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout
  - Production Readiness Review
  - Prototype fabrication, CMM firmware ported on CMX
  - Basic tests for backward compatibility in test rig at MSU
- 2013: Prototype testing/installation/commissioning, final fabrication
  - Full prototype tests in test rig at CERN
  - CMX firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMX modules
- 2014: Final commissioning in the L1Calo trigger system in USA15

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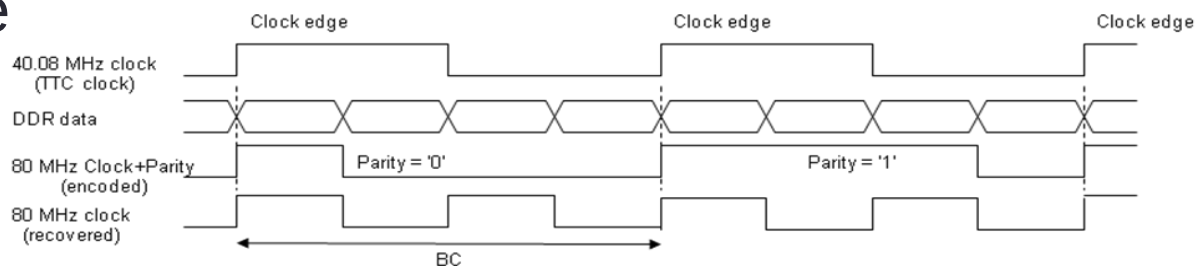
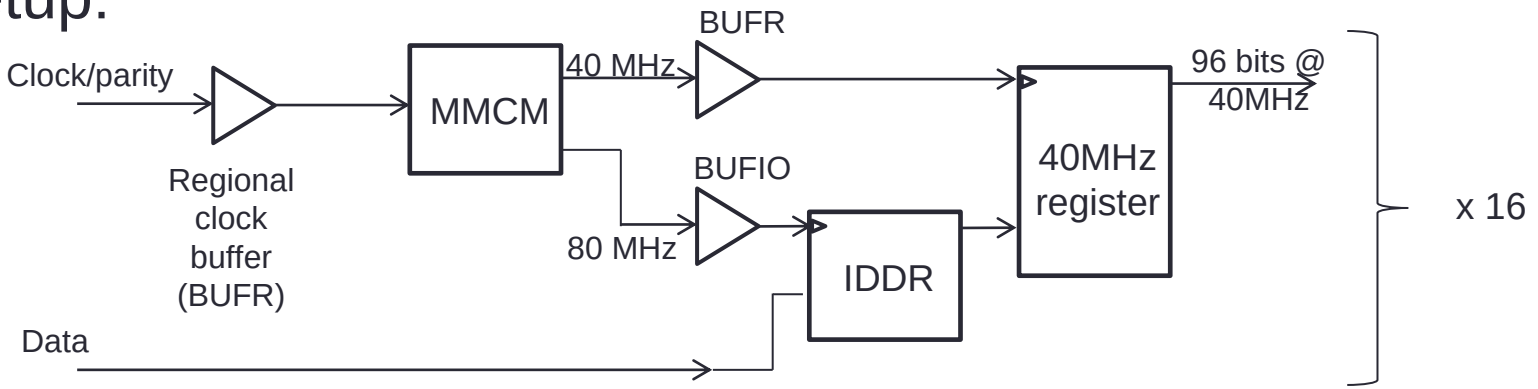
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout
    - CMX technology choice (FPGA choice, CMX/TP functionality) - DONE
    - 6U VME test card for VAT interface – PCB ready for testing in June
    - Real-time data path layout (ongoing)
    - CMX input module firmware currently under test on the XILINX development module
    - Power budget estimate
  - Prototype fabrication
    - mechanical testing in January
      - Will happen within ~month, not urgent yet.
      - Blank card, backplane connectors, front panel tests.
  - CMM firmware ported on CMX
    - Firmware for VAT interface (2 CPLD + TTC FPGA) to Spartan-3AN FPGA (Adapt VHDL code, create test bench, specify VME register model) (Yuri)
    - Most of the work completed at Stockholm (Pawel Plucinski, Sam Silverstein)
      - Needs to be adapted to final package choice
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review (L1Calo/TDAQ) Fall/Winter
    - PRR after the prototype(s) is tested and
    - final check before going into full production

2011/2012: design studies: Clock/parity recovery

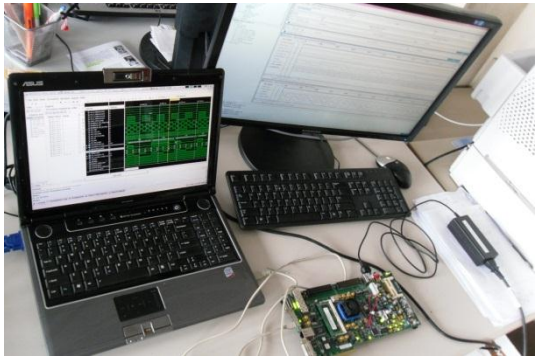
- Clock+Parity encoded on single line
- Variable duty cycle



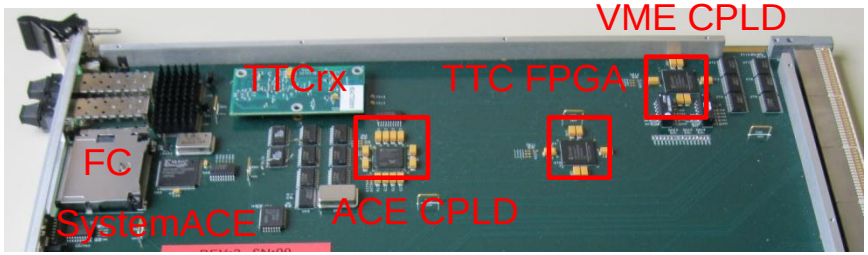
- Setup:



- Scheme tested using Virtex 6 eval board
- Data capture developed, simulated and 'Placed and Routed' on target FPGA
  - Needs repeating – different package chosen

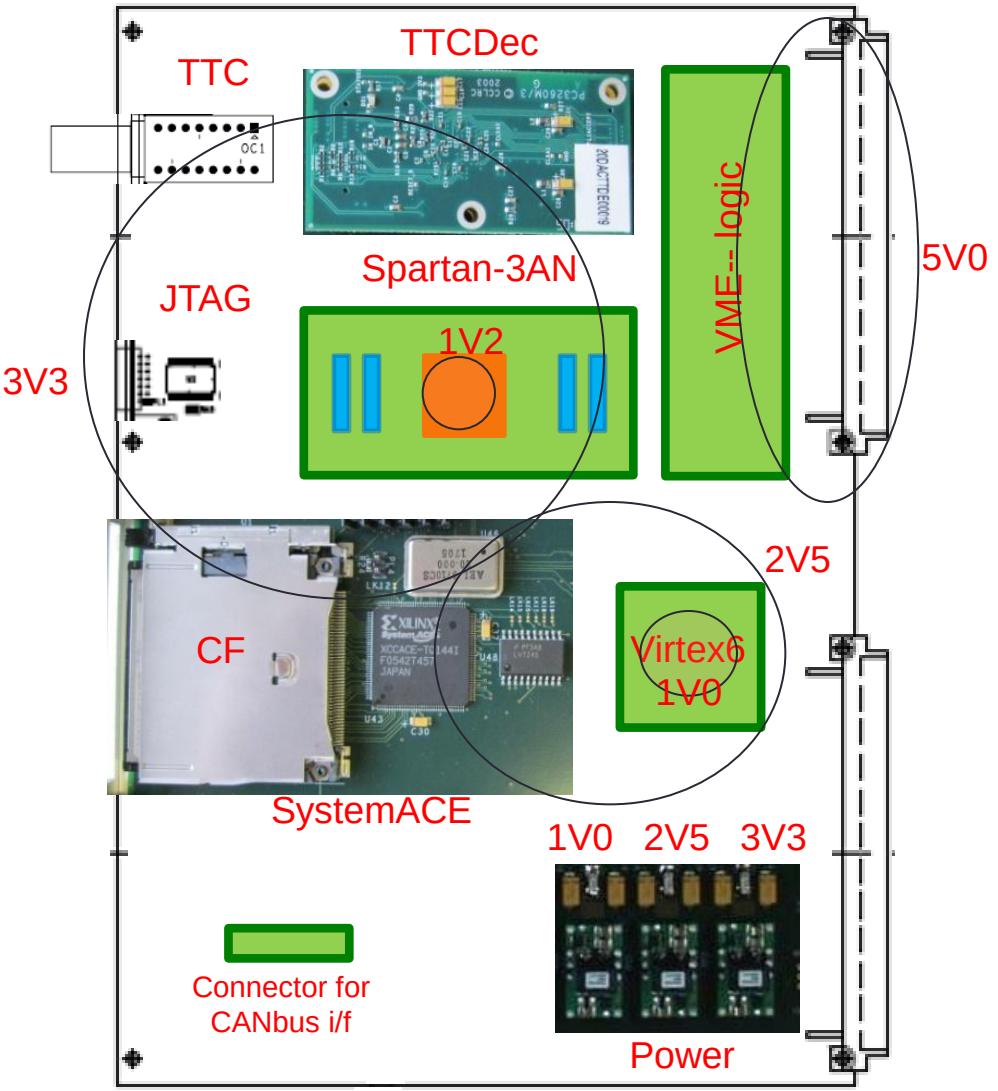


2012: PCB layout: VME/ACE/TTC (VAT) interface test card



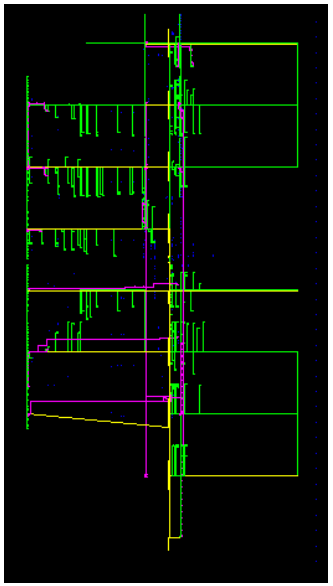
VME/ACE/TTC (VAT) part of CMM

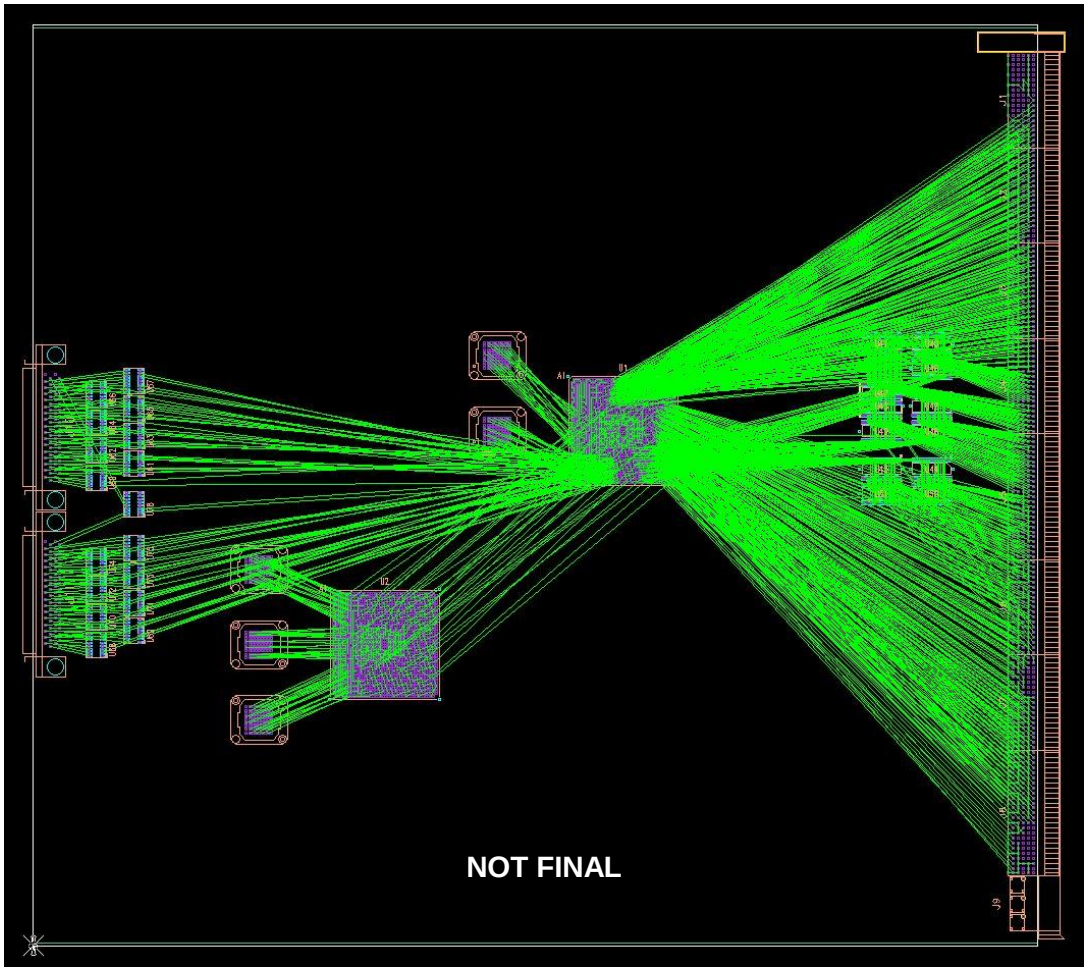
- Redesign HW with new components
  - Fit design into single device
- 6U VME test card for
  - Hardware implementation
  - Main FPGA re-configuration
  - Software
  - To be merged into CMX design
- PCB arrives in June
- Next:
  - Firmware for VAT card
  - Firmware for Virtex 6 FPGA
  - Test Stand and software



2012 PCB Layout: Backplane – FPGA connection

- Challenging milestone
  - Signal density
  - Avoid contention
- Drives FPGA package choice
- Implications for Firmware design





- 2013: Prototype testing/installation/commissioning, final fabrication
  - Full prototype tests in test rig at CERN
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMX modules

Conclusions

- Schedule proposed is maintained
  - Minor adjustments
- Tasks proceeding according to plan
- Need more detailed set of steps for in-situ tests before and after first beam
- Optimistic outlook for project completion