Status and planning of the CMX

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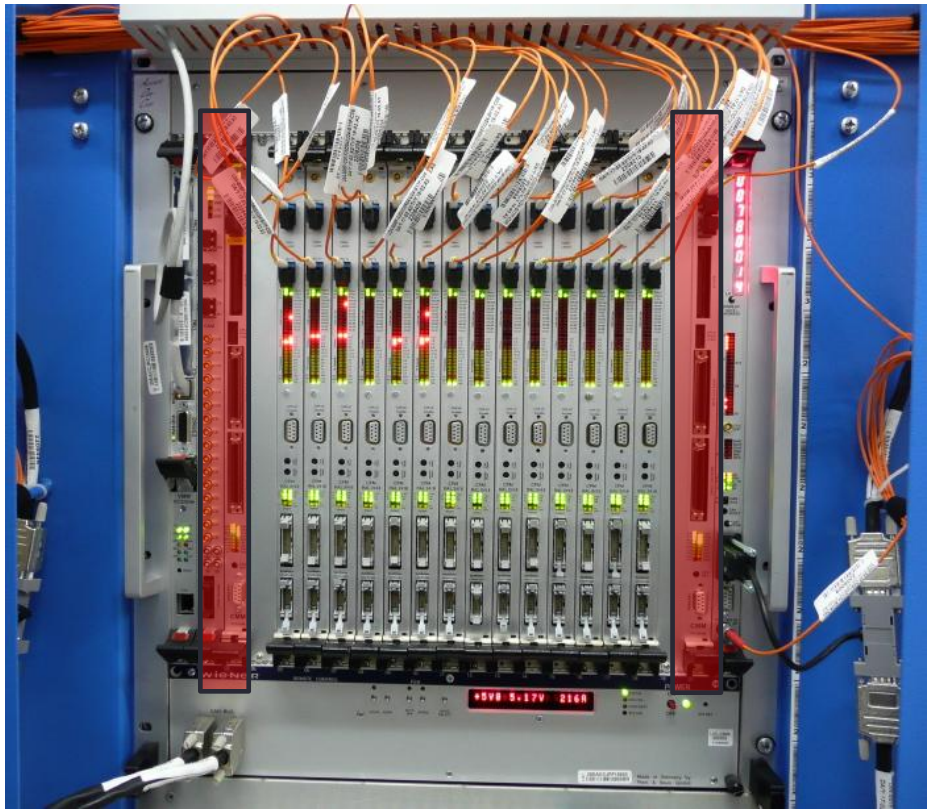
Level-1 Calorimeter Trigger General Meeting, CERN

May 24, 2012

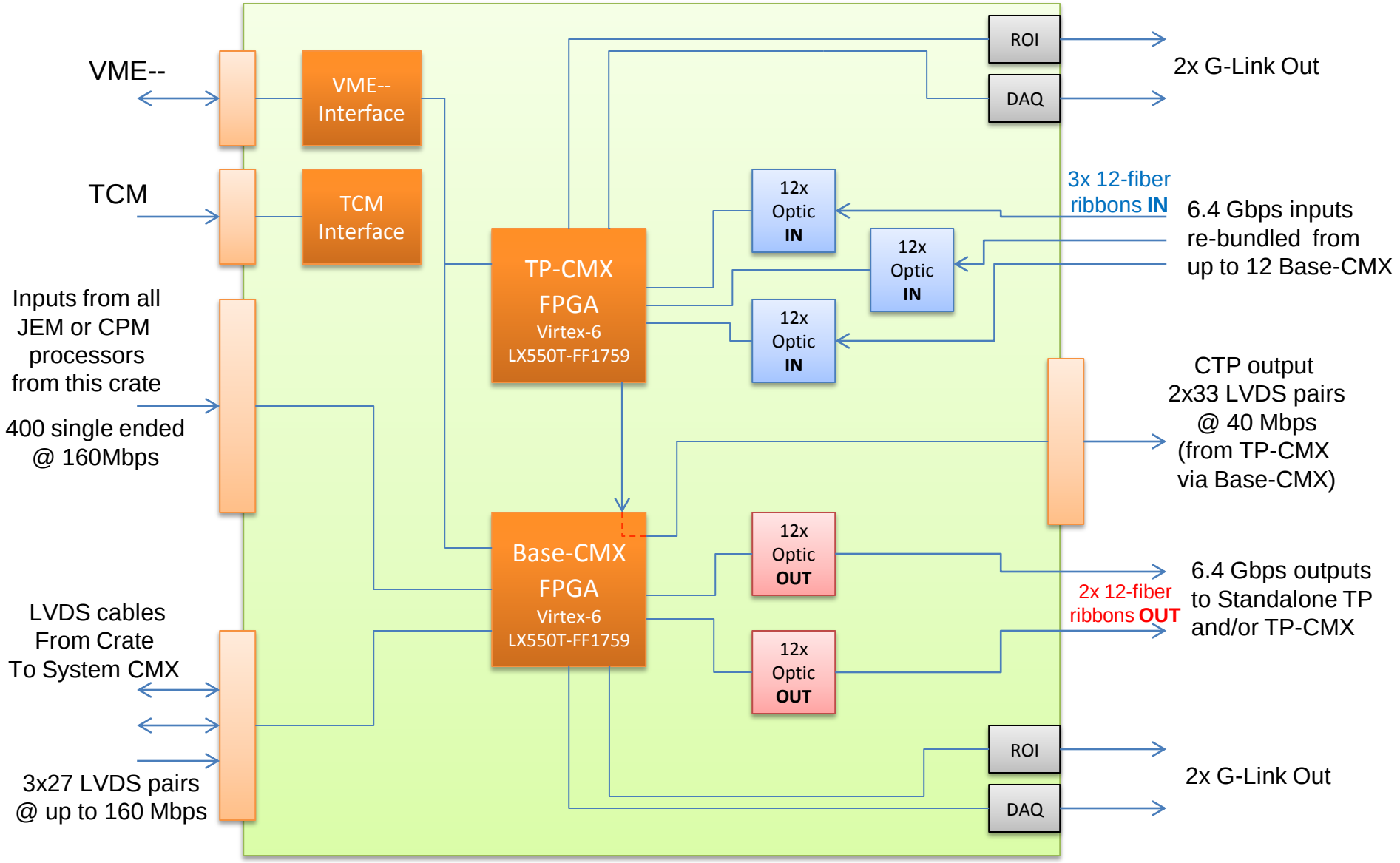
CMX: CMM upgrade



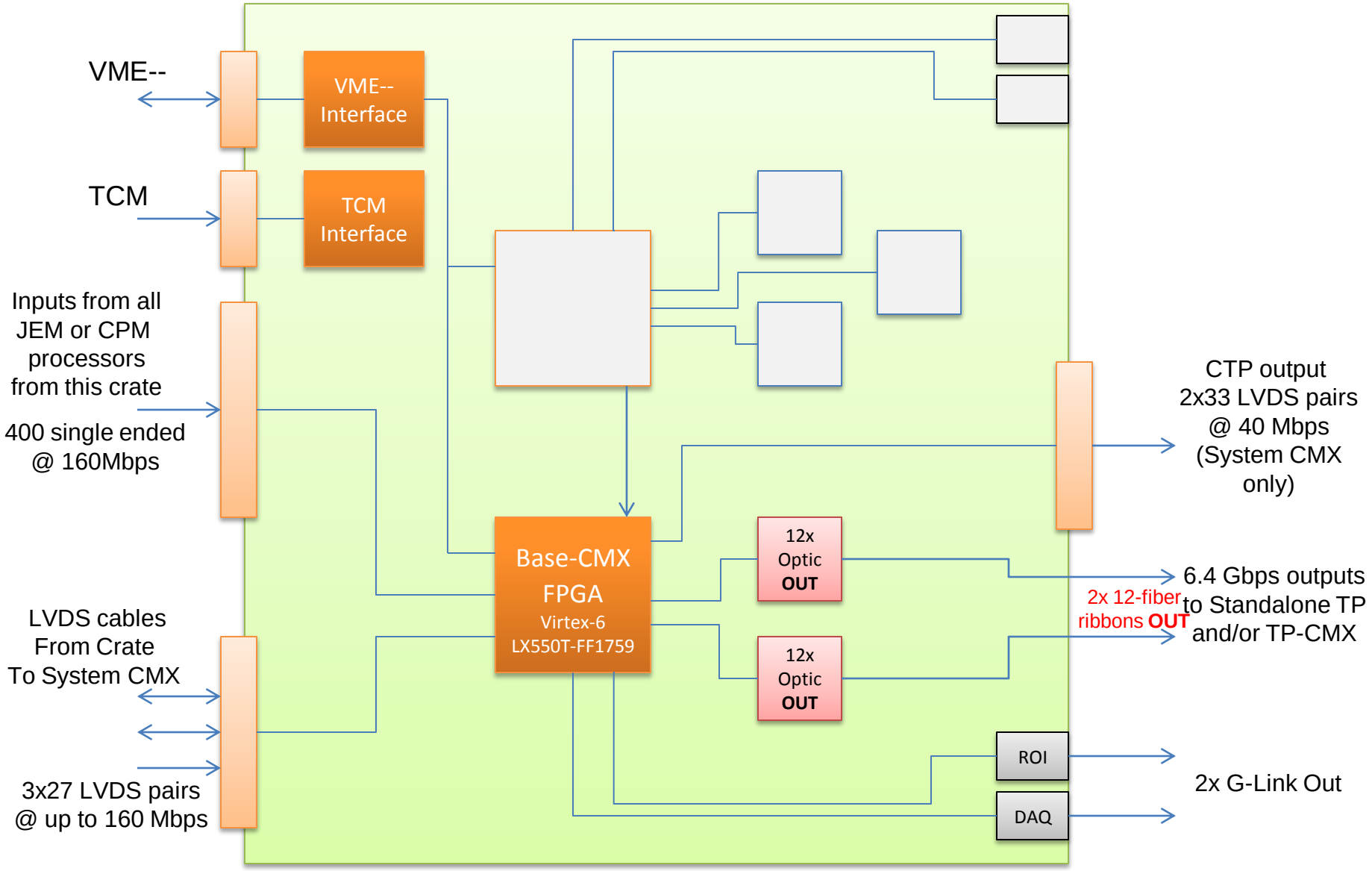
CMX replaces CMM:

1) JEM/CPM to CMX (backpl) rate 40 →160Mbps
2) Crate CMX to System CMX (cables) rate 40 →160Mbps
3) Cluster information sent to Topological Processor (12-fiber ribbons @6.4Gbps)
4) Optional partial TP capability included
   - Standalone TP is now planned
   - Some TP capability still desired for CMX platform (flexibility)

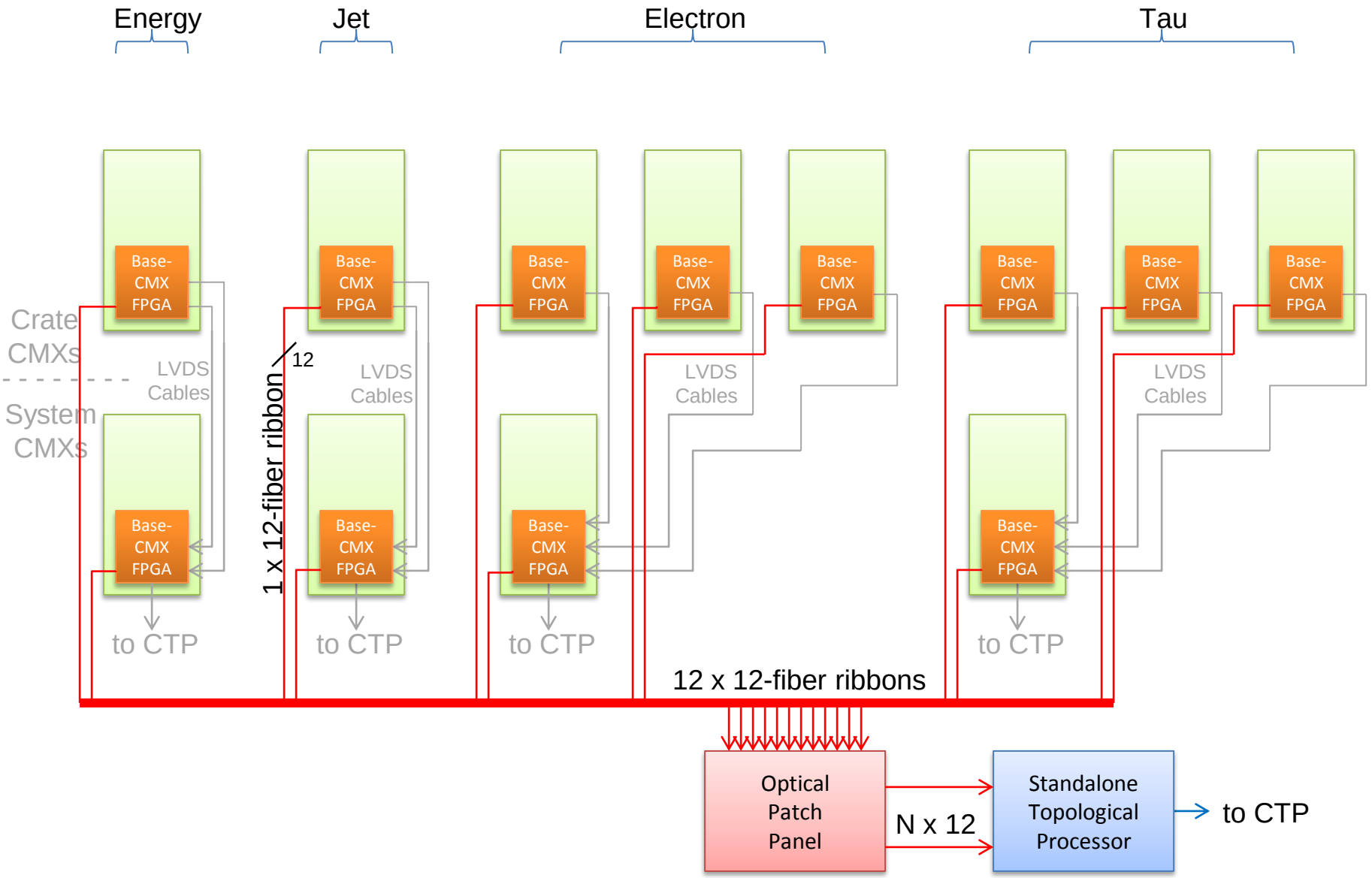
The CMX overview



CMX: modular design, most cards assembled without TP functionality



CMX: Use scenario with standalone TP



CMX development work on 3 fronts

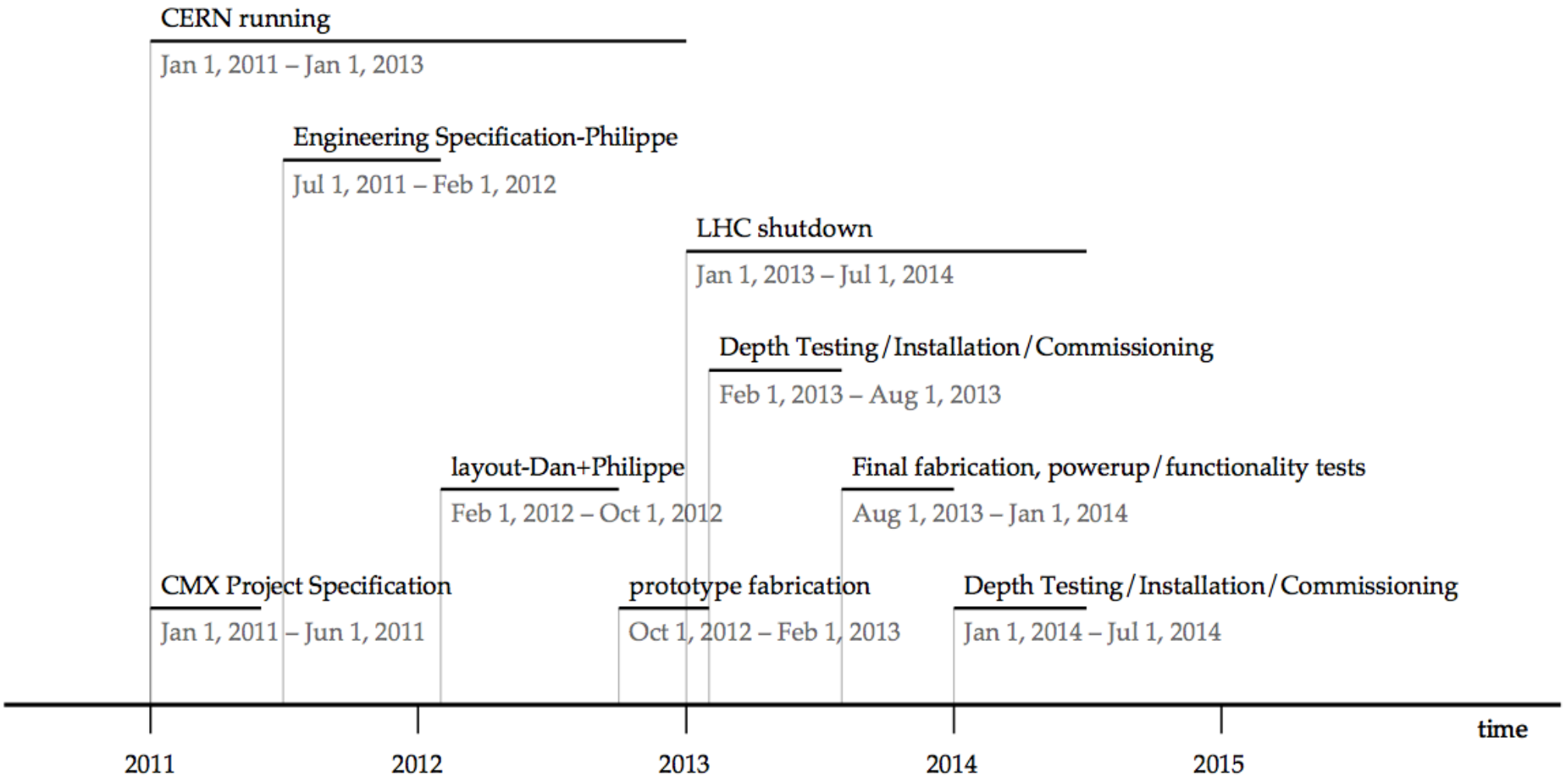
- **3 parallel efforts**
  - CMX Engineering @MSU
    - Philippe, Dan, and Chip
  - CMX input module firmware @CERN
    - Wojtek and Yuri
  - VME/ACE/TTC (VAT) interface @CERN
    - Yuri

- CMX development schedule from Stockholm Preliminary Design Review is still valid
  - Minor adjustments

CMX development schedule from PDR

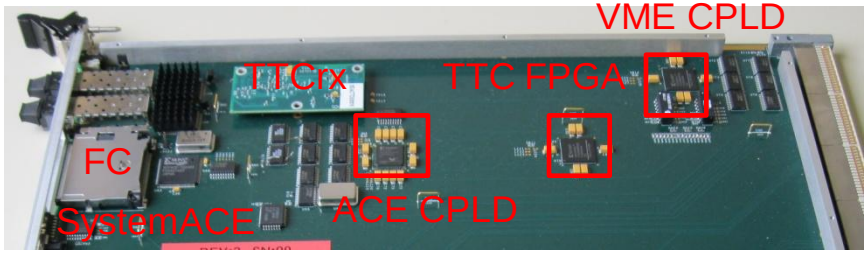
- 2011: Project and engineering specifications
  - CMX project Preliminary Design Review (done)
  - Preliminary engineering design studies (done, RAL review)
  - Test rig installed, checked out at MSU (postponed until 2012)
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout (ongoing)
  - CMM firmware ported to CMX
  - Prototype fabrication (fall 2012)
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review
- 2013: Prototype testing/installation/commissioning, final CMX fabrication
  - Full prototype tests in test rig at CERN
  - CMX firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of Final CMX (bulk with just Base, few with TP)
- 2014: Final commissioning in the L1Calo trigger system in USA15

CMX development timeline



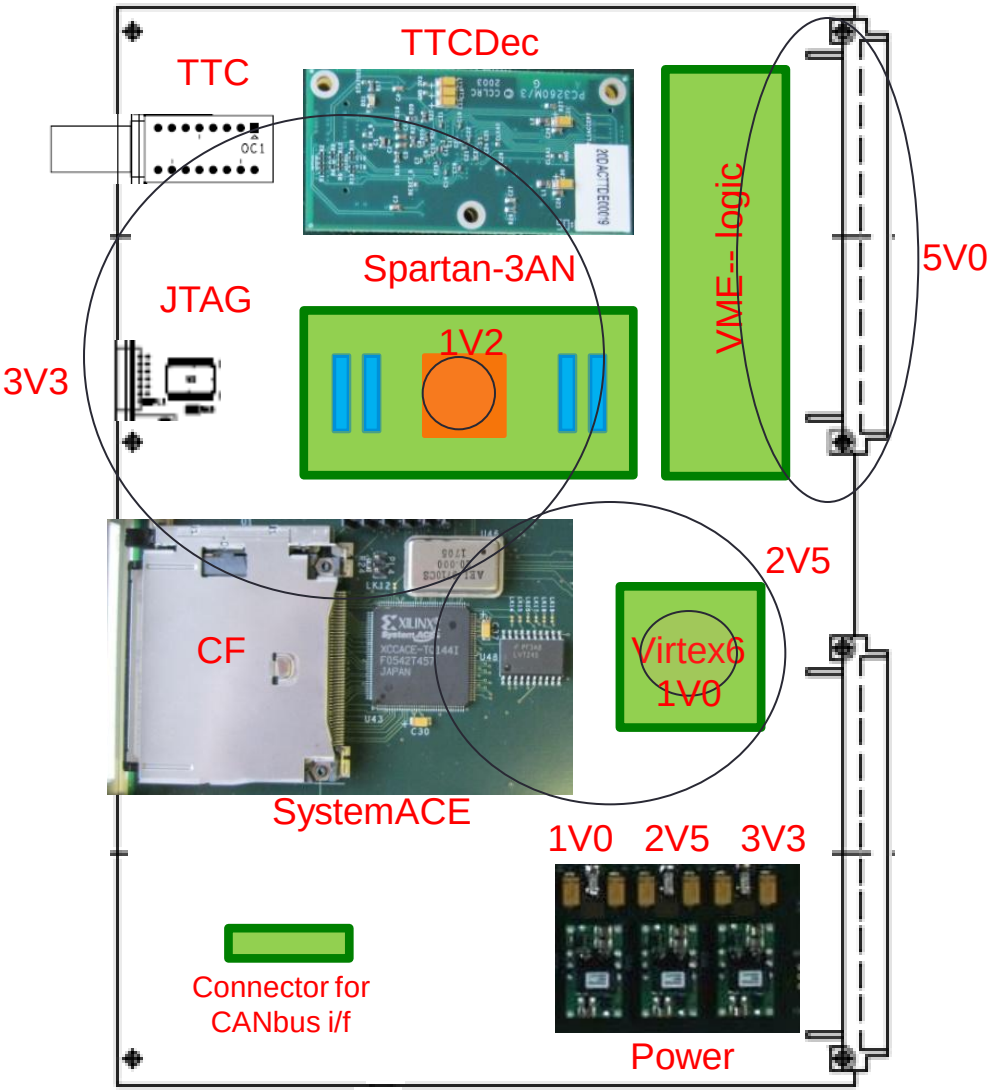
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout
    - CMX technology choice with Dual FPGA design: Base-CMX & TP-CMX (RAL Feb 2012)
    - 6U VME test card for VAT interface (PCB ready for testing in June)
    - Real-time data path layout (ongoing)
    - CMX input module firmware currently under test on the XILINX development module
    - Power budget estimate
  - Prototype fabrication
    - mechanical testing
      - Blank card, backplane connectors, front panel tests.
      - Will happen before real prototype board, but not urgent yet.
  - CMM firmware ported on CMX
    - Firmware for VAT interface (2 CPLD + TTC FPGA) to Spartan-3AN FPGA (Adapt VHDL code, create test bench, specify VME register model) (Yuri)
    - Most of CMM data path work completed at Stockholm (Pawel Plucinski, Sam Silverstein)
      - Needs to be adapted to final package choice
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review (L1Calo/TDAQ) Fall/Winter
    - PRR after the prototype(s) is tested and
    - final check before going into full production of final modules

2012: PCB layout: VME/ACE/TTC (VAT) interface test card



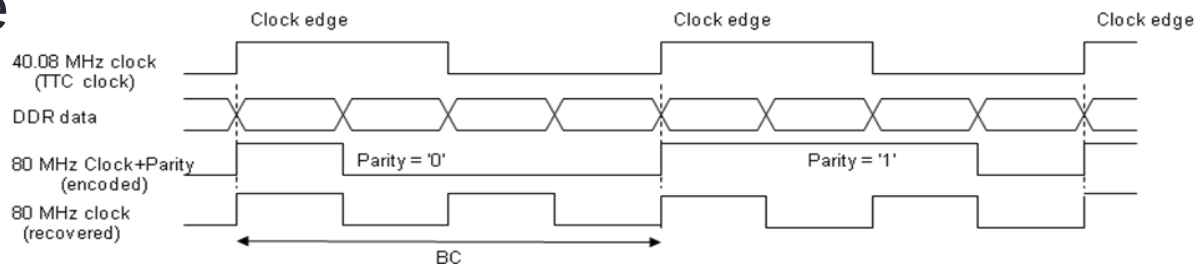
VME/ACE/TTC (VAT) part of CMM

- Redesign HW with new components
  - Fit design into single device
- 6U VME test card for
  - Hardware implementation
  - Main FPGA re-configuration
  - Software
  - To be merged into CMX design
- PCB arrives in June
- Next:
  - Firmware for VAT card
  - Firmware for Virtex 6 FPGA
  - Test Stand and software

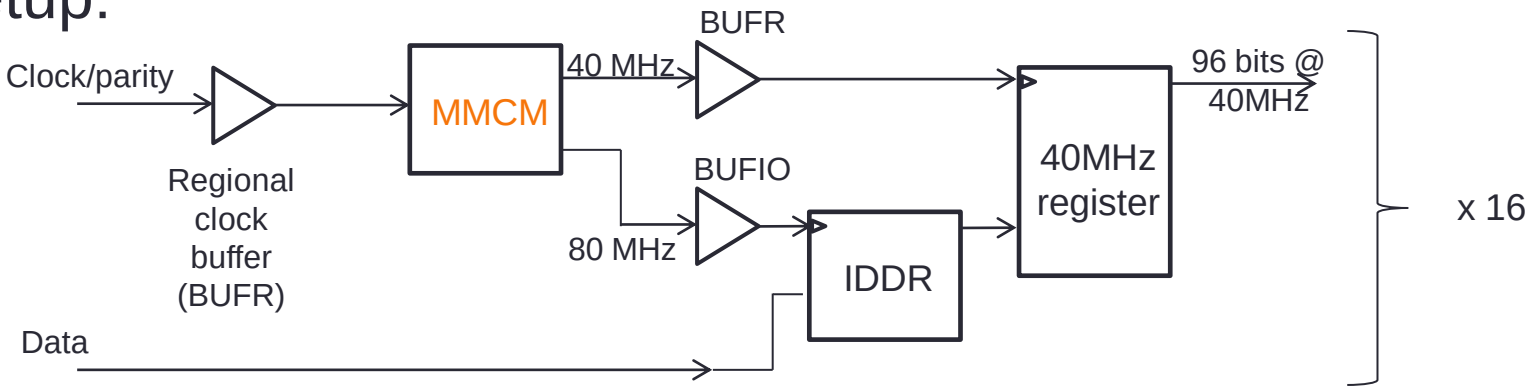


2011/2012: design studies: Clock/parity recovery

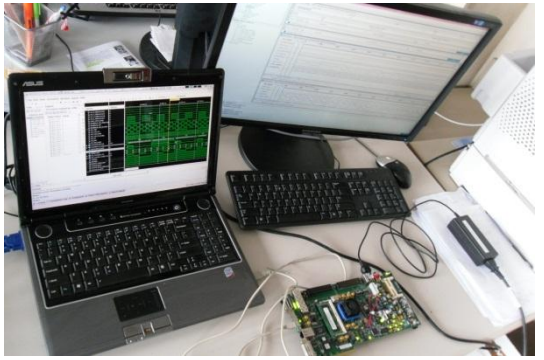
- Clock+Parity encoded on single line
- Variable duty cycle



- Setup:

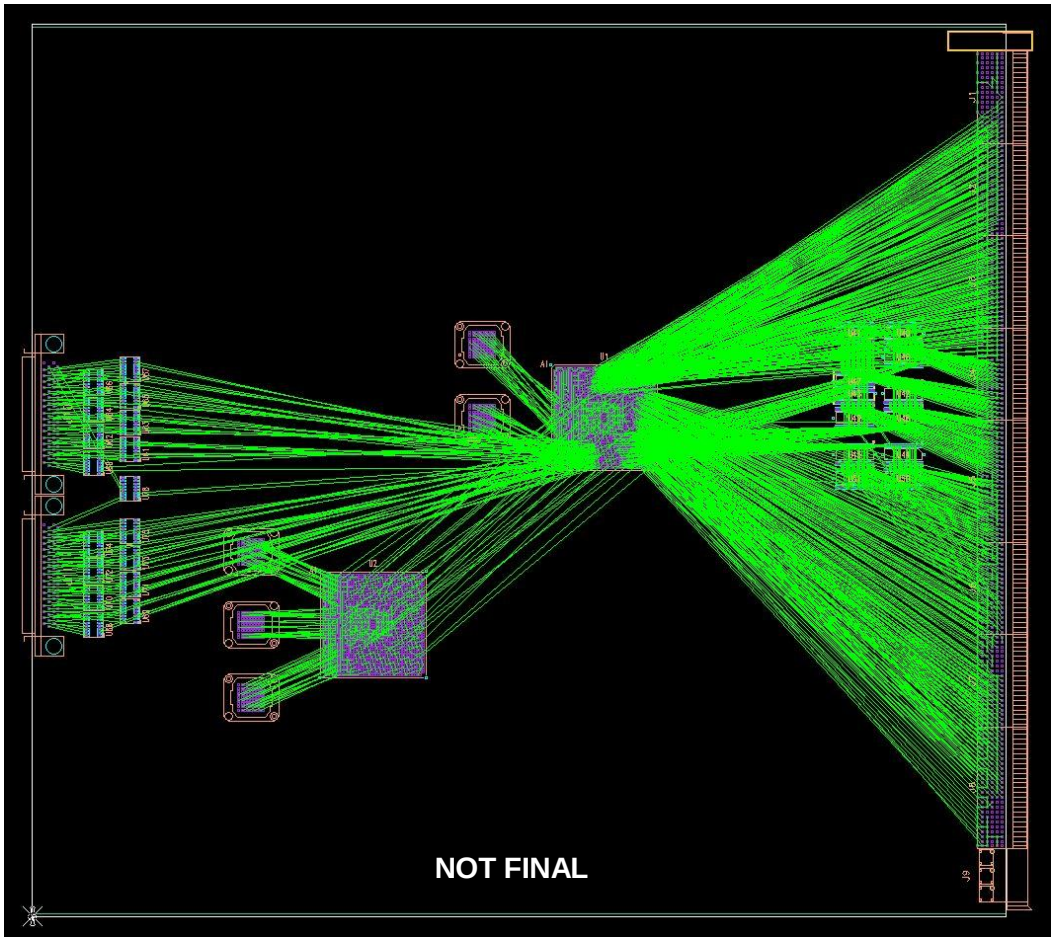


- Scheme tested using Virtex 6 eval board
- Data capture developed, simulated and 'Placed and Routed' on target FPGA
  - Needs repeating – different package chosen

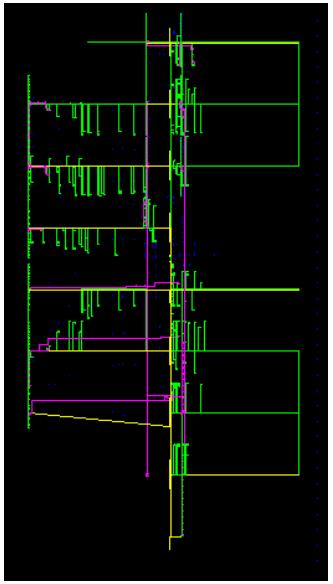


2012 PCB Layout: Backplane – FPGA connection

- Optimize Real-Time Path Layout
  - High local density near FPGA
  - Especially 400x JEM/CPM inputs
  - Spread out & mixed up on backpln → grouped & sorted at FPGA
  - Span neighbor IO blocks
  - Regional Clock input for clock/parity
  - Tune IO Assignments
  - Cleanest connections: no extra via
  - Minimize number of trace layers



- In Parallel with Firmware design
  - Validate assignment
  - Timing constraints



Conclusions

- Original schedule is maintained
  - With minor adjustments
  - Prototype effort proceeding in parallel on 3 fronts according to plan
  - Will need to increase level of detail for set of steps during in-situ tests before and after first beam
- Optimistic outlook