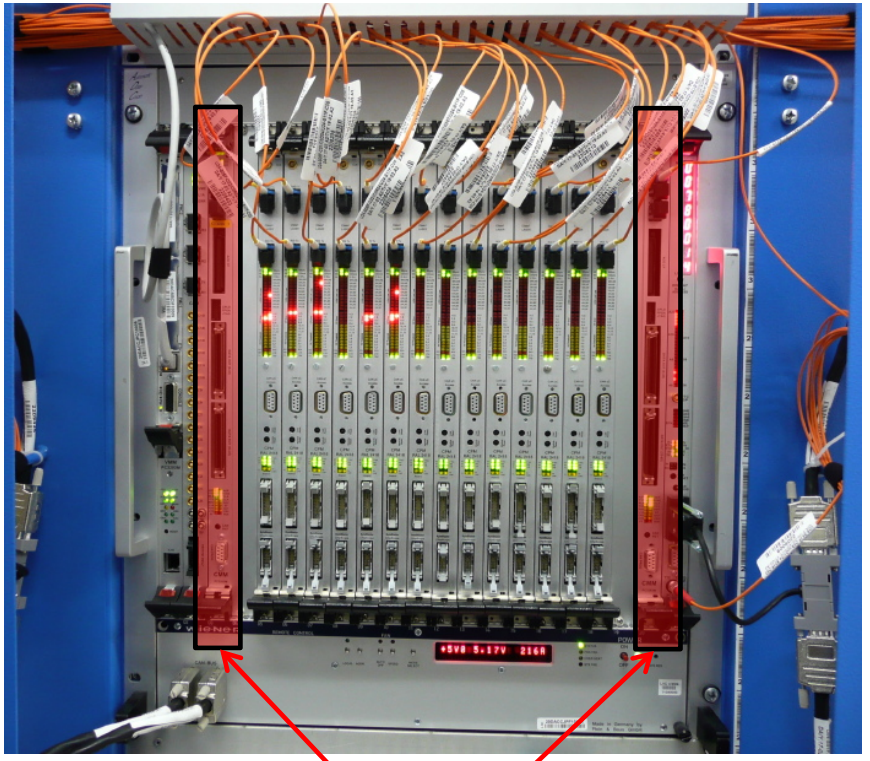
CMX status

Yuri Ermoline for the MSU group

Mini-TDAQ week, CERN, 9-11 July 2012,

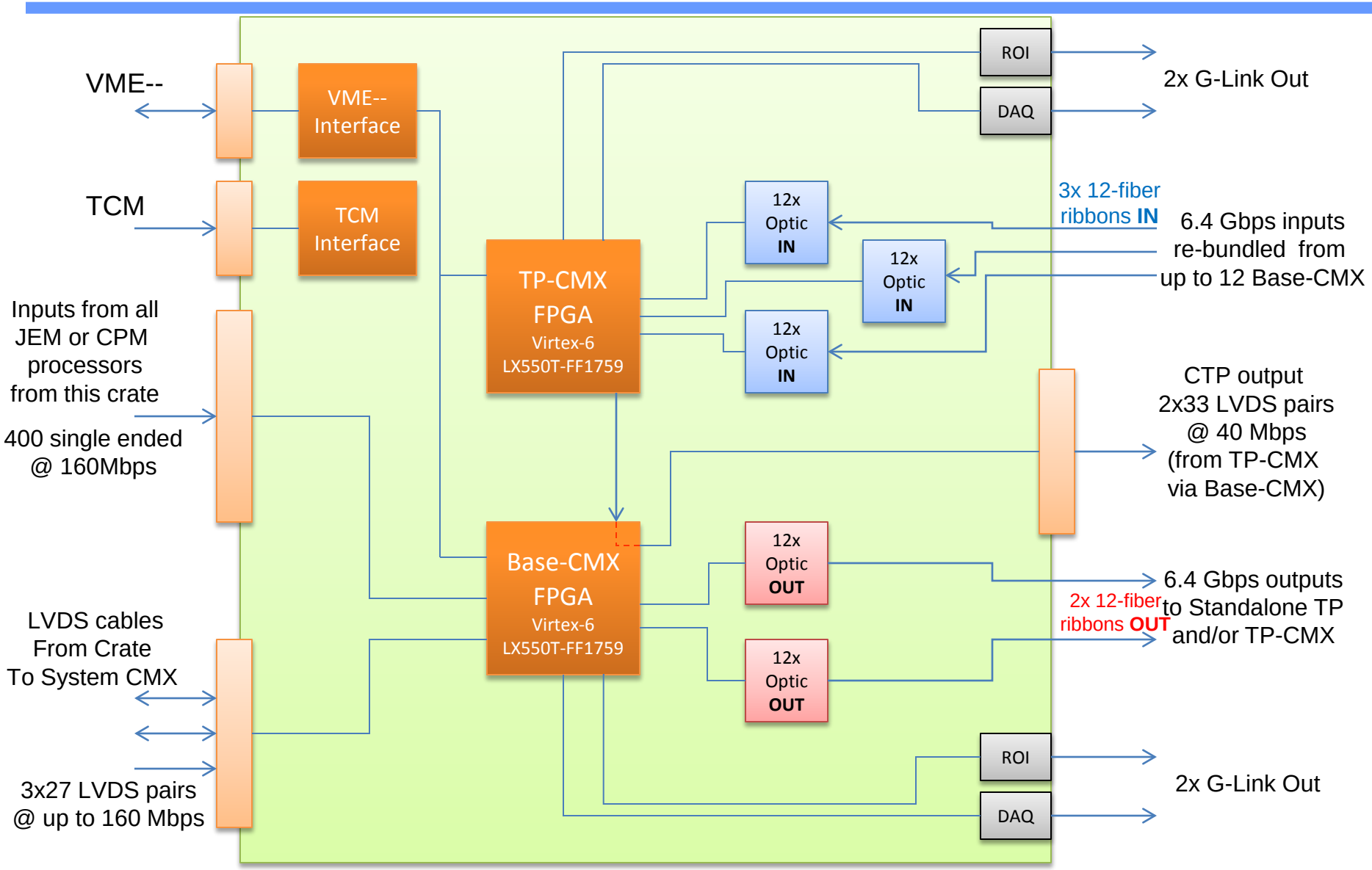
CMX: CMM upgrade

- CMX replaces CMM in L1Calo crate
  - Modern hardware implementation
  - JEM/CPM to CMX (backplane) rate 40 →160Mbs
    - ⇨ New data format
  - Crate CMX to System CMX (cables) rate 40 →160Mbs
  - Cluster information sent to TP (Topological Processor) over optical links (12-fiber ribbons @6.4Gbps)
- Optional partial TP capability included
  - Standalone TP is now planned
  - Some TP capability still desired for CMX platform (flexibility)

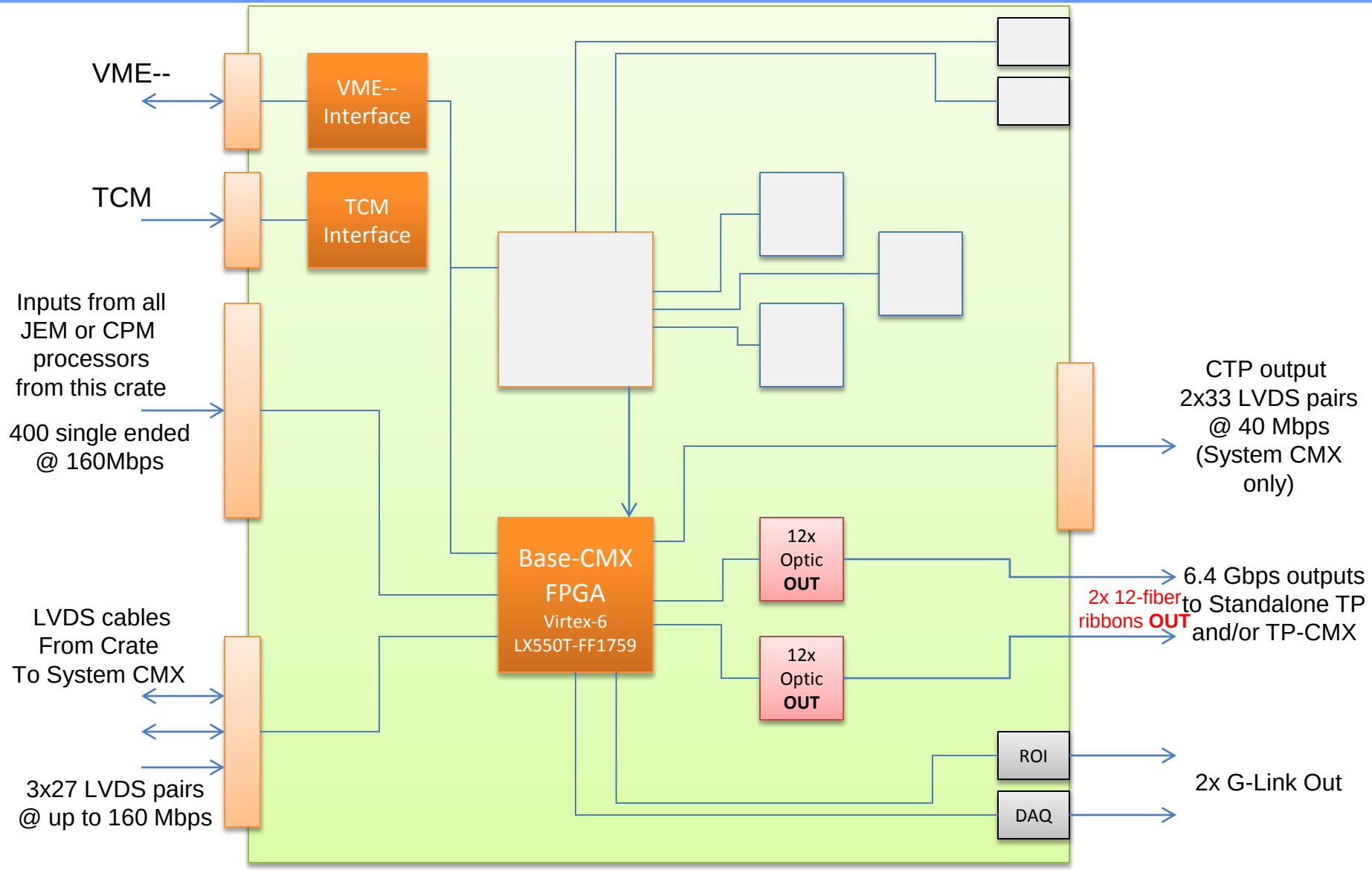


CMX

CMX overview: modular design (Base + TP)



Most cards assembled without TP functionality



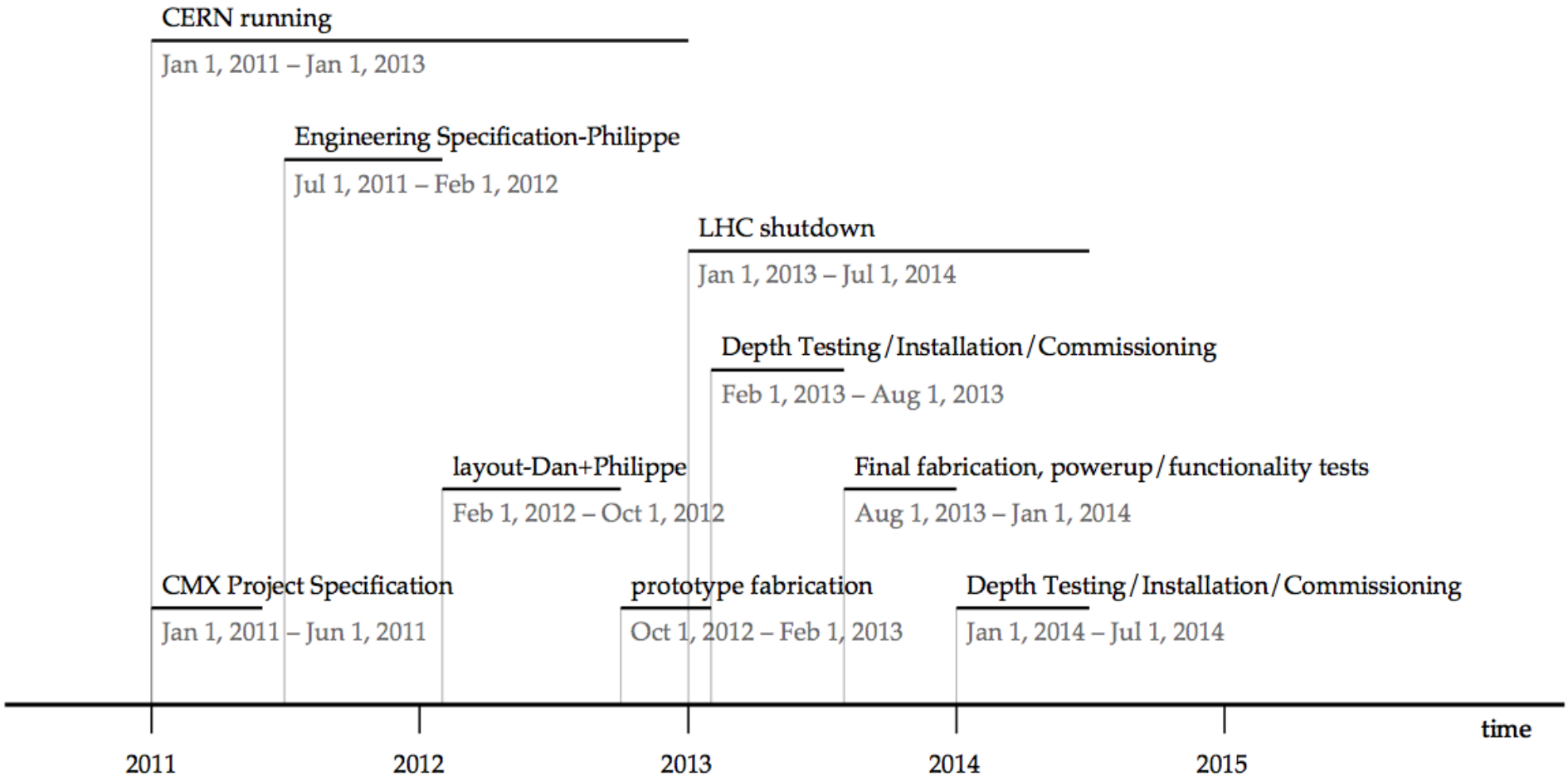
CMX development activities

- Engineering @MSU + CMX input module firmware @CERN
  - Philippe, Dan, Chip and Wojtek
  - Real-time data path layout - backplane to FPGA signal routing
  - Input module firmware currently under test - data capture at 160 MBit/s
  - Prototype blank card mechanical testing
- VME/ACE/TTC (VAT) interface @CERN
  - Yuri + Seth Caughron (recently joined the efforts from software side)
  - 6U VME test card – PCB ready for testing in July
- Power budget estimate
  - Measurements using 6U VME test card
    - ⇨ Estimation vs. real consumption

CMX development schedule (still valid)

- 2011: Project and engineering specifications
  - CMX project Preliminary Design Review (Done)
  - Preliminary design studies (Ongoing)
  - Test rig installed, checked out at MSU (postponed until 2012)
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout (ongoing)
  - CMM firmware ported on CMX
  - Prototype fabrication (fall 2012)
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review
- 2013: Prototype testing/installation/commissioning, final fabrication
  - Full prototype tests in test rig at CERN
  - CMX firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMX modules
- 2014: Final commissioning in the L1Calo trigger system in USA15

CMX development timeline

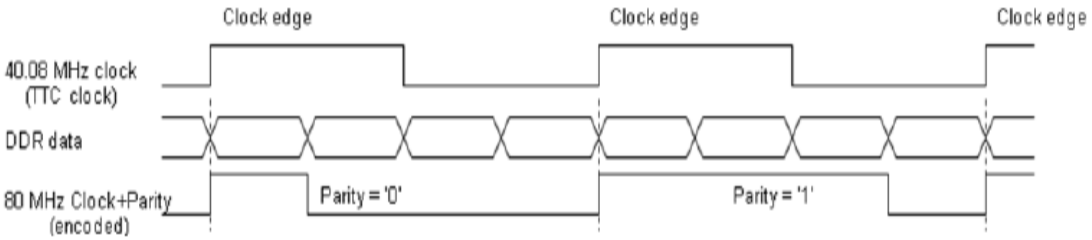


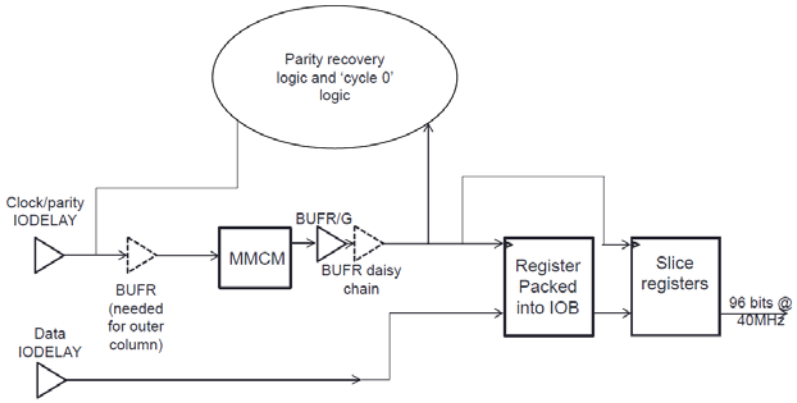
- Prototype design and fabrication
  - CMX schematics and PCB layout (ongoing)
    - ⇨ Dual FPGA design: Base-CMX & TP-CMX (RAL Feb 2012)
    - ⇨ Real-time data path layout (ongoing)
    - ⇨ Input module FW is currently under development and test
    - ⇨ 6U VME test card for VME/ACE/TTC (VAT) interface (PCB ready for testing)
    - ⇨ Power budget estimate
  - CMM firmware ported on CMX
    - ⇨ Most of CMM data path work completed at Stockholm (Pawel & Sam)
      - needs to be adapted to final package choice
    - ⇨ Firmware for VAT interface (2 CPLD + TTC FPGA) to Spartan-3AN (Yuri)
  - Prototype fabrication
    - ⇨ mechanical testing (blank card, backplane connectors, front panel tests)
      - Will happen before real prototype board, but not urgent yet.
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review (L1Calo/TDAQ) Fall/Winter
    - ⇨ After the prototype is tested - final check before going into full production

Backplane data transfer

- Design challenges:
  - 25 backplane traces @ 160 MHz from 16 sources to CMX
  - Absolute and Relative skew of incoming Processor input signals
    - ⇨ Max skew within signals from one source processor module (2 ns ?)
    - ⇨ Unequal length of the traces (source/backplane/destination)
    - ⇨ There will only be a small difference in trace length on CMX, and it will likely not be the dominant source of skew among signals coming from a given processor module
- 3 possible schemes:
  - forwarded coded clock/parity + 24 data (96 bits)
  - forwarded clock + 24 data (96 bits including 1 to 4 parity bits)
  - parity + 24 data (96 bits, no forwarded clock - global clock from TTC)
- Available resources in FPGA:
  - Data phase correction in IODELAY (per trace) – up to 2.4ns
  - Clock phase adjustment in MMCM (per source)
  - Clock capable pins, clock buffers and clock distribution networks

Forwarded coded clock/parity + 24 data



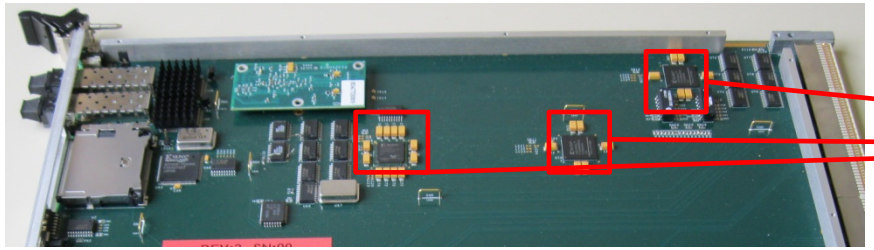


- Data/clock/parity need to be brought in alignment at the FPGA inputs
  - PCB/backplane traces length difference compensated by IODELAY
    - ⇨ Implemented in BLT, software based procedure, done once
- Coded clock/parity – signal used as clock and as data
  - Need MMCM (located far from IO pins) to recover clock
    - ⇨ 16 MMCMs out of 18 used, Extra clock delay
  - “Hand-made” FPGA layout
- Need to re-synchronize to CMX internal clock
- 96 data bits available

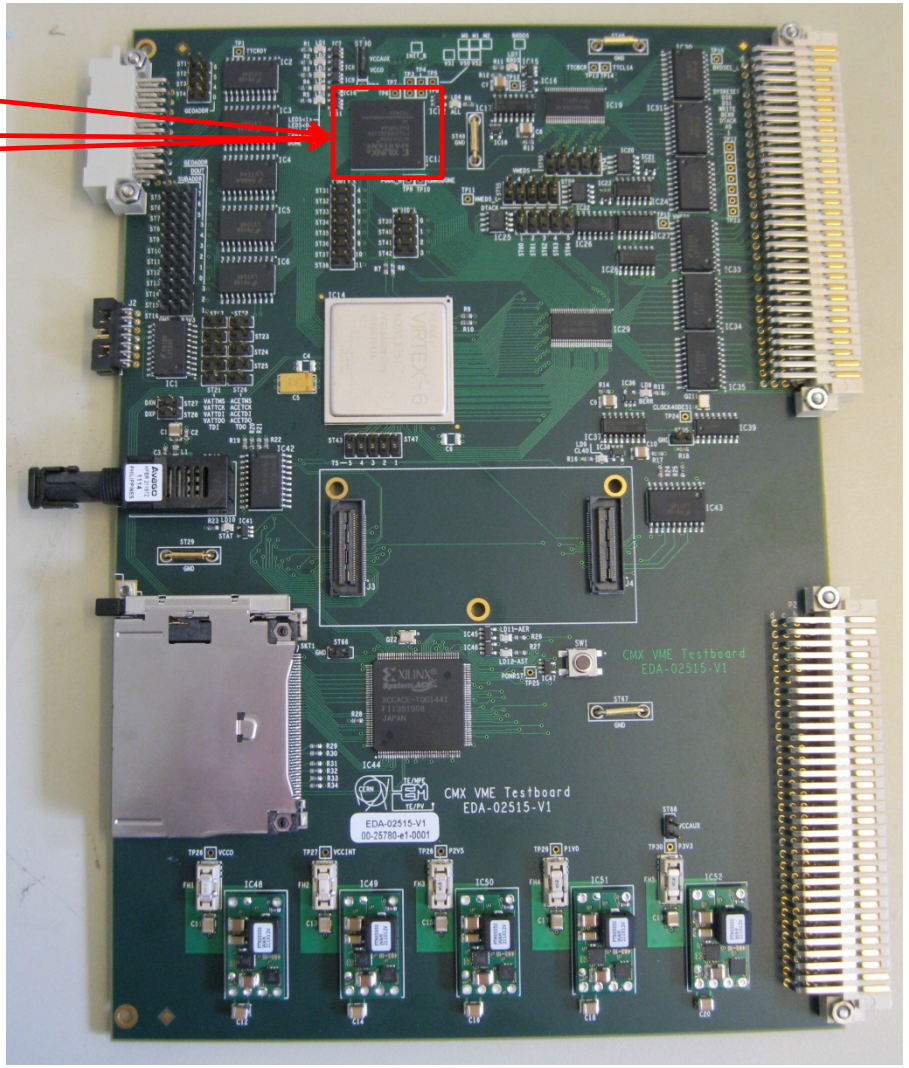
Forwarded clock + 24 data

- Implemented in BLT
  - Tested with up to 8 sources in the crate
- Data/clock/parity need to be brought in alignment at the FPGA inputs
  - PCB/backplane traces length difference compensated by IODELAY
    - ⇨ software based procedure, done once
- Forwarded clock used directly in IO blocks
  - No need for MMCMs
  - Regional clock distribution networks
- Need to re-synchronize to CMX internal clock
- Penalty: < 96 data bits available
  - 1 to 4 parity bits
- → Defined as preferable data transfer scheme
  - PCB/FPGA layout should be able to support all 3 schemes
    - ⇨ regional clock input for all input signals from same CPM/JEM
    - ⇨ cleanest/most direct access possible to one MMCM if needed

Test card for VME/ACE/TTC (VAT) part of CMX



ACE FPGA I2C CPLD VME CPLD



- Redesign HW with new components
  - Fit design into single device
- 6U VME test card:
  - HW/SW implementation
  - Main FPGA re-configuration
  - To be merged into CMX design
- PCB is ready for testing, next:
  - VME/ACE/TTC Firmware for VAT and Virtex6 FPGAs:
    - ⇨ Specify new VME register model
  - Test Stand and software

Conclusions

- Original schedule is maintained
  - With minor adjustments
- Prototype effort proceeding in parallel on 3 fronts according to plan
  - Providing necessary information for technical decisions
    - ⇨ Increasing level of details
- Technical decisions are made
  - Upon agreement within L1 Calorimeter Trigger
    - ⇨ CMX Base/TP functionality, FPGA choice, link speed, data transfer scheme

- General outlook is optimistic