CMX status and plans

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Level-1 Calorimeter Trigger Joint Meeting
CERN, 10-12 October 2012,

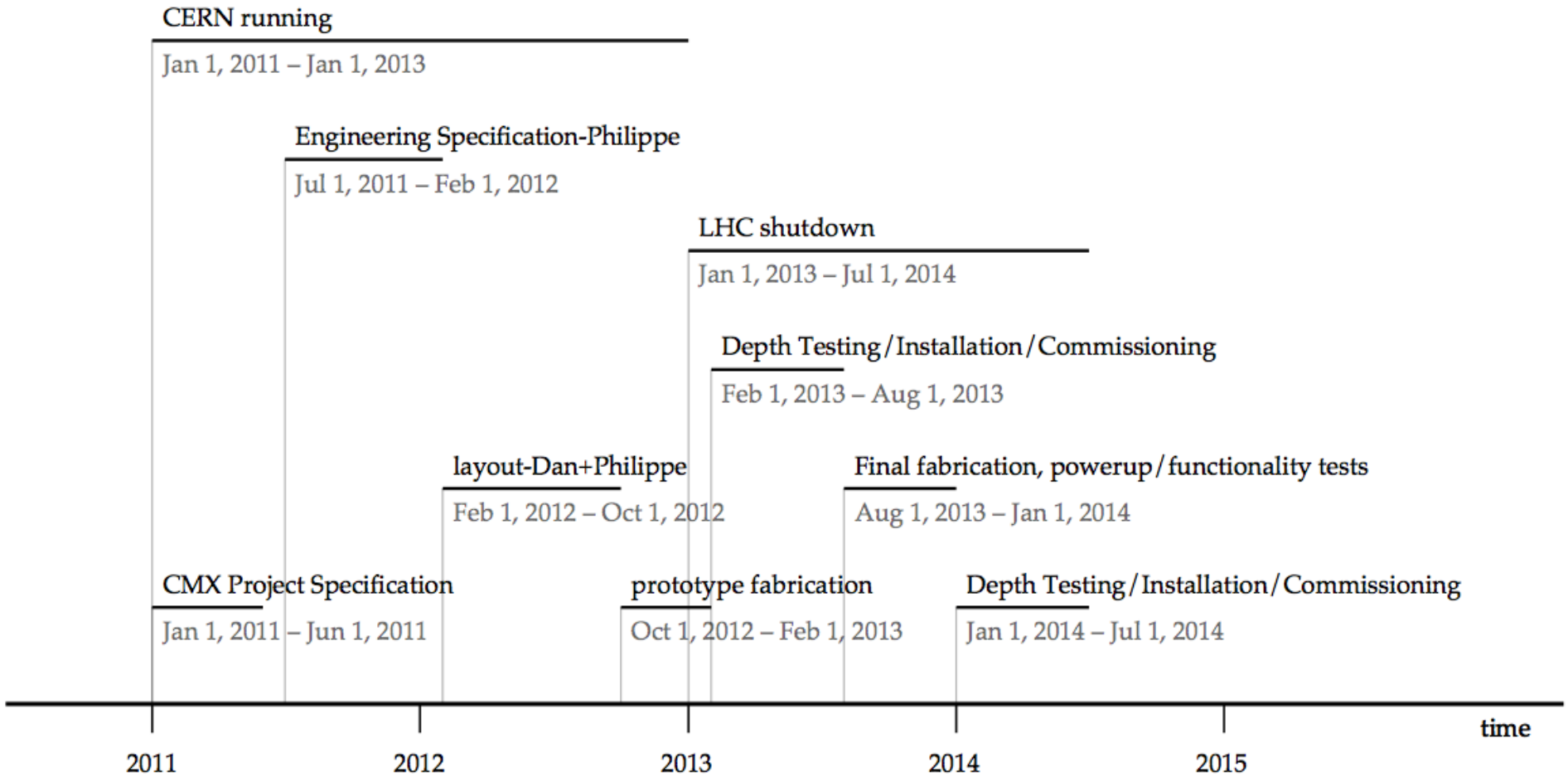
Summary

- Efforts proceeding in parallel on 3 fronts according to plan
  - @MSU – CMX PCB design
    - ⇨ Dan, Philippe, Chip
  - @CERN – VAT card and test rig
    - ⇨ Yuri, Seth
  - @Vancouver – CMX input module firmware
    - ⇨ Wojtek
- Original schedule is maintained
  - With minor adjustments

CMX development schedule (still valid)

- 2011: Project and engineering specifications
  - CMX project Preliminary Design Review (Done)
  - Preliminary design studies (Ongoing)
  - Test rig installed, checked out at MSU (postponed until 2012)
- 2012: Prototype design and fabrication
  - CMX schematics and PCB layout (ongoing)
  - CMM firmware ported on CMX
  - Prototype fabrication (fall 2012)
  - Basic tests for backward compatibility in test rig at MSU
  - Production Readiness Review
- 2013: Prototype testing/installation/commissioning, final fabrication
  - Full prototype tests in test rig at CERN
  - CMX firmware development and test
  - Test in the L1Calo system during shutdown
  - Fabricate and assemble full set of CMX modules
- 2014: Final commissioning in the L1Calo trigger system in USA15

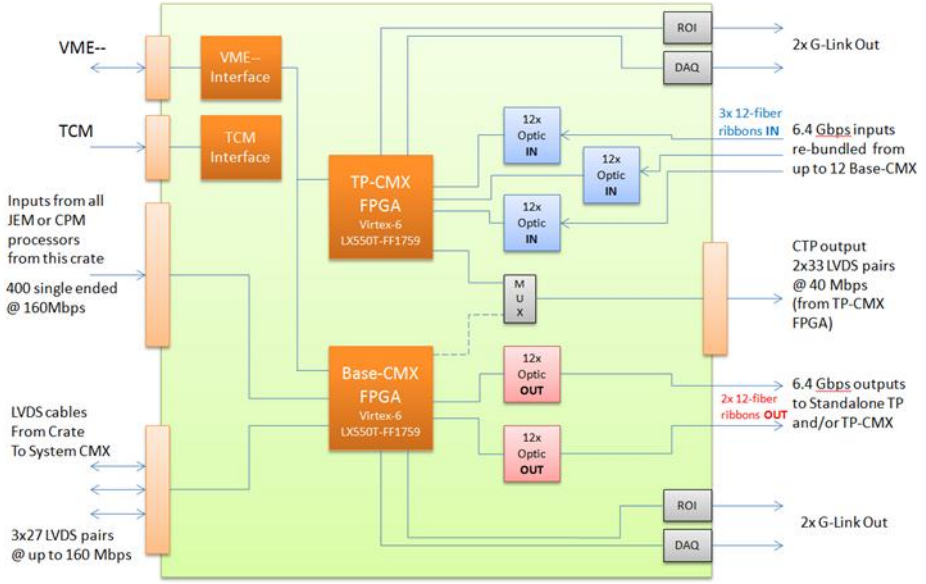
CMX development timeline



Atlas L1Calo CMX Card

CMX is upgrade of CMM with higher capacity

1) Inputs from JEM or CPM modules
   - 40 → 160Mbps (400 signals)
2) Crate CMX to System CMX Cable IO
   - 40 → 160Mbps (81 signals)
3) Output to CTP
   - 40 → 80Mbps (66 signals)
4) Bigger FPGA (Xilinx Virtex 6 VLX550T)
   - e.g. for additional thresholds



Functionality new to CMX

1) Cluster information sent by each CMX to Topological Processor
   - Two 12-fiber ribbons of optical output @6.4Gbps per fiber
2) Optional partial TP capability included
   - A Standalone TP is being built but some TP capability is still desirable on the CMX platform
   - Three 12-fiber ribbons of optical input at @6.4Gbps per fiber
   - Separate Virtex 6 FPGA used for TP Functionality (optionally installed)
     - Most CMX cards will be built without the TP FPGA installed

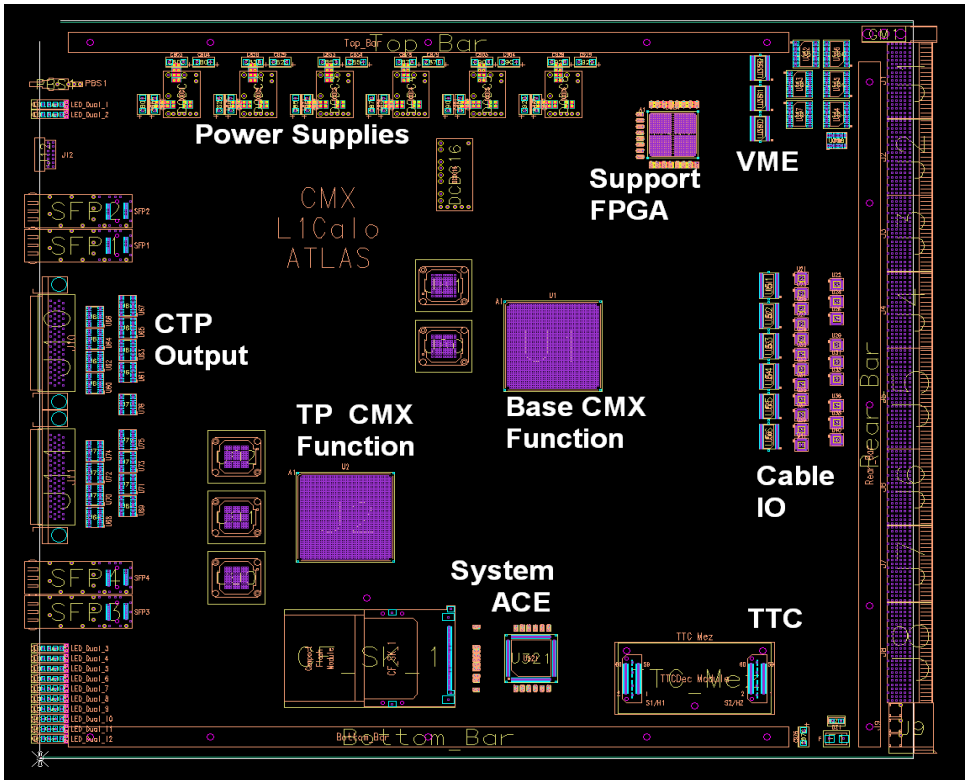
Atlas L1Calo CMX Card

Main Data Path

- Backplane Inputs, Cable IO and CTP Output all understood
  - Maximized signal integrity
    - Critical for 160Mbps bandwidth
    - All critical signals between ground planes
    - PCB trace layout optimized (no extra vias)
    - Pin assigment verified for firmware routability
    - 24-layer card
- Working on details of Optical IO

Ancillary Functions

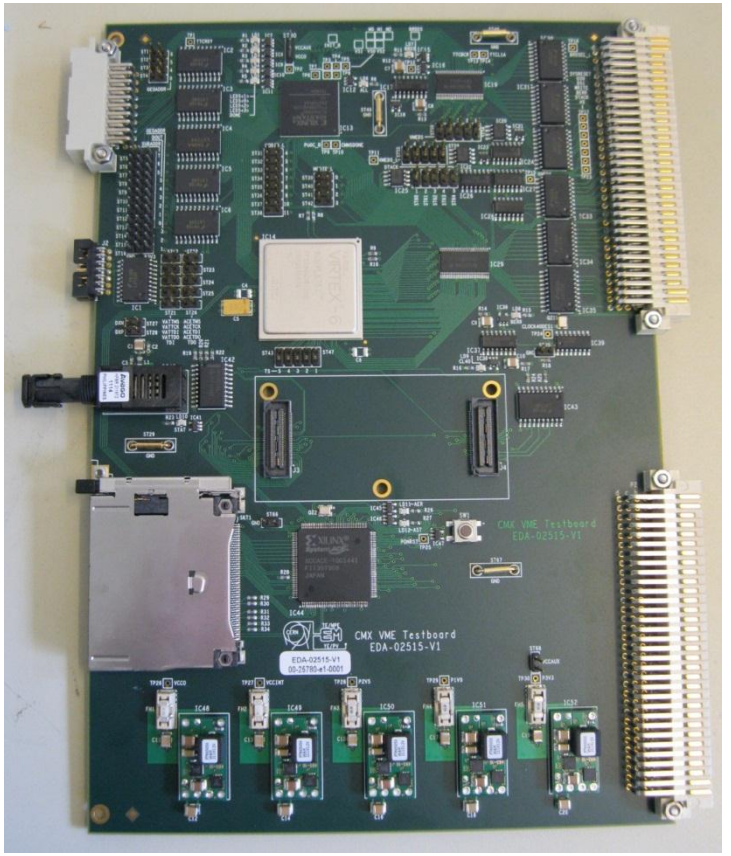
- Understanding Power issues
  - Sizing power supplies
  - Need to satisfy firmware requirements
  - Investigating FPGA heat dissipation
- Working on Clock Distribution
  - All clocks and IOs are synchronized to TTC
- Optimizing overall parts placement



Atlas L1Calo CMX Card

VAT card: parallel effort and study platform

- VME/ACE/TTC (**VAT**) ancillary functions of CMX
- Redesign of CMM with new components
  - Most ancillary functions fit in single Support FPGA
- Build a **6U VME test card**
  - Include a small Virtex 6
  - Practice firmware configuration via System ACE
  - Test bed of operating environment for CMX
  - Can start design of CMX control Software
  - Lessons and details to be merged into CMX
- PCB done June 2012
- Currently working on
  - Firmware for VAT card
  - Test Firmware for Virtex 6 FPGA
  - Test Stand and software



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